MAINTENANCE MANUAL

FM/AM-1200S/A

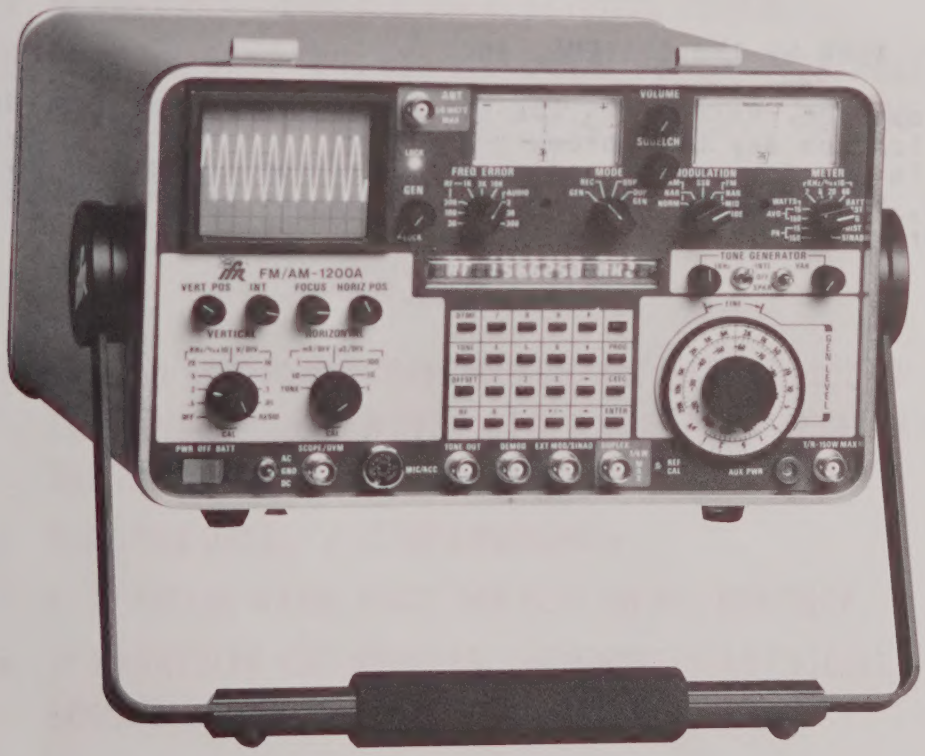
COMMUNICATIONS SERVICE MONITOR

MP MASTER
MA30506

MAINTENANCE MANUAL

FM/AM-1200S/A

COMMUNICATIONS SERVICE MONITOR



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WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

CAUTION

INTEGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FET'S, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNGROUNDED TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

1. BEFORE USING IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.

2. WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.

3. TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.

4. DEVICES MUST NEVER BE INSERTED INTO NOR REMOVED FROM CIRCUITS WITH POWER ON.

5. PC BOARD, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG.

NOTE

Remove any built-in power source, such as a battery, before laying PC Boards on conductive mat or storing in conductive bag.

6. PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BOX.

THE USE OF SIGNAL GENERATORS FOR MAINTENANCE AND OTHER ACTIVITIES CAN BE A SOURCE OF ELECTROMAGNETIC INTERFERENCE TO COMMUNICATION RECEIVERS, WHICH CAN CAUSE DISRUPTION AND INTERFERENCE TO COMMUNICATION SERVICE OUT TO A DISTANCE OF SEVERAL MILES.

USERS OF THIS EQUIPMENT SHOULD SCRUTINIZE ANY OPERATION WHICH RESULTS IN RADIATION OF A SIGNAL (DIRECTLY OR INDIRECTLY) AND SHOULD TAKE NECESSARY PRECAUTIONS TO AVOID POTENTIAL COMMUNICATION INTERFERENCE PROBLEMS.

LIST OF EFFECTIVE PAGES

The manual pages listed below which are affected by a current change or revision, are so identified by a revision number and an asterisk.

Date of issue for original and changed pages are:

Original ..... 0 ..... May 1, 1989

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 274 CONSISTING OF FOLLOWING:

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Title	0
Copyright	0
Warning	0
Caution	0
A	0
B Blank	0
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x Blank	0
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1-6 Blank	0
2-1 thru 2-85	0
2-86 Blank	0
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3-10 Blank	0
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5-4 Blank	0
6-1 thru 6-65	0
6-66 Blank	0
A-1 thru A-7	0
A-8 Blank	0
B-1 thru B-2	0
C-1 thru C-4	0
D-1 thru D-3	0
D-4 Blank	0
E-1	0
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F-1 thru F-2	0
G-1 thru G-3	0
G-4 Blank	0
H-1	0
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PREFACE

SCOPE

This manual contains maintenance instructions for the FM/AM-1200S Communication Service Monitor beginning with unit serial number 6815 and the FM/AM-1200A Communication Service Monitor beginning with serial number 1627. Units prior to these serial numbers should refer to IFR Part Number 1002-5501-100. The information in this manual enables the technician to:

1. Service, test, repair or replace any major assembly or module within the test set.

2. Maintain the operating conditions of the set to expected performance standards.

3. Understand the principles of operation as they relate to the overall operation of the set as well as to individual circuits.

APPLICABILITY

All information contained in this manual applies to both the FM/AM-1200S and FM/AM-1200A models, unless otherwise specified. For brevity, whenever text information is applicable to both models, the units are referenced as "FM/AM-1200S/A" (instead of FM/AM-1200S and FM/AM-1200A individually).

ORGANIZATION

The contents of this manual are divided into six major sections and nine appendices.

A. SECTION 1 - INTRODUCTION:

Provides a brief description of the electrical and mechanical configuration of the FM/AM-1200S/A, intended to familiarize the technician with the overall structure of the set.

B. SECTION 2 - THEORY OF OPERATION:

Describes the FM/AM-1200S/A circuit theory on three levels of complexity: 1) a simplified overview, 2) a functional theory of interactive modules, and 3) a detailed theory of each Module or PC Board Assembly. A block diagram accompanies each discussion of theory.

C. SECTION 3 - PERFORMANCE EVALUATION:

Contains "covers on" functional checkout procedures for evaluating the performance of the FM/AM-1200S/A in each of its operating modes.

D. SECTION 4 - CALIBRATION:

Contains step by step calibration procedures for use at normal calibration intervals or after making repairs of module replacements.

E. SECTION 5 - PREVENTIVE MAINTENANCE:

Contains routine instructions for cleaning and inspecting the FM/AM-1200S/A.

F. SECTION 6 - MECHANICAL ASSEMBLIES, PC BOARDS & SCHEMATICS

Contains component layout drawings for all mechanical assemblies, PC Board assemblies, interconnect diagrams, circuit schematics, waveforms, and charts reflecting voltage levels keyed to test points.

G. APPENDICES:

Contains useful supplementary maintenance and operational data.

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SECTION 1 - INTRODUCTION

1-1 GENERAL

This section provides a brief description of the internal electrical and mechanical configurations of the FM/AM-1200S/A, and will familiarize the technician with the overall structure of the set. FM/AM-1200S/A specifications are in Appendix A.

1-2 DIFFERENCES BETWEEN MODELS

The FM/AM-1200S is identical to the FM/AM-1200A with the following exceptions:

A. The FM/AM-1200S contains a Spectrum Analyzer consisting of the Analyzer RF, Analyzer IF and Analyzer Log Amplifier Modules.

B. The Scope Control PC Board in the FM/AM-1200S is different from the one installed in the FM/AM-1200A.

C. The graticule overlay on the FM/AM-1200S is marked with a dBm scale, while the overlay on the FM/AM-1200A is not.

D. The FM/AM-1200S contains Duplex/Tracking Generator Module while the FM/AM-1200A contains a Duplex Generator Assembly.

1-3 ELECTRICAL DESCRIPTION

The FM/AM-1200S/A is a processor controlled, digitally synthesized FM/AM/SSB receiver and generator, with an integral Oscilloscope/ Spectrum Analyzer. The receiver is a triple conversion superheterodyne receiver capable of receiving signals from 250 kHz to 999.9999 MHz. The Signal Generator can produce modulated or unmodulated RF signals from 250 kHz to 999.9999 MHz. A Function Generator can produce six functions with ranges from 10 Hz to 10 kHz and one function up to 30 kHz. The Duplex Generator can produce a signal up to 49.99 MHz from the received frequency. The Oscilloscope and Spectrum Analyzer on the FM/AM-1200S utilize a common CRT. The Bandwidth of the Oscilloscope is DC to 1 MHz. The dynamic range of the Spectrum Analyzer is from -30 dBm to -100 dBm.

1-3-1 FUNCTIONAL CONSTRUCTION

Individual modules which make up each function are listed as follows:

1. Power Supply
   - Line Supply Assembly
   - Inverter Assembly
   - Battery Charger PC Board

2. Reference Frequencies
   - Frequency Standard PC Board
   - Standard TCXO or Optional Oven Oscillator
   - Digital Module

3. Processor
   - Processor PC Board
   - Interface I/O PC Board
   - DVM I/O PC Board
   - Display PC Board
   - Keyboard
   - RS-232c (see NOTE 1)

4. Frequency Synthesizer
   - High Loop Assembly
   - Dual VCO Assembly
   - 1120 MHz Low-pass Filter
   - High/Low-pass Filter
   - Low Loop Assembly

5. Receive/Generate
   - Output Amplifier Assembly
   - IF Module Assembly
   - Frequency Synthesizer Function
   - 10.7 MHz Gen/Rec Assembly
   - Receive Audio PC Board
   - Generate Audio PC Board
   - Duplex Generator Assembly (see NOTE 2)
   - Duplex/Tracking Generator (see NOTE 3)
   - Function Generator
   - Front Panel Monitoring Displays

6. Oscilloscope/Spectrum Analyzer
   - CRT Assembly
   - Scope Control PC Board
   - Scope Power Supply PC Board
   - Analyzer RF Assembly (see NOTE 3)
   - Analyzer IF Assembly (see NOTE 3)
   - Analyzer Log Amplifier Assembly (see NOTE 3)

NOTE: 1. Option Combinations:

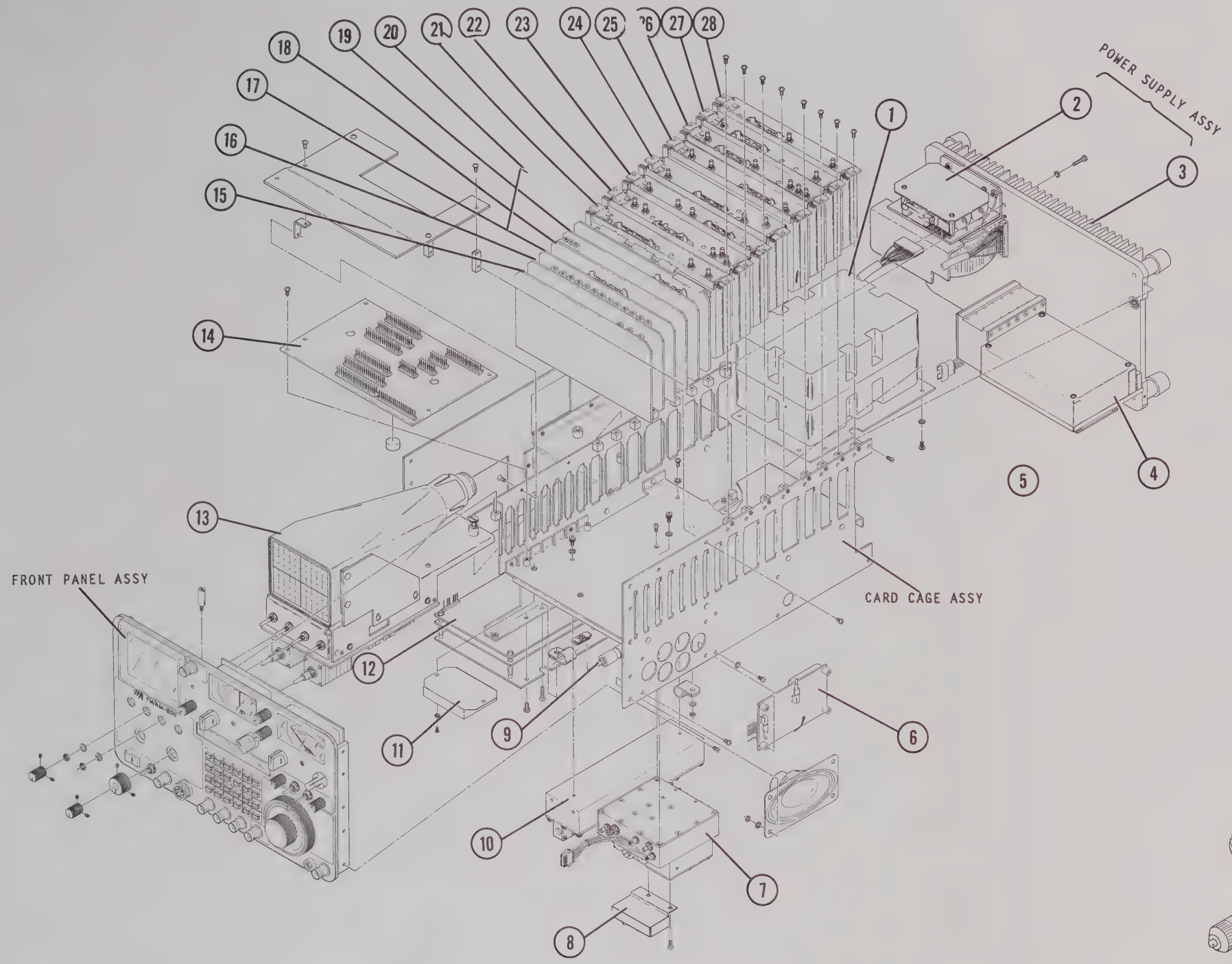
- GPIB may be substituted for RS-232c
- Cellular may be included with RS-232c only
- Encode/Decode may be included with Cellular

2. FM/AM-1200A Only

3. FM/AM-1200S Only

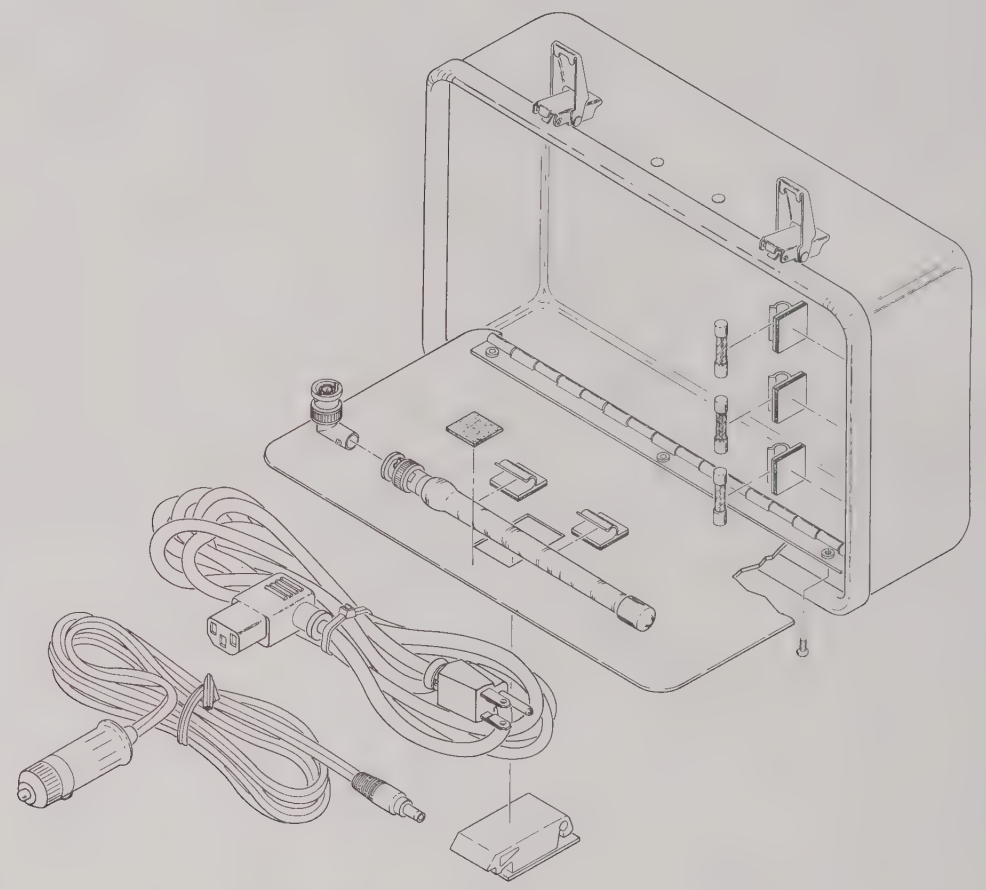
1-4 MECHANICAL DESCRIPTION

Figure 1-1 is an "exploded" composite view of the FM/AM-1200S/A, identifying and locating its major assemblies. Front and rear panel controls, connectors and indicators are identified in Figure 1-2. This illustration foldout is to provide ready identification of references when performing testing or calibration of the FM/AM-1200S/A.

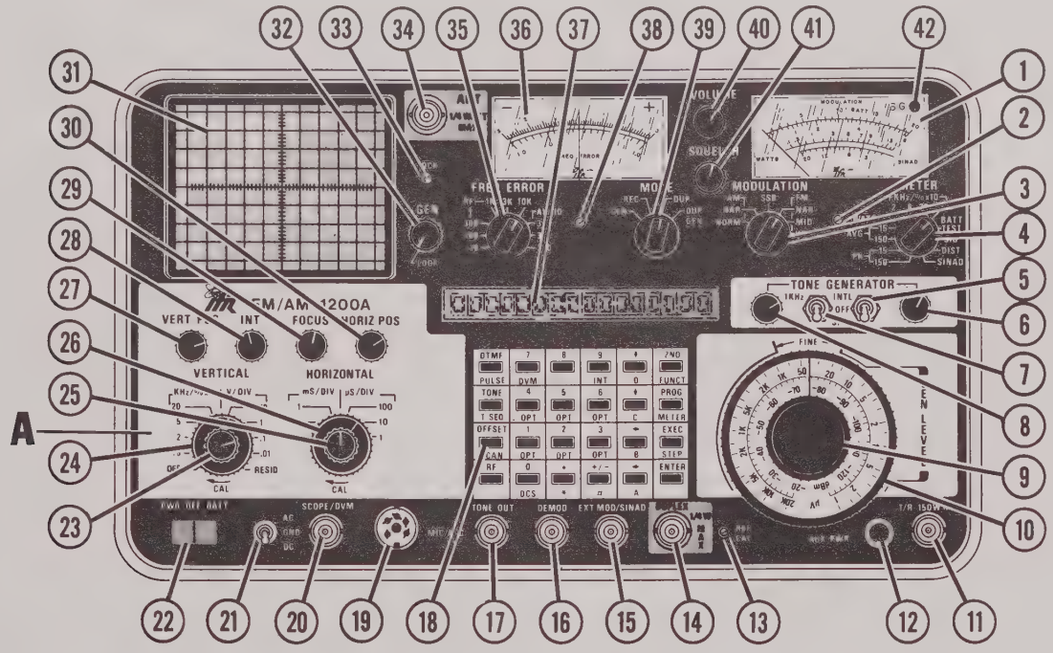


LEGEND			
1.	Battery	15.	Gen. Audio PC Board
2.	Line Supply	16.	Rec. Audio PC Board
3.	Rear Panel	17.	Tone Gen. PC Board
4.	Battery Charger & Inverter Supply Assy.	18.	DVM I/O PC Board
5.	Output Amp. Assy.	19.	CPU PC Board
6.	Frequency Standard	20.	Interface PC Board
7.	IF Block Assy.	21.	Fast Low Loop Assy
8.	Mixer Null Assy.	22.	High Loop Assy
9.	Low-pass Filter Assy.	23.	Duplex/Tracker Assy.*
10.	Dual VCO Assy.	24.	Digital Assy.
11.	High/Low-pass Filter Assy.	25.	10.7 MHz Gen/Rec Assy.
12.	Cellular Assy. (Option)	26.	Analyzer RF Assy.**
13.	Scope Assy.	27.	Analyzer IF Assy.**
14.	Motherboard	28.	Analyzer Log Amp Assy.**

* In FM/AM-1200A. this is replaced by Duplex Assy.
** In FM/AM-1200S only.

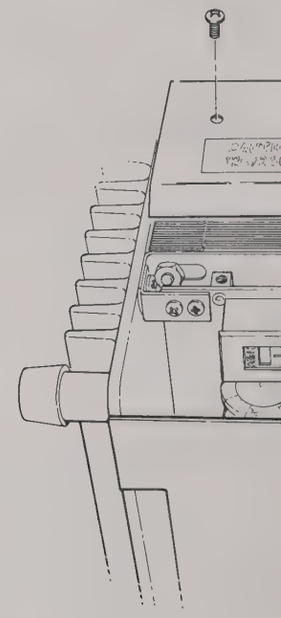


LID ASSEMBLY



1. MODULATION METER
2. Modulation Meter Zero Adjustment
3. MODULATION Select Control
4. Modulation METER Control
5. VAR Tone Selector Switch
6. VAR Tone Level Control
7. 1 kHz Tone Selector Switch
8. 1 kHz Tone Level Control
9. RF Level Attenuator Control
10. RF Level Attenuator Vernier Control
11. T/R Connector
12. AUX POWER Connector (Option 05 Gen. Amp only)
13. REF CAL Adjustment
14. DUPLEX Output Connector
15. EXT MOD/SINAD Connector
16. DEMOD Connector
17. TONE OUT Connector
18. Keyboard
19. MIC/ACC Connector
20. SCOPE/DVM Connector
21. AC/GND/DC Switch (Scope)
22. PWR/OFF/BATT Switch
23. Scope VERTICAL Attenuator Vernier Control
24. VERTICAL Attenuator Selector Control
25. Scope HORIZONTAL Sweep Vernier Control
26. HORIZONTAL Sweep Selector Control
27. VERT POS Control
28. INT Control
29. FOCUS Control
30. HORIZ POS Control
31. CRT Display
32. GEN/LOCK Control
33. LOCK Lamp
34. ANT Connector
35. FREQ ERROR Meter Range Selector Control
36. FREQ ERROR Meter
37. VFD (Vacuum Fluorescent Display)
38. FREQ ERROR Meter Zero Adjustment
39. MODE Selector Control
40. VOLUME Control
41. SQUELCH Control
42. SIG Indicator Lamp

FM/AM-
FRONT



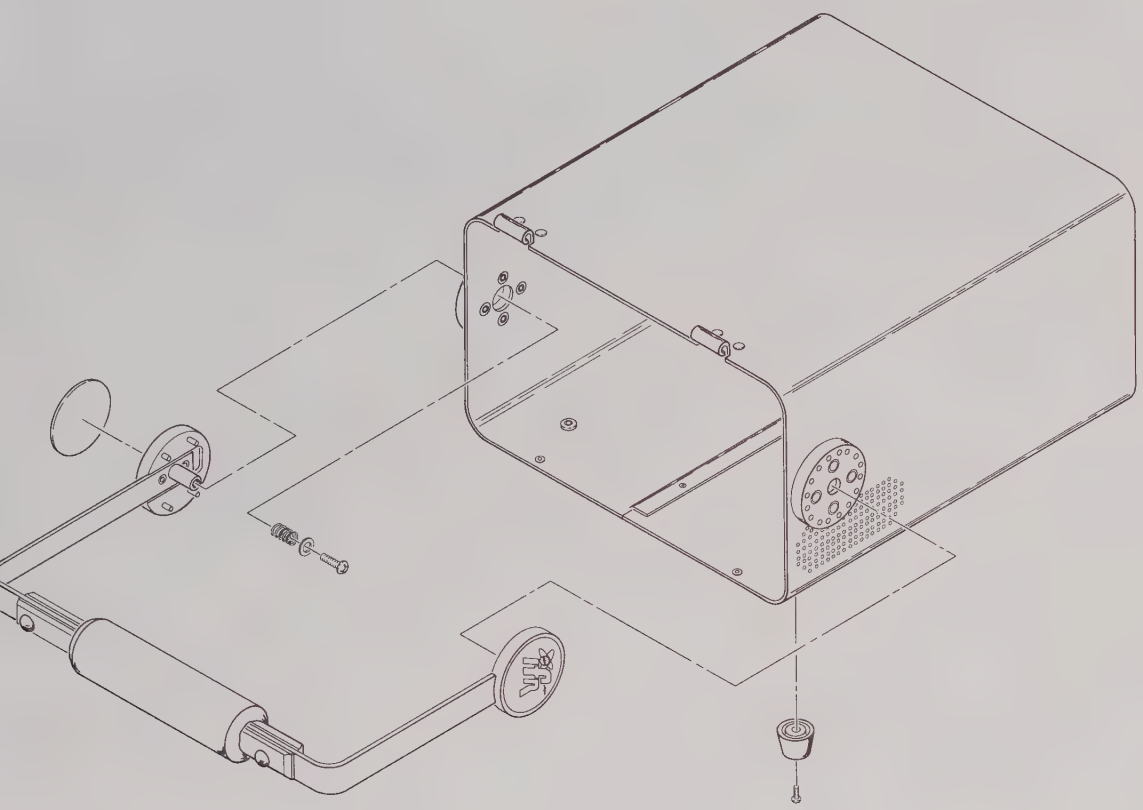
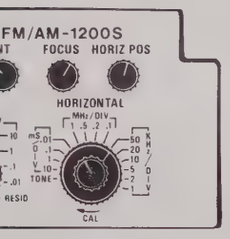
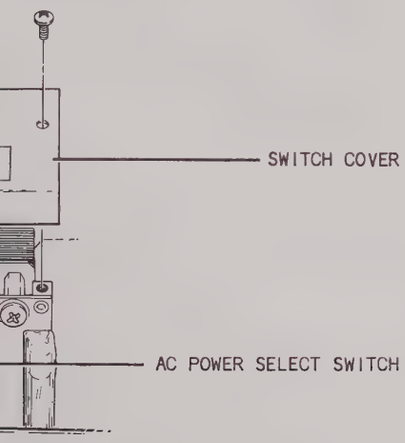


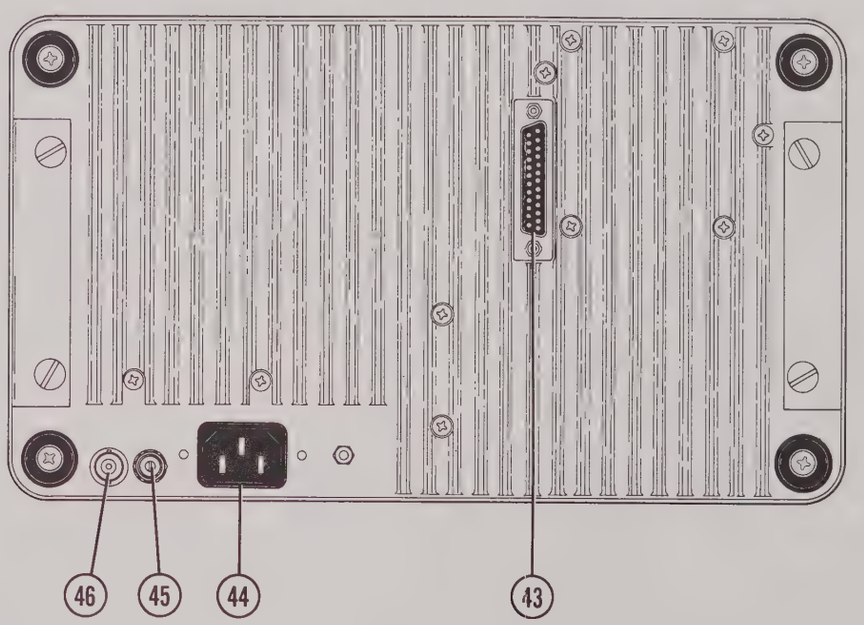
Figure 1-1 FM/AM-1200S/A Composite
(Module Identification)



ETAIL **A**

00S
NEL CORNER PIECE





43. RS-232c Connector (see Note)
44. AC Power Input Connector
45. DC Power Input Connector
46. External Reference Connector

NOTE: RS-232c Connector (43) is also used to connect the Cellular Option (FM/AM-1200S only), the Encode/Decode Option (FM/AM-1200S only) or to connect the FM/AM-1200S/A to a computer interface.

Figure 1-2 Description of Controls, Connectors & Indicators

SECTION 2 - THEORY OF OPERATION

2-1 GENERAL

This section contains three levels of Theory of Operation using following organization:

A. System Theory of Operation

Paragraph 2-2 provides a simplified description of signal flow through the FM/AM-1200S/A for both Receiver and Signal Generator operation. This description is based on the System Block Diagram shown in Figure 2-1. A brief overview of the Oscilloscope and Spectrum Analyzer is also covered within this paragraph.

B. Functional Theory of Operation

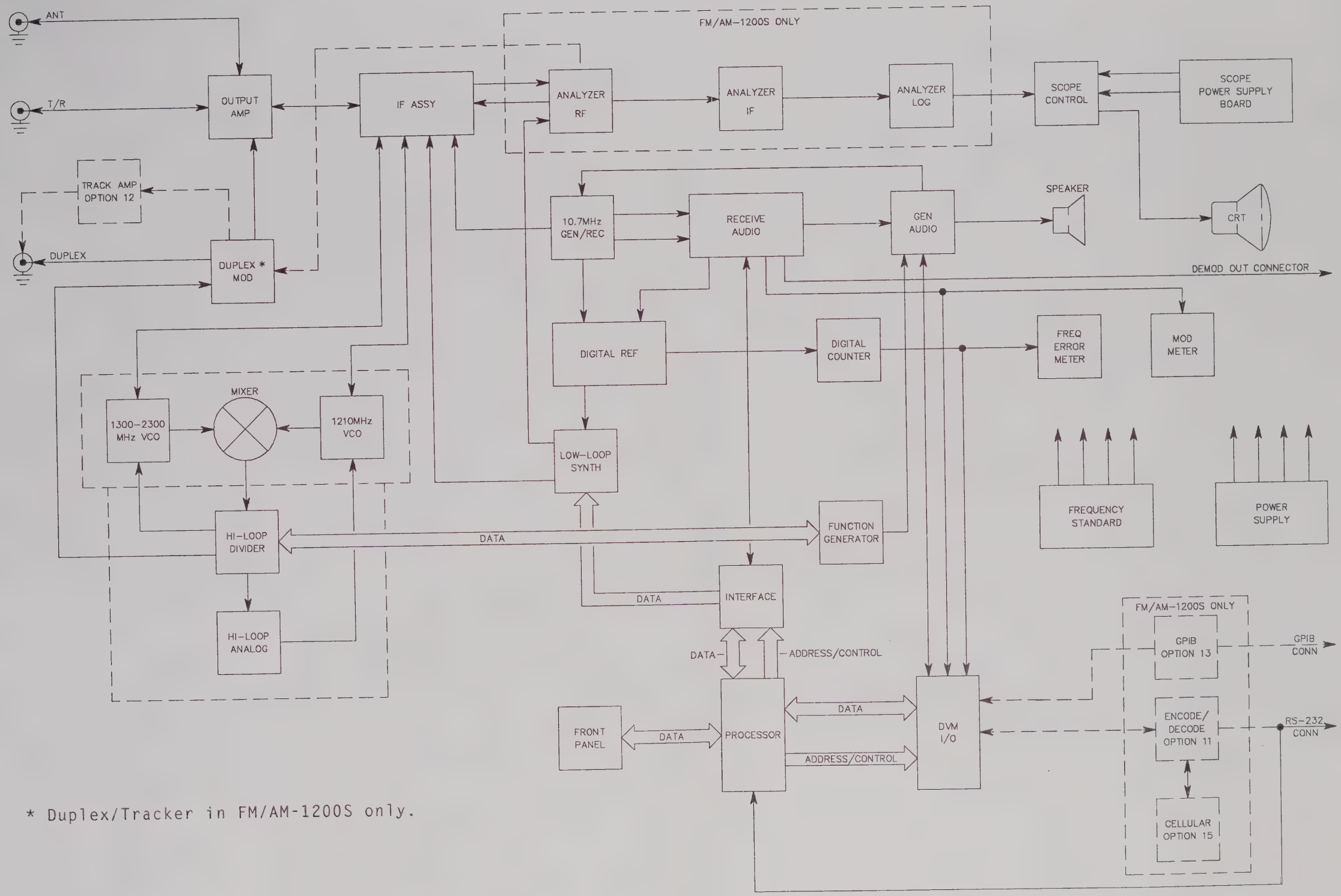
Paragraph 2-3 provides a description of the major functional groupings in the FM/AM-1200S/A. This description is based upon the corresponding functional block diagrams as shown.

C. Module Theory of Operation

Paragraph 2-4 provides detailed theory of operation for each module and/or assembly contained in the FM/AM-1200S/A. All discussions are based upon the accompanying block diagrams for each module.

2-2 SYSTEM THEORY OF OPERATION

The FM/AM-1200S/A is a processor controlled, digitally synthesized FM/AM/SSB Receiver and Generator, with an integral Oscilloscope/ Spectrum Analyzer. The triple conversion superheterodyne receiver is capable of receiving signals from 250 kHz to 999.9999 MHz. The Signal Generator is capable of producing modulated or unmodulated RF signals from 250 kHz to 999.9999 MHz. Tone configurations available to modulate the generator are Ramp, Triangle, Square, Sine, DTMF, Pulse and DCS. A Duplex Generator can produce a signal to ±49.99 MHz from the received frequency. The Spectrum Analyzer (installed in the FM/AM-1200S only) utilizes a common CRT with the Oscilloscope. The bandwidth of the Oscilloscope is DC to 1 MHz. The dynamic range of the Spectrum Analyzer is from -30 dBm to -100 dBm.



* Duplex/Tracker in FM/AM-1200S only.

Figure 2-1 System Block Diagram

In receive operation mode, the input frequency is converted to 10.7 MHz in the IF Block Assembly. The IF signal is filtered and sent to the FREQ ERROR Meter and demod circuits. This demodulated audio signal is then applied to the DEMOD Connector, to the Speaker through an audio amplifier, and to the MODULATION Meter through a scaling circuit.

In generate operation mode, the 10.7 MHz Rec/Gen Module provides a frequency of 10.7 MHz, which can be either frequency or amplitude modulated. This signal is converted to the selected RF, amplified, then applied to the T/R Connector through a selectable attenuator.

In duplex mode, a separate Signal Generator produces an RF signal at a selected offset frequency to ±49.99 MHz. This offset frequency is applied directly to the DUPLEX Connector and through a fixed attenuator to the T/R Connector.

The FM/AM-1200S/A Function Generator produces a ramp, triangle or square wave at frequencies between 10 Hz and 10 kHz, and a sine wave up to 30 kHz. The Function Generator also produces a Digitally Coded Squelch and a Pulse Signal. The DVM I/O PC Board generates a Dual Tone Multiple Frequency. The selected signal (waveform) is applied to the TONE OUT Connector. This signal can be used to modulate the 10.7 MHz IF or it can be applied directly to the Speaker. An additional square wave is also generated, for use as a reference, during audio frequency error measurements. A fixed 1 kHz sine wave is also generated in the Digital Module and applied to the TONE OUT Connector, which can either be used to modulate the 10.7 MHz IF or applied to the Speaker.

The FM/AM-1200S/A Oscilloscope is a single trace, 1 MHz unit which can monitor demod audio or generate audio and external signals applied at the SCOPE/DVM Connector. The Spectrum Analyzer (in the FM/AM-1200S only) can be used to monitor generated or received signals. Received signal levels can be monitored from -30 dBm to -100 dBm.

2-3 FUNCTIONAL THEORY OF OPERATION

2-3-1 PROCESSOR OPERATION

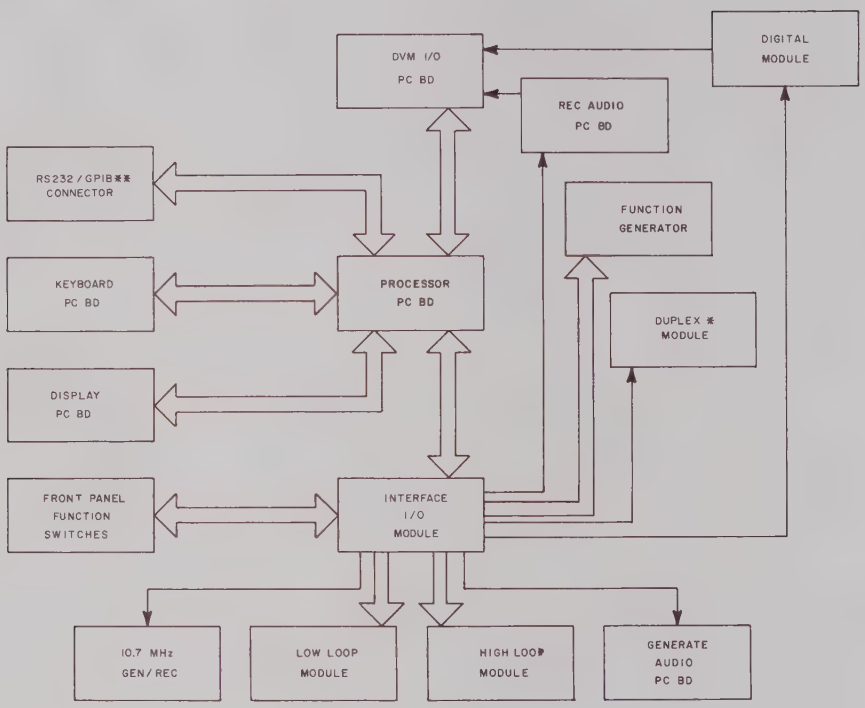


Figure 2-2 Processor Functional Block Diagram

** GPIB - Option 13

The Processor, through the Interface PC Board, transfers all data within the FM/AM-1200S/A over an internal data bus. It communicates directly with the Interface PC Board, Keyboard, VFD, DVM I/O PC Board and RS-232c Connector. Options which communicate with the Processor, when available, include GPIB (in lieu of RS-232c) and Cellular (used with RS-232c only). The Interface PC Board communicates directly with the High Loop Module, Low Loop Module, Function Generator PC Board, Duplex Module, Generate Audio PC Board, 10.7 MHz Gen/Rec Module, Digital Module, Receive Audio PC Board, and the Front Panel.

The Processor contains two routines. The first routine, "the Front Panel Routine," receives all data from the keyboard and control settings, then processes it. The Data is output to the hardware latches on the Interface PC Board to the appropriate modules. The second routine of the processor is the RS-232c routine. The data flows the same as in the Front Panel routine, except all control input enters through the RS-232c Connector.

2-3-2 RECEIVER SECTION OPERATION

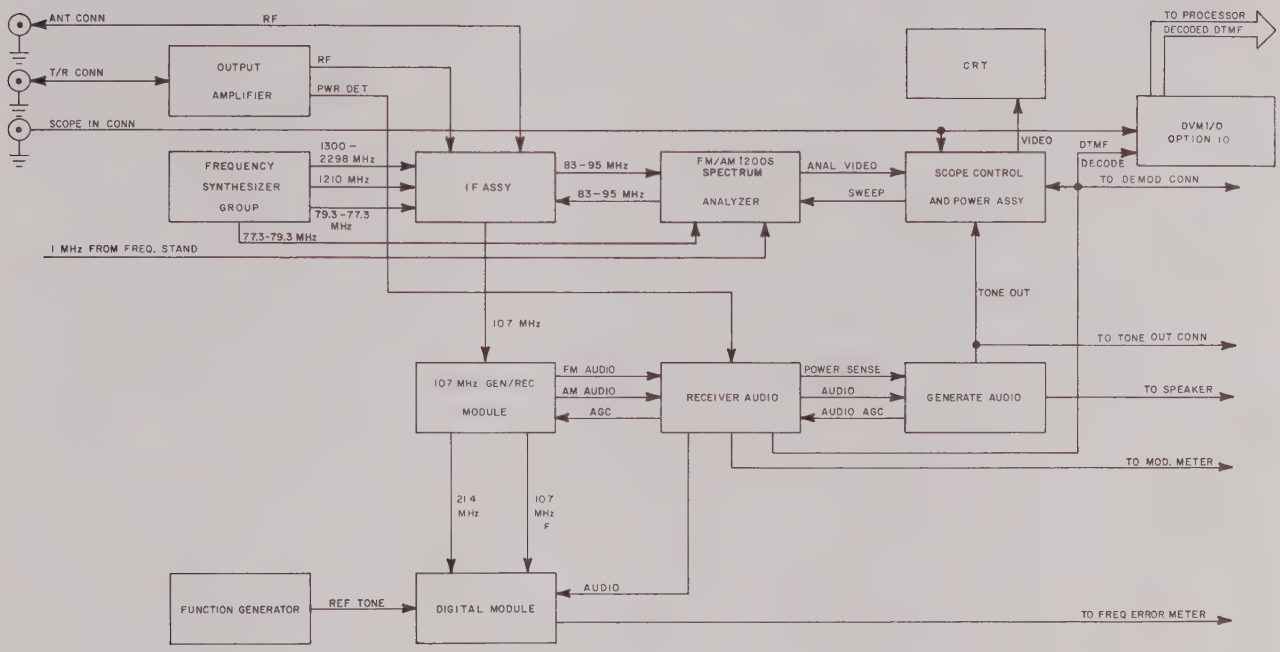


Figure 2-3 Receiver Functional Block Diagram

RF signals are received through either the ANT Connector or T/R Connector. Off-The-Air signals are received at the ANT Connector; whereas a transmitter under test is connected directly to the T/R Connector. The signal received at the T/R Connector is attenuated 80 dB and applied to an antenna relay in the IF Block Assembly. Off-The-Air signals received at the ANT Connector are fed through a static protect circuit, RF gain stage and then to the antenna relay.

The signal received at the ANT connector is coupled through the antenna relay (which is normally energized) to the 1000 MHz Low-pass Filter in the IF Block Assembly. If a signal of 100 mW or greater is received at the T/R Connector, the relay is de-energized and the signal from the T/R Connector is coupled to the 1000 MHz Low-pass Filter.

Whichever received signal source is selected, the received RF is converted twice in the IF Block Assembly by two local oscillators in the dual VCO from the Frequency Synthesizer Group. In the FM/AM-1200S, this converted signal (83-95 MHz) is fed to the Spectrum Analyzer for display. In both the FM/AM-1200S and the FM/AM-1200A, the signal is fed back to the IF module where it is down-converted to 10.7 MHz by a

local oscillator signal from the Low Loop Synthesizer. The 10.7 MHz signal is fed to the 10.7 MHz Gen/Rec Module where it is bandpass filtered and demodulated. The 10.7 MHz Gen/Rec Module has an AM and an FM detector. The AM detector produces a DC level (AGC) proportional to the level of the 10.7 MHz IF input. When an AM signal is present, the demod audio signal will ride on this DC level. The FM detector sends a 10.7 MHz signal which is sent to the Digital module for frequency error measurements. When an FM signal is present, the FM detector also produces a demod audio signal. The demodulated audio signal from the 10.7 MHz Gen/Rec Module is fed to the Receive Audio PC Board where it is amplified and audio bandpass filtered. The Receive Audio PC Board output is fed to the Generate Audio PC Board, front panel DEMOD Connector, Oscilloscope, Front Panel MODULATION Meter and Digital Module. The output from the Generate Audio PC Board is fed through an audio amplifier to the Speaker. The audio signal fed to the Digital Module is compared with a reference tone from the Function Generator to produce the audio error signal which is fed to the FREQUENCY ERROR Meter. If the DVM I/O PC Board is installed, AC or DC voltages present at the SCOPE/DVM Connector, and DTMF in the demodulated audio signal can be decoded and displayed on the Vacuum Fluorescent Display (VFD).

2-3-3 GENERATOR SECTION OPERATION

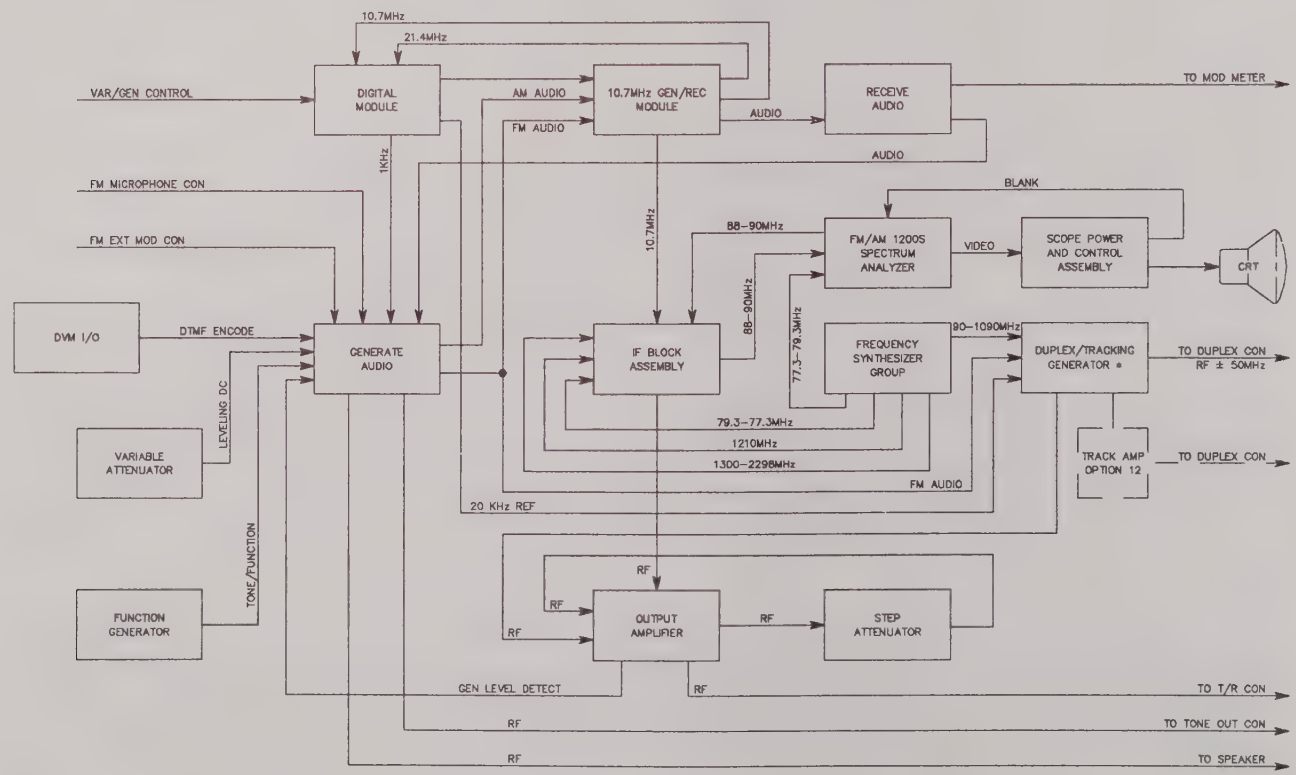


Figure 2-4 Generator Functional Block Diagram

In generate mode, a 21.4 MHz VCO circuit in the 10.7 MHz Gen/Rec Module produces a 21.4 MHz signal. This signal is phase-locked to the 10 MHz Frequency Standard by a phase-lock loop in the Digital Module. The 21.4 MHz signal is divided by 2, to produce the 10.7 MHz IF, which passes through a leveler/modulator circuit for level control, then to the IF Block Assembly.

The 10.7 MHz IF is mixed with the low loop synthesizer signal (77.3001-79.300 MHz) to produce an 88-90 MHz IF which is fed through an 89 MHz bandpass filter and amplified. At this point, the 88-90 MHz IF is fed to the Analyzer RF Module for analyzer display, and to the second mixer in the IF Block Assembly. The second mixer mixes the 88-90 MHz IF with the 1210 MHz signal from the High Loop Synthesizer Module to produce a 1298-1300 MHz IF. This signal is amplified, filtered and fed to the third mixer. The third mixer mixes the 1298-1300 MHz IF with the 1300-2298 MHz signal from the High Loop Synthesizer Module to produce the selected RF signal. This signal is fed to a 1000 MHz Low-pass Filter, then out of the IF Block Assembly to the Output Amplifier Assembly. In the Output Amplifier, the RF signal is amplified, then its level is sampled to produce a level control signal to the leveler/ modulator in the Generate Audio Module. Thus, the leveler/modulator circuit adjusts the level of the 21.4 MHz generator output sufficiently to vary 0-11 dB at the Output Amplifier. The RF signal then goes to a 10 dB step attenuator for operator generator level selection, then back to the Output Amplifier, where it is attenuated an additional 20 dB. The signal is then routed to the T/R Connectors and to the Unit Under Test.

To modulate the carrier, internal signals from the Digital Module (1 kHz sine wave), Function Generator, DVM I/O (DTMF), and external signals from the MIC/ACC and EXT MOD Connectors are combined in the leveler/ modulator circuit of the Generate Audio Module. For Frequency Modulation, the output from the Generate Audio PC Board varies the 21.4 MHz generator frequency. For amplitude modulation, the combined audio signal is fed to the fine attenuator. The output of the fine attenuator is summed with the control voltage from the output amplifier on the Generate Audio PC Board. This signal is fed to the 10.7 MHz GEN/REC Module where it controls the RF output level and AM modulates the 10.7 MHz signal.

The Duplex/Tracker (Duplex Generator in the FM/AM-1200A) receives a 20 kHz reference frequency from the Digital Module and a 90-1088 MHz signal representing the selected RF from the High Loop Module in the Frequency Synthesizer. According to the frequency offset selected, the generator frequency is up to 49.99 MHz above or below the selected RF. One Duplex/Tracker (Duplex Generator) output is through the DUPLEX Connector on the Front Panel at -40 dBm in the DUPLEX LOW Mode and -15 dBm in the DUPLEX HIGH Mode (-60 dBm for the FM/AM-1200A). A second output is to the Output Amplifier, which attenuates the signal and routes it to the T/R Connector at a -85 dBm level (-80 dBm in the FM/AM-1200A).

In the Tracking Modes (available only with Tracking Generator Option 12 installed), the tracking output from the Duplex/Tracker is routed to the Track Amp. The Track Amp passes the signal unchanged from the Duplex/Tracker to the DUPLEX Connector in the TRACK LOW (-50 dBm) and TRACK MED (-15 dBm) Modes. In the TRACK HIGH Mode, however, the -15 dBm output from the Duplex/Tracker is amplified to a -6 dBm level, then routed to the DUPLEX Connector.

2-3-4 FREQUENCY SYNTHESIS OPERATION

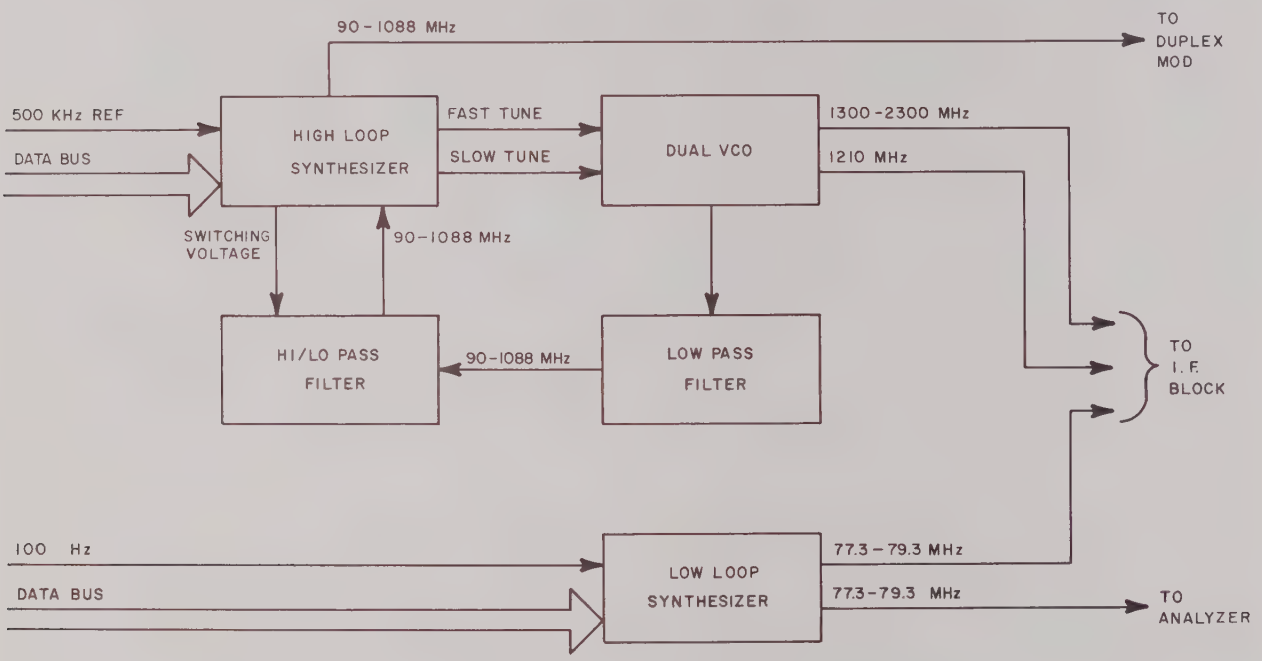


Figure 2-5 Frequency Synthesis Functional Block Diagram

The Frequency Synthesis Group consists of the High Loop Synthesizer, Low Loop Synthesizer, Low-pass Filter and Hi/Low-pass Filter. The Low Loop Synthesizer generates a 77.3-79.3 MHz signal, selectable in 100 Hz steps. This signal is fed to both the IF Block Assembly and Analyzer RF Module. The High Loop Synthesizer generates two DC voltages which control two separate oscillators in the Dual VCO Module. One oscillator operates at 1300-2300 MHz, the other operates at 1210 MHz. Both the 1210 MHz and 1300-2300 MHz signals are fed to the IF Block Assembly in addition to being mixed within the module to produce a 90-1088 MHz signal. The mixed signal is fed through the Low-pass and Hi/Low-pass Filters to the High Loop Module. There it is divided down and compared with a 500 kHz reference signal received from the Frequency Standard PC Board. The 90-1090 MHz signal is also sent from the High Loop Synthesizer Module to the Duplex Module.

2-3-5 REFERENCE FREQUENCY OPERATION

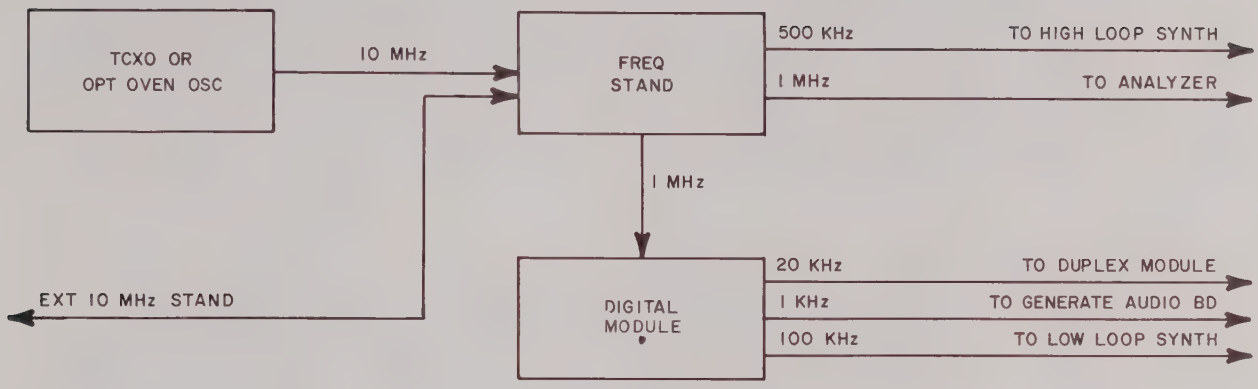


Figure 2-6 Reference Frequency Functional Block Diagram

The FM/AM-1200S/A uses 10 MHz as the primary standard frequency. A TCXO (Temperature Compensated Crystal Oscillator) or, optionally, an oven oscillator normally produces this frequency. An external 10 MHz standard can also be used in place of the TCXO. The Frequency Standard divides the 10 MHz to 1 MHz which is sent to the Digital Module and Analyzer RF Module, and to 500 kHz which is fed to the High Loop Synthesizer Module. The Digital Module further divides the 1 MHz signal to 20 kHz which is fed to the Duplex Module, to 1 kHz sine wave which is sent to the Generate Audio PC Board and to 100 Hz which is fed to the Low Loop Synthesizer Module.

2-3-6 OSCILLOSCOPE/SPECTRUM ANALYZER OPERATION

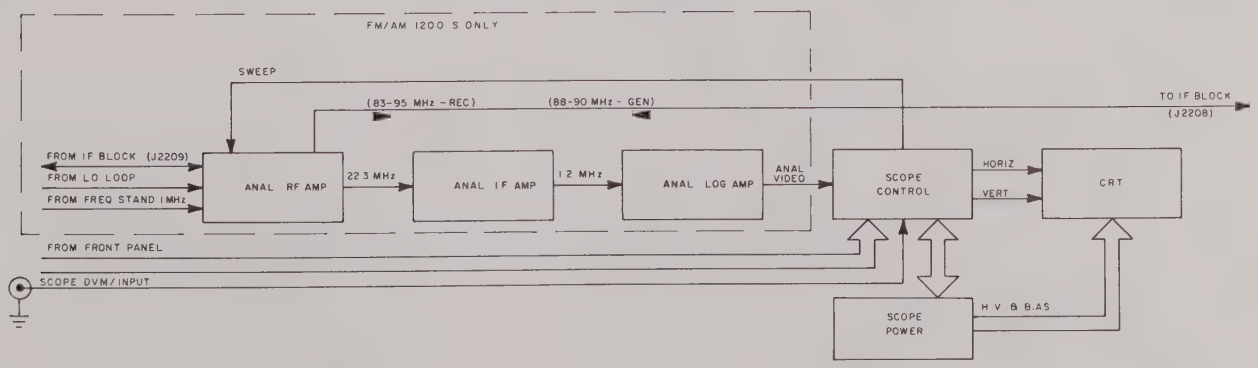


Figure 2-7 Oscilloscope/Spectrum Analyzer Functional Block Diagram

During analyzer operation, an 83-95 MHz signal is sent from the IF Block Assembly to the Analyzer RF Module where it is mixed with a sweep oscillator, centered at 111.3 MHz, to produce a 22.3 MHz signal which is fed to the Analyzer IF Module. The 22.3 MHz signal is mixed with a 33 MHz signal in the Analyzer IF Module, producing a 10.7 MHz signal. This signal is then filtered and mixed with a 9.5 MHz signal, producing a 1.2 MHz signal which is fed to the Analyzer Log Amp Module. In the Analyzer Log Amp Module, the amplitude of the 1.2 MHz signal is converted from a logarithmic value to a linear value, AM detected, and fed to the Scope Control PC Board for presentation on the Scope (CRT).

The Scope Power PC Board supplies all voltages necessary to bias the CRT. It also supplies the voltages for horizontal and vertical deflection to the Scope Control PC Board. The Scope Control PC Board receives signals from the Front Panel (Tones, Demod, Residual Distortion and SCOPE Connector). The signal selected for display is attenuated, sent to the vertical deflection amplifier and to a triggering circuit. Sweep speed is selected and sent to the horizontal deflection amplifier. The horizontal and vertical deflection signals are sent from the Scope Control PC Board to the CRT for display. The sweep signal is sent to the Analyzer RF Module to control the sweep oscillator.

2-4 DETAILED THEORY OF OPERATION

The following paragraphs discuss, in detail, the theory of operation for each module contained within the FM/AM-1200S/A. In addition to the detailed block diagrams, which are included with each topic, reference should be made to the apppropriate schematic or interconnect drawing contained in Section 7.

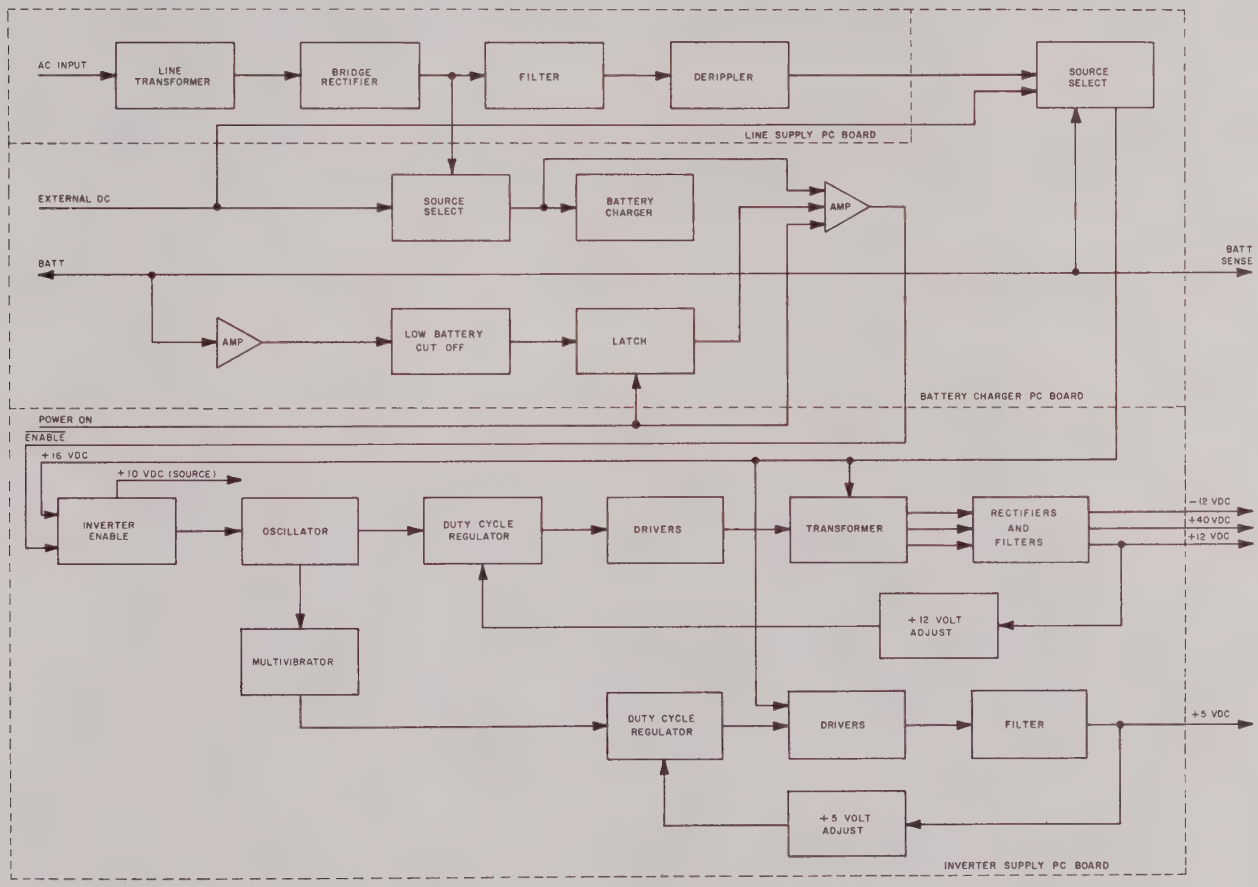


Figure 2-8 Power Supply Module Block Diagram

2-4-1 POWER SUPPLY MODULE

The Power Supply System consists of three major components:

Line Supply PC Board - which is an AC to DC converter containing a power transformer, bridge rectifier, filter and derippler.

Inverter Supply PC Board - which is a DC to DC converter utilizing a 50 kHz oscillator, duty cycle regulator, transformer and rectifier and filter circuits which furnish the ±12 VDC and +40 VDC, and a multivibrator, filter and voltage regulator for the +5V.

Battery Charger PC Board - which is mounted on the Power Supply Assembly, contains the battery charger circuit low-battery cutoff and selects the power source for the Inverter Supply PC Board.

A. Power Supply Line

1. For FM/AM-1200S Only

The AC Power Input Connector on the Rear Panel is connected to the Power Supply through J68001. Power is supplied to T68001 via F68001 and S68001. T68001 has two primary windings which are connected in parallel when 115 VAC is selected by S68001, or in series if 220 VAC is selected. The secondary winding of T68001 is connected to full wave rectifier BR68001, which is mounted on the Line Supply Bracket, which makes thermal contact with the Rear Panel heat sink. C68001 and C68002 filter and deripple the +16 VDC (nominal). Unregulated voltage from BR68001 is applied to the Battery Charger PC Board to operate inverter on/off switching. Derippled voltage from Q68001 is applied through the Battery Charger PC Board to the Inverter Supply PC Board.

2. For FM/AM-1200A Only

The AC Power Input Connector on the rear panel is connected to the Line Supply Assembly through J1701. Power is supplied to T1701 through F1701 and S1701. T1701 has two primary windings which are connected in parallel when 115 VAC is selected by S1701, or in series if 230 VAC is selected. The secondary winding of T1701 is connected to full wave rectifier, BR1701, which is mounted on the rear panel heat sink. C1701 and C1702 filter and deripple the +16 VDC (nominal). Unregulated voltage from BR1701 is applied to the Battery Charger PC Board for charging the battery, operating the inverter on/off switching. Derippled voltage from Q4601 is applied through the Battery Charger PC Board to the Inverter Supply PC Board.

B. Battery Charger PC Board

External DC power, filtered +16 VDC from the Line Supply Assembly and the battery are all independently applied to the Battery Charger PC Board through J1601. All three sources are compared by diodes CR1601, CR1602 and CR1603 respectively, and the highest voltage source (Ext. DC or AC) is applied through fuse F1601 to the Inverter Supply PC Board. The external DC and unfiltered +16 VDC from the Line Supply Assembly are applied through CR1605 and CR1606 to the battery charger circuit and inverter enable circuit.

The battery charger circuit consists of adjustable regulator U1601, R1601 through R1604 and C1601. R1602, R1603 and trimpot R1604 form a voltage divider to adjust the output voltage to 14.4 VDC and R1601 provides a minimum load to regulator U1601. Anytime AC or DC power in excess of the battery level is applied to the test set, the battery charger circuit charges the battery. The position of the PWR/OFF/BATT Switch does not affect the charging circuit.

Q1601, Q1602, Q1604 and associated components make up the inverter enable circuit. When AC or DC power is applied, and the PWR/OFF/BATT Switch is in the OFF position, Q1601 does not conduct. However, with the PWR/OFF/BATT Switch in the PWR position, Q1601 conducts, turning on Q1602 to pull down on the inverter enable line, causing Q1501 on the Inverter Supply PC Board to conduct. If external AC power is interrupted, diodes CR1602 and CR1603 switch the inverter supply to the battery, when the charge on capacitors C1701 and C1702 in the Line Supply Assembly drop below the battery voltage. As the voltage drops, the base to emitter voltage difference on Q1601 decreases until it is shut off. This, in turn, shuts off Q1604, driving the voltage to the base of Q1601 higher to prevent oscillation.

The battery enable circuit consists of flip-flop U1602B and related components. When the PWR/OFF/BATT Switch is pressed in the PWR position, C1604 is allowed to charge through R1610, clocking U1602B to high Q, which turns on Q1602 enabling the Inverter Supply PC Board.

A low battery cutoff circuit stops battery operation if the battery voltage drops below approximately +11.4 VDC. +12 VDC is applied to the emitter of transistor Q1603 while the battery voltage is applied to its base. When the battery voltage drops to approximately 11.4 VDC, Q1603 turns on, applying +12 VDC to the SET pin of U1603. This sets the timer to terminal count, providing a high output to reset U1602B. Q of U1602B then goes low, terminating operation.

C. Inverter Supply PC Board

The Inverter Supply PC Board contains a duty cycle regulator, transformer and rectifier circuits. These produce the regulated +12 VDC, +40 VDC and -12 VDC which are distributed throughout the test set. The inverter supply voltage from the Battery Charger PC Board is +12 VDC to +30 VDC, depending upon the source.

When the test set is turned on, the low enable line pulls down on the base of Q1501. Q1501 conducts, allowing +10 VDC, set by Zener diode CR1504, to supply power to op amps U1501, U1502, U1503, U1505, U1506 and U1507 and through a voltage divider using R1505 and R1506, to the non-inverting input of U1501. Simultaneously, Q1502 is turned off, allowing U1501 to produce a sawtooth output at approximately 45 kHz which is applied to the non-inverting input of U1502.

Zener diode CR1506 applies a 6.9 VDC reference to the inverting input of U1503 which is configured as an integrator. A sample voltage from the +12 VDC secondary winding of T1501, after being rectified by CR1511 and filtered by L1502 and C1509, passes through a voltage divider, consisting of R1518, R1519 and trimpot R1520 for calibration before it is applied to the non-inverting input of U1503. As power is applied to the primary winding of T1501, C1509 becomes charged through CR1511. U1503 compares the voltage at C1509 with the reference set by CR1506 to produce a reference level for U1502.

U1502 compares the oscillator output level with the reference level from U1503 to produce a pulsed output whose duty cycle decreases as the reference level increases. R1510 sets a minimum reference level to maintain a maximum duty cycle of 50%. The high output from U1502 turns on Q1503, applying voltage to the gate of Q1505. Q1505 conducts, pulling current through the primary winding of T1501. When U1502 output goes low, Q1503 is turned off, and Q1504 is turned on. This then turns off Q1505. The result of this action is to build, then collapse the magnetic field from the primary winding of T1501 proportional to the duty cycle of U1502.

The power induced by the primary winding of T1501 into the secondary windings is proportional to the amount the magnetic field has developed during the duty cycle of U1502. Because the test set loads on the +40 VDC and -12 VDC supplies, these two track the +12 VDC supply. As the load on the +12 VDC supply varies (e.g., when using the Oscilloscope or Spectrum Analyzer), integrator U1503 detects the effect on the +12 VDC supply line and raises or lowers the duty cycle reference level at U1502 accordingly. Increasing the load on the +12 VDC supply increases the duty cycle, which increases the transfer of power from the primary winding of T1501 to the secondary windings.

The AC voltages from the secondary windings are half-wave rectified by individual diodes. The +40 VDC supply is Resistance-capacitance (R-C) filtered; the other supplies are Inductance (L-C) filtered.

The +5 VDC is produced by toggling Q1508 and Q1510, which charges C1514. L1507 dampens the spikes produced as Q1508 and Q1510 are turned on and off. CR1513 is a damper diode which suppresses spikes induced by L1507. The duty cycle is controlled by the interaction of multivibrator U1505, comparator U1506, integrator U1507, and transistors Q1506, Q1507, and Q1509.

A ramp voltage is generated at pin 3 of U1506 by charging C1513 through R1524. When pin 10 of U1505 is low, C1513 is disharged. When pin 10 goes high, C1513 is charged, creating a ramp voltage. U1505 is triggered by the 50 kHz oscillator, U1501, such that the +5V regulator and the +12V regulator alternately pull on the supply line. By alternating in this manner, ripple current is decreased on the supply line.

Integrator U1507 compares the charge on C1514 with a fixed DC reference set by CR1506, to produce a reference level for comparator U1506. U1506 sets the duty cycle for the +5V regulator. When Q1509 is off, FET's Q1508 and Q1510 are held off by Q1506. When Q1509 is on, the FET's are turned on through Q1507.

2-4-2 PROCESSOR PC BOARD (FM/AM-1200S THRU SER NO 7030)

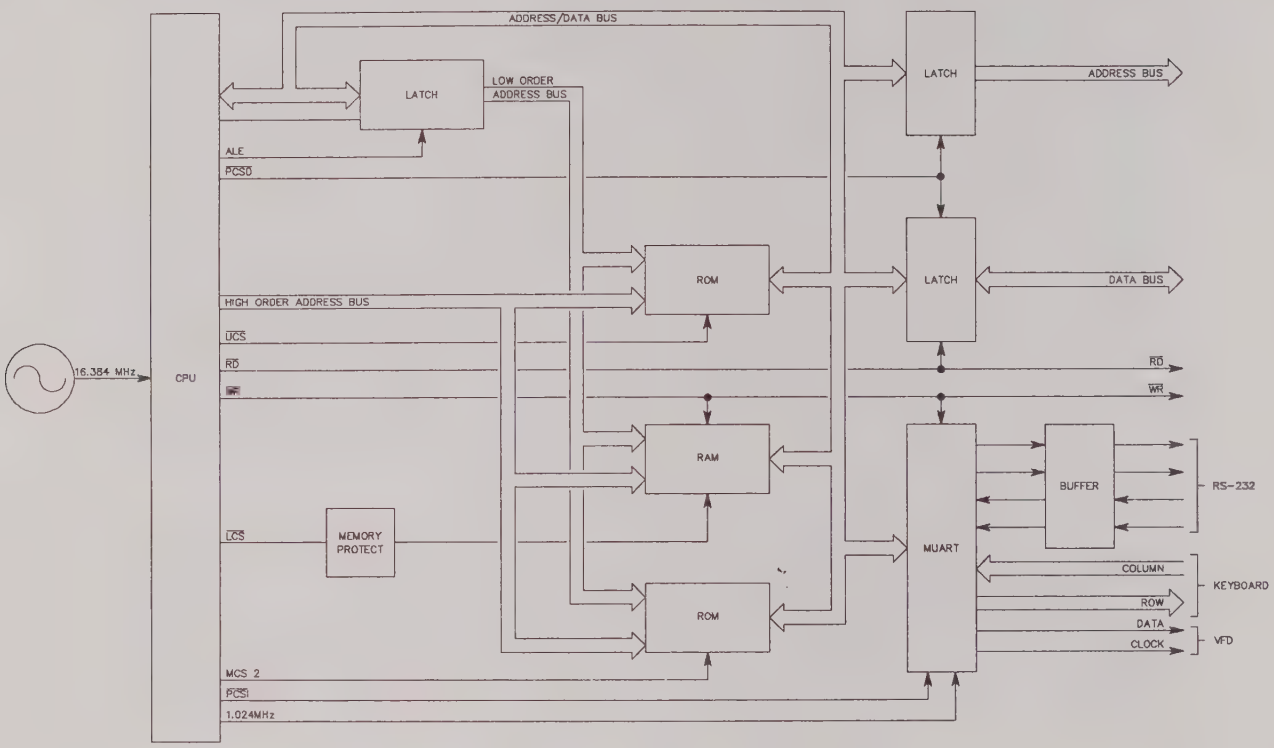


Figure 2-9 Processor PC Board Block Diagram

The Processor PC Board contains an 80188 microprocessor, U67001, system ROM, U67003 and U67004, RAM, U67005, MUART (Multifunction Universal Asynchronous Receiver Transmitter), U67008, latch, U67007, Octal Transceiver, U67006, RS-232c Transceiver, U67009, buffer, U67002, and associated components.

The microprocessor is an eight-bit processor with a 16-bit internal architecture and onboard peripherals (e.g., onboard timers). The address/data bus is latched by U67002 to provide low order addresses to the onboard memory, latched by U67007 to address peripherals on the Interface PC Board, and used directly to transfer data between memory, the MUART, Data Transceiver U67006 and the microprocessor. All chip select lines originate in the CPU.

Y67001 is a 16.384 MHz crystal for the on-chip oscillator in U67001. A 1.024 MHz clock (timer 0) is sent to the MUART as a timebase for the timers and UART functions. ROMs U67003 and U67004 contain all the main operating functions such as RF controls, tone control and tone sequences.

The memory protect circuit, consisting of Q67001 thru Q67004, and associated components is a voltage comparator which detects when power is turned off. A backup +3V Lithium Battery (BT67001), which is part of the memory protect circuit, is placed in line with RAM U67005, so when power is removed, the memory contents in RAM will be retained. This is accomplished by placing +3 VDC on pin 28 of U67005.

In the keyboard circuit, bits 0 thru 3 of Port 2 from U67008 are the row lines for the keyboard and are driven low. The column lines for the keyboard are held high by +5 VDC through RN67003 and monitored by NAND/AND gate U67010. When a button on the keyboard is pressed, one of the column lines will be driven low to be detected by U67010, causing it to change states and generating an interrupt. During this interrupt routine, the row lines are driven low one at a time. As each row line is driven low, the column lines are read by the CPU. After all four row lines have been strobed and all column lines read, the CPU determines which key was pressed and enters a routine for that key. If more than one key is pressed, no action is taken by the CPU.

The MUART also functions as a parallel/serial converter to transfer data between the CPU and RS-232c Interface. U67009, a dual RS-232c transmitter/receiver, contains level translators which convert TTL levels to ±9 VDC. The MUART is also used to send serial data and clock to the VFD Controller.

2-4-2a PROCESSOR PC BOARD (FM/AM-1200S, SER NO 7031 THRU 8300; FM/AM-1200A SER NO THRU 1706)

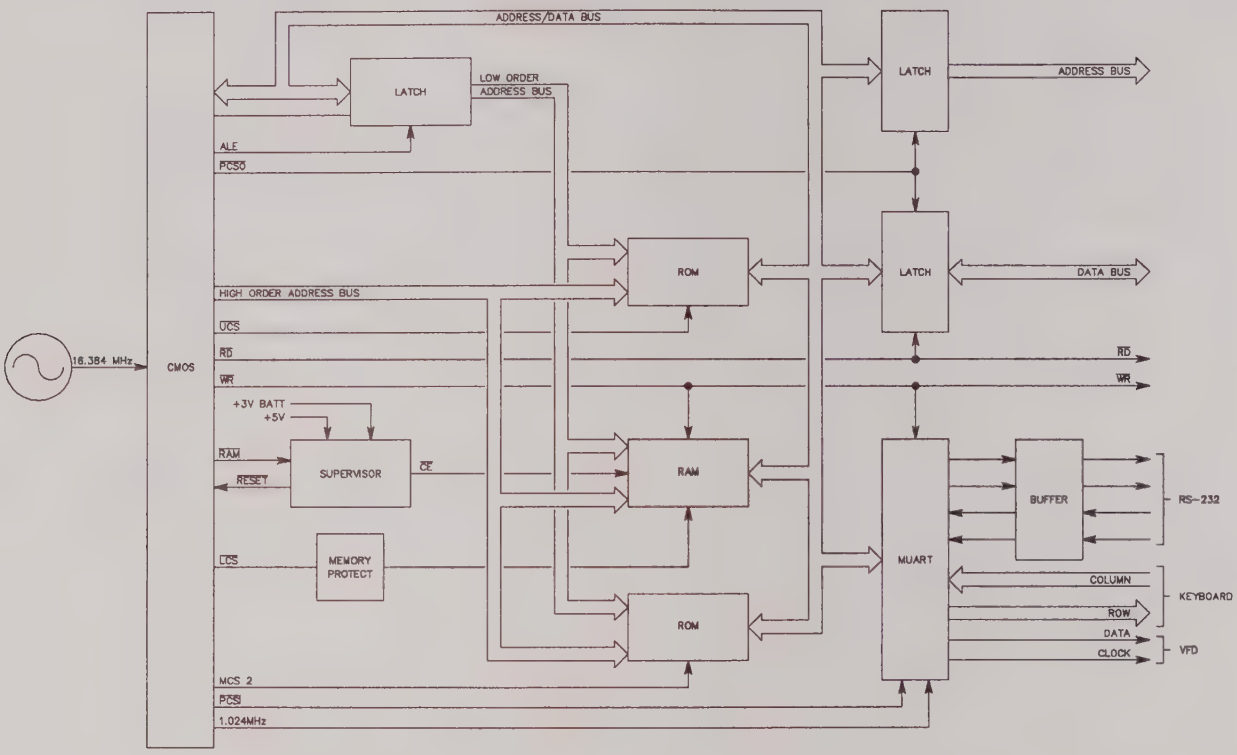


Figure 2-9a Processor PC Board Block Diagram

The Processor PC Board contains an 80C188 CMOS, U67001, system ROM, U67003 and U67004, RAM, U67005, MUART (Multifunction Universal Asynchronous Receiver Transmitter), U67008, latch, U67007, Octal Transceiver, U67006, RS-232c Transceiver, U67009, buffer, U67002, and associated components.

The CMOS is an eight-bit processor with a 16-bit internal architecture and onboard peripherals (e.g., onboard timers). The address/data bus is latched by U67002 to provide low order addresses to the onboard memory, latched by U67007 to address peripherals on the Interface PC Board, and used directly to transfer data between memory, the MUART, Data Transceiver U67006 and the microprocessor. All chip select lines originate in the CPU.

Y67001 is a 16.384 MHz crystal for the on-chip oscillator in U67001. A 1.024 MHz clock (timer 0) is sent to the MUART as a timebase for the timers and UART functions. ROMs U67003 and U67004 contain all the main operating functions such as RF controls, tone control and tone sequences.

The memory protect circuit, Q67001, Q67002, Q67005, and associated components, is a voltage comparator which detects when power is turned off. A backup +3V Lithium Battery (BT67001), which is part of the memory protect circuit, is placed in line with RAM U67005, so when power is removed, the memory contents in RAM are retained. This is accomplished by placing +3 VDC on pin 28 of U67005.

In the keyboard circuit, bits 0 thru 3 of Port 2 from U67008 are the row lines for the keyboard and are driven low. The column lines for the keyboard are held high by +5 VDC through RN67003 and monitored by NAND/AND gate U67010. When a button on the keyboard is pressed, one of the column lines will be driven low to be detected by U67010, causing it to change states and generating an interrupt. During this interrupt routine, the row lines are driven low one at a time. As each row line is driven low, the column lines are read by the CPU. After all four row lines have been strobed and all column lines read, the CPU determines which key was pressed and enters a routine for that key. If more than one key is pressed, no action is taken by the CPU.

The MUART also functions as a parallel/serial converter to transfer data between the CPU and the RS-232c. U67009, a dual RS-232c transmitter/receiver, contains level translators which convert TTL levels to ±9 VDC. The MUART is also used to send serial data and clock to the VFD Controller.

2-4-2b PROCESSOR PC BOARD (FM/AM-1200S FROM SER NO 8301 AND ON; FM/AM-1200A FROM SER NO 1707 AND ON)

The Processor PC Boards beginning with the serial numbers indicated above includes a MAX691 Supervisory Chip (U67011). This chip selects between +5 VDC from the power supply and approximately +3 VDC from battery on PC Board to supply power to RAM. It is also used to reset the unit, provide write protect for RAM at power up, and control the CMOS 80C188 processor.

2-4-3 INTERFACE PC BOARD

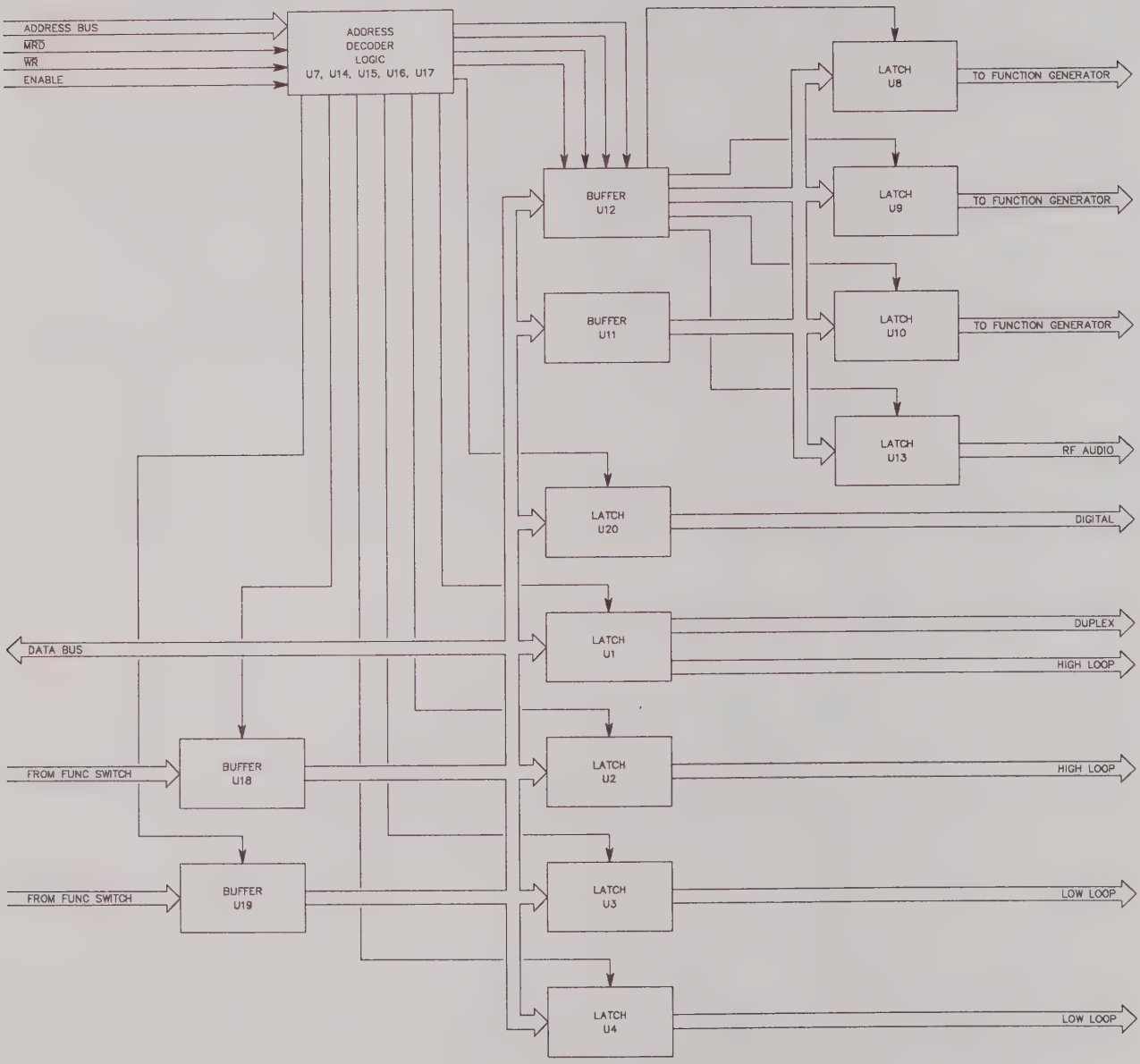


Figure 2-10 Interface PC Board Block Diagram

A. All Units

The Interface PC Board latches all data from the Processor PC Board to the following: Function Generator, High Loop Assembly, Low Loop Assembly, Receive Audio PC Board, Digital Module, and the Duplex Module. Data from the Function Switch PC Board is buffered on the Interface PC Board before being sent to the Processor.

The address decoder (U1007, U1014, U1015, U1016 and U1017) decodes the 8-bit address bus and the 3-control lines (MRD, WR, Enable) to set the latches or read the buffers.

B. FM/AM-1200S Only

The FM/AM-1200S includes latches U1023 and U1024, used to set up Q and Center Frequencies on the Programmable Filter (U1021). U1023 also latches information from the Processor to select filter types on U1021 using analog filter switches U1020A (low-pass), U1020B (bandpass), U1020C (high-pass), or for all filters. U1024 can also latch information from the Processor to enable filtering via U1021.

C. Cellular Option (FM/AM-1200S Only)

When the FM/AM-1200S includes Cellular mode, audio (SAT and ST) is amplified per U1019A before it is bandpass-filtered (U1021A) via a filter switch (U1020A). Audio is filtered again through a low-pass filter (R1006, R1007, R1008, C1016 and C1017) before it is passed through the Signal Routing Switch (U1022A and U1022B). Audio is then routed back to the Receive Audio PC Board (i.e., Demod Audio and Meter circuits). If cellular mode is turned off, the programmable filter is bypassed.

The oscillator circuit includes a 10 MHz Crystal Oscillator (U1014D), a buffer (U1014C) and two divide-by-ten circuits, which are used to produce 100 kHz and 1 MHz clocked signals. The clocked signals are input to U1022C, where the clock rate from 1 MHz to 100 kHz is selected as input to a Programmable Filter. The Filter Range is from 5 kHz to 20 kHz (1 MHz clock) or from 500 Hz to 2 kHz (100 kHz clock).

R1002 is adjusted to maintain unity gain when the cellular option is active. Input is AUDIO IN from the Receive Audio PC Board (pins 2 and 9 from J61003). Output is through Demod Audio Out and Meter Audio Out (Pins 4 and 7 of J61003) to the Receive Audio PC Board.

2-4-4 DVM I/O PC BOARD

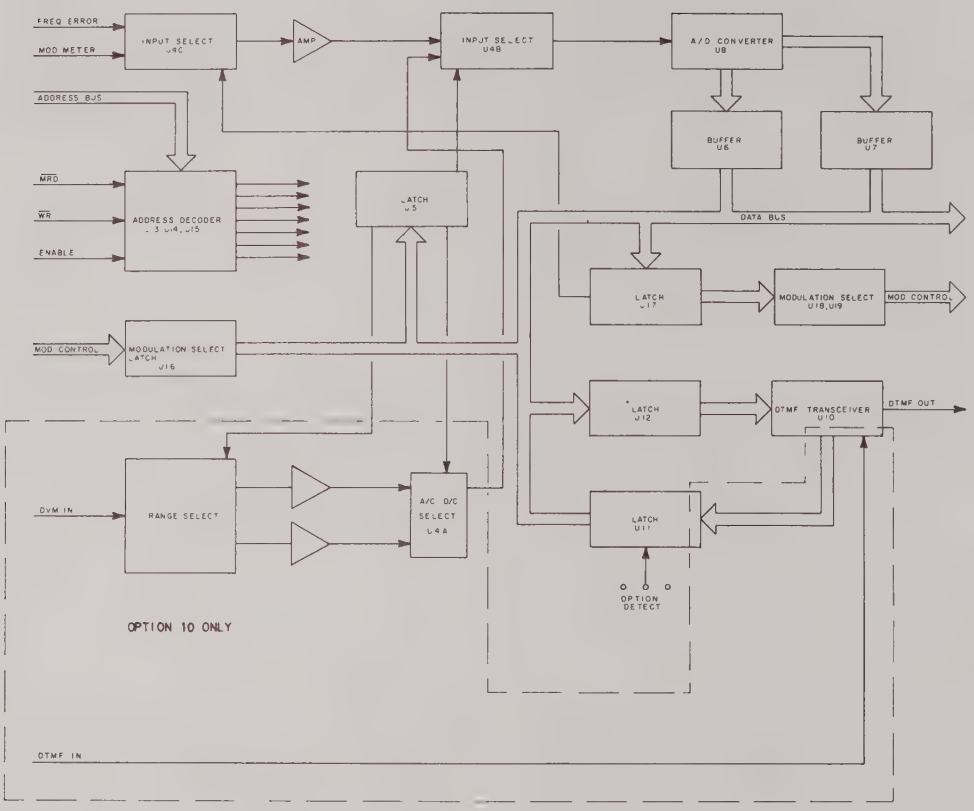


Figure 2-11 DVM I/O PC Board Block Diagram

A. Standard DVM I/O PC Board (FM/AM-1200S Only)

Frequency error and modulation monitor signals are routed to the Meter Input Select Chip (U3004C). Signal selection is made when the Address Decoder (U3013, U3014 and U3015) clocks the DØ data bit through latch U3017. If DØ is low, frequency error is switched to op amp U3009. If DØ is high, modulation monitor is switched to the op amp.

Signals reflecting the setting of the MODULATION Select Control on the front panel are latched through U3016 to the processor. Signals controlling the setting of the MODULATION Select Control (as in RS-232c operation) are latched through U3017, U3018 and U3019 and sent to the 10.7 MHz Gen/Rec Module, the Receive Audio Module, and the Generate Audio Module.

When the processor selects a DTMF encoding operation, the necessary bits will be latched into U3012 and sent to U3010, a DTMF transceiver. From the transceiver, the encoded DTMF is sent to the Generate Audio module for output.

B. Optional DVM I/O PC BOARD (Option 10)

When the optional DVM I/O PC Board is installed, the same circuitry is present as described for the standard DVM I/O PC Board, plus there is also an auto-ranging voltmeter circuit and a DTMF decoder circuit.

J3003 is an input from the SCOPE/DVM Connector on the front panel. RN3001 is a voltage divider network, the output of which is selected through relays K3001, K3002 and K3003. The processor latches the relay control lines through U3005 and automatically selects the necessary control line.

Both the AC and DC voltages are read, with the AC voltage being presented to pin 5 of U3004A and the DC voltage being presented to pin 3 of U3004A. The processor, through latch U3005, selects which voltage is to be digitized, depending on user operation of the keyboard (+/- key)(i.e., D3 is set high or low). The selected voltage is switched through U3004B when the user selects DVM operation. When D3 is high, the selected signal from the op amp is sent to the A/D converter (U3008) to be digitized. The digitized signal is then latched through U3006 and U3007 and sent to the Processor PC Board to be displayed on the VFD.

The DTMF decoder circuit uses U3010, the DTMF transceiver, to decode the demod audio received from the Receive Audio Module. The decoded data is latched into U3011 to be sent to the processor and then to be displayed on the VFD.

C. Cellular Option (FM/AM-1200S Only)

If the cellular option is active, the XMIT DET (transmit detect) line is added to the DVM I/O PC Board, with input from the Generate Audio PC Board. When RF Power is applied to the T/R Connector, pin 14 of U3020 goes high, causing U3018 to switch its output from pin 6 (15 kHz) to pin 9 (200 kHz). If cellular is not selected, this function is performed with the Modulation Select Control. U3020 is a dual 4-input multiplexer chip.

2-4-5 FREQUENCY STANDARD PC BOARD

The Frequency Standard uses a voltage controlled, Temperature Compensated Crystal Oscillator (TCXO) to furnish a constant 10 MHz reference. When desired, an external 10 MHz reference signal can be used by connecting the signal source to the External Reference Connector on the rear panel of the test set. A bi-quinary ripple counter divides the 10 MHz signal to a 500 kHz signal which is fed to the High Loop Module, and to a 1 MHz signal which is fed to the Digital Module and, on the FM/AM-1200S, to the Spectrum Analyzer RF Module.

A level detect circuit determines when an external 10 MHz reference signal of sufficient amplitude is present on the External Reference Connector and responds by deactivating the TCXO and couples the external 10 MHz reference signal to the frequency divider.

The internal 10 MHz reference signal produced by the TCXO is also fed back to the rear panel External Reference Connector, which can be used during calibration.

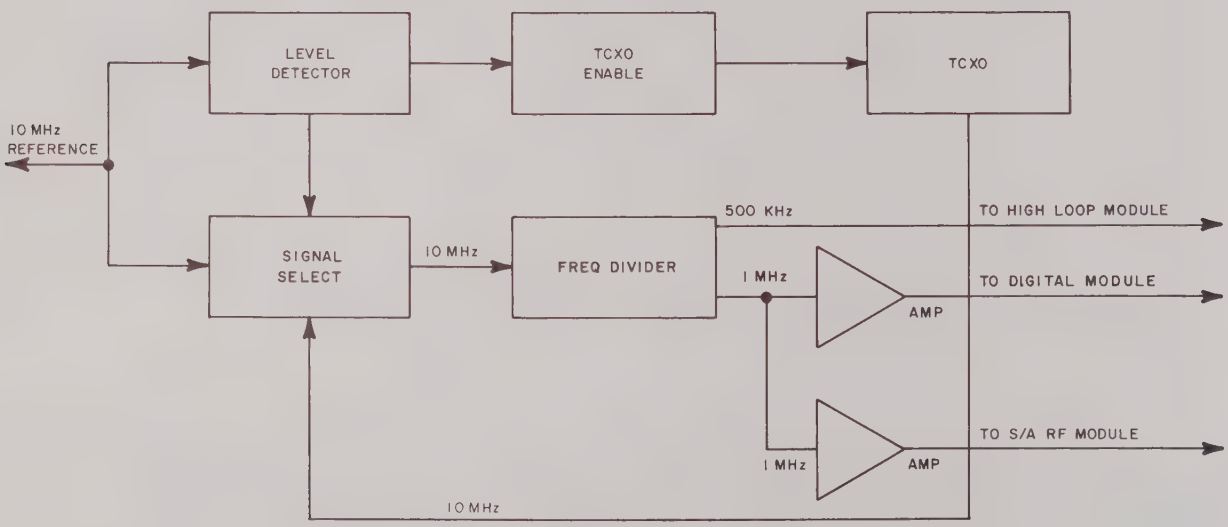


Figure 2-12 Frequency Standard PC Board Block Diagram

When an external 10 MHz reference signal exceeding 5 Vp-p is applied through the External Reference Connector to NAND gate U2802, a level detector, consisting of op amp U2801 and associated components, produces a constant high, turning off Q2801 and interrupting power to the TCXO. The high output of U2801 is also fed to U2802, passing the external 10 MHz reference signal to the frequency divider circuit.

The internal 10 MHz reference signal from the TCXO is applied to pin 9 of NAND gate U2802. The gated output from U2802, pin 6 is fed to U2803 and through R2807 to the External Reference Connector.

The level detector in the signal select circuit controls the base voltage to transistor Q2801, which, in turn, controls the +12 VDC to the TCXO. R3501 on the front panel allows fine adjustment of the operating frequency to calibrate the TCXO. The TCXO coarse adjustment is within the TCXO Assembly mounted on the Frequency Standard PC Board.

The frequency divider circuit consists of dual counter U2803, two buffer transistors, Q2802 and Q2803, and associated components. The 10 MHz input is divided by 10 in the first counter and applied to the base of both transistors. Q2802 supplies a 1 MHz reference to the Digital Module through P402. Q2803 supplies 1 MHz to the Spectrum Analyzer (in the FM/AM-1200S) through P404. The output of the first counter is further divided to 500 kHz and sent to the High Loop Module through P4001.

2-4-6 DIGITAL MODULE

The Digital Module contains two PC Boards, the Digital Reference PC Board and the Digital Counter PC Board. The Digital Reference PC Board receives a 1 MHz signal from the Frequency Standard and divides it down for use throughout the FM/AM-1200S/A.

SIGNAL	DESTINATION	USE
20 kHz	Duplex Module	REF Freq
10 kHz	Digital Counter PCB	Time Base*
1 kHz	Digital Counter PCB	Time Base*
1 kHz	Digital REF	REF Freq for 21.4 MHz OSC
1 kHz Sine	Front Panel	Fixed Tone
100 Hz	Low Loop Assy	REF Freq
100 Hz	Digital Counter	Time Base*
10 Hz	Digital Counter	Time Base*

* These signals are used in the Digital Counter PC Board for FREQ Error Measurements.

The Digital Reference PC Board also contains a 1 kHz sine wave filter, phase-lock loop for the 21.4 MHz oscillator on the 10.7 MHz Gen/Rec Module, and tone multipliers for audio error measurements. The Digital Counter PC Board contains all logic and counters for FREQ Error Measurements.

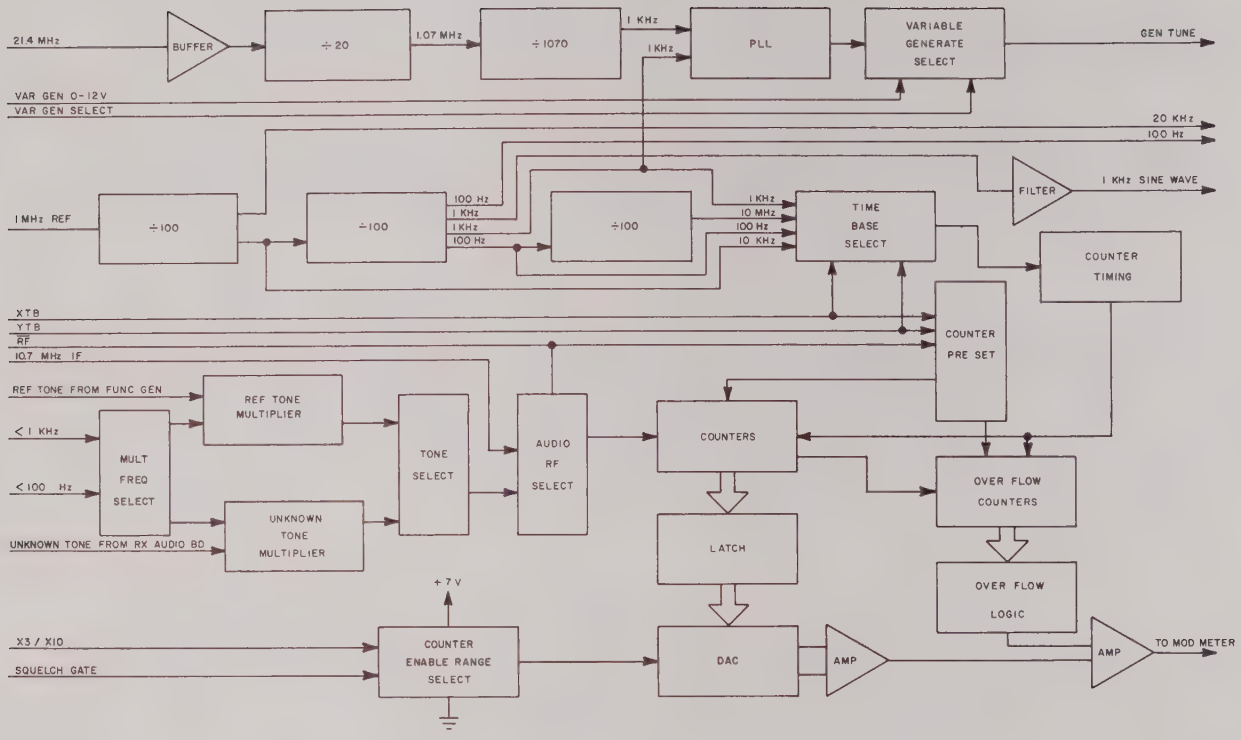


Figure 2-13 Digital Module Block Diagram

A. Dividers

The 1 MHz signal enters the module at J4503 and is divided by U4505 to produce 20 kHz (duplex REF Freq) and 10 kHz which is fed to U4506. U4506 divides the 10 kHz down to 1 kHz and 100 Hz. The 100 Hz is fed to U4507 where it is divided down to 10 Hz.

The 10 kHz, 1 kHz, 100 Hz, and 10 Hz are fed to multiplexer U4508 for time base selection for the digital counter. Selection of the time base is made by two control lines (XTB, YTB) from the Interface PC Board.

YTB	XTB	TIME BASE
LOW	LOW	10 Hz
LOW	HIGH	100 Hz
HIGH	LOW	1 kHz
HIGH	HIGH	10 kHz

B. PLL (Phase-Lock Loop)

The 21.4 MHz signal from the 10.7 MHz Generate/Receive Module enters the Digital Module at J4502. First the signal is inverted by Q4501, then divided by 20 in U4501. This 1.07 MHz signal is fed to U4502 and divided by 1070 to produce a 1 kHz signal. This 1 kHz signal is fed to U4503, a phase-lock loop, and compared with the 1 kHz REF signal from divider U4506 to produce a steering voltage for the 21.4 MHz Oscillator on the 10.7 MHz Gen/Rec Module. This steering voltage is fed to the analog multiplexer circuit, U4504. A variable DC voltage is also sent to U4504 from the front panel GEN/LOCK Control. When the variable GEN/LOCK Control is in the detent position, the VAR GEN enable line is low, which selects the steering voltage from the PLL chip, U4503, and passes this signal to the Gen Tune line. When the variable GEN/LOCK Control is out of detent, the VAR GEN enable line is high, which selects the DC voltage from the Front Panel Variable GEN/LOCK Control and passes it to the Gen Tune Line.

C. Tone Multipliers

Because the audio frequencies are too low for counting to the required accuracy within the available time base periods, both the reference and unknown frequencies are multiplied by a factor of 100 by separate phase-locked loop circuits. The incoming tones are applied to the reference signal pin of the appropriate PLL (Phase-Locked Loop) (U4510 for the unknown, U4512 for the reference). The VCO output from the PLL is divided by 100 by a counter (U4511 for the unknown, U4513 for the reference) and applied to the comparator pin of the PLL. The output of each loop is then applied to U4518. To inhibit the loop functions during the RF mode, Q4502 allows a +12V potential to inhibit operation of U4510 and U4512. When the audio mode is selected, the high mode select signal turns on Q4502, grounding the +12 potential, allowing U4510 and U4512 to operate.

D. Sine Wave Filter

A 1 kHz square wave signal from the time base divider is filtered by a three-stage active filter consisting of op amps U4514 and U4515, and related components. The output of the filter is a 6 Vp-p sine wave supplied to the Generate Audio Module, through the front panel select switch and tone control, as the fixed tone signal.

E. Preset Logic

Quad NOR gate U4414, quad NAND gate U4416 and hex inverter U4417 form a logic network to preset the counter system for a 1, 10 or 100 multiplier, according to the position of the FREQ ERROR Meter Control ($\overline{X3}$/X10 selection is in the meter driver circuit). These presets are loaded into the counters during the 15 µs output pulse from U4413B (for audio frequencies, the preset count is zero).

F. Signal Select Circuit

Multiplexer U4401A couples the IF carrier from the 10.7 MHz Gen/Rec Module directly to the counter system when an RF position is selected on the FREQ ERROR Meter Range Control. When an audio position is selected, the Q output of U4412B first selects the reference frequency from the Variable Tone Generator, then the unknown audio frequency from the Receive Audio Module. The selected signal is then coupled by U4401A to the counter circuit.

G. Counter Timing Circuit

The timing circuit consists of decade counter U4411, dual D-type flip-flop U4412, multiplexer U4401B, inverter U4421E and dual one-shot multivibrator, U4413. The input to the timing circuit is the selected time base frequency from multiplexer U4508. One output operates audio select multiplexer U4413 in the signal select circuit; other outputs control the counter circuit.

U4411 receives and counts the time base pulses. Starting with a high Q state of U4412A, when pin 2 of U4411 (representing binary 8) goes high, U4411 clocks U4412A to low Q. This produces a high output from U4421E, which clocks U4412B, and, simultaneously, provides a spike through C4413. The spike preloads a count of seven into U4411, overriding its count and pulling pin 2 back low. The next time base pulse causes pin 2 to again go high, clocking U4412A back to high Q. Pin 2 stays high for one more count, then goes low for the next eight counts. With the following pulse, the cycle repeats.

The high Q from U4412A inhibits the counter system for one time base period and is available to U4401B. When the $\overline{Q}$ output of U4412B is high, it is also available to U4401B. With the FREQ ERROR Meter Range Control in an RF position, U4401B selects the $\overline{Q}$ from U4412A; in an AUDIO position, it selects the $\overline{Q}$ from U4412B. The leading edge of the signal, as Q goes high, clocks U4413A, producing, as its output, a 15 µs low Q. As U4413A output $\overline{Q}$ returns high, it is applied to the counter circuit latch components and it clocks U4413B. U4413B now produces two 15 µs pulses—a high $\overline{Q}$ and a low $\overline{Q}$. These signals reset the counter system and U4412B. In the audio mode, U4412B has

already been clocked to high Q; however, in RF mode, it has just been clocked to a high $\overline{Q}$, and is now, just a few microseconds later, clocked back to high $\overline{Q}$. The counter system counts upward when U4412B Q is low and downward when Q is high. This allows the counters to count upward on the audio reference frequency while Q is low, then downward on the unknown audio frequency while Q is high (while in the audio mode), but allows them, when in RF mode, to only count upward.

H. Counter Circuit

The counter circuit contains binary counters U4402 through U4406, dual D-type flip-flop U4407, latch U4408 and related gates and inverters. U4402 and U4403, the two least significant digit counters, furnish the meter deflection count, while U4404, U4405 and U4406 are overrange counters. If any terminal count in the latter is not zero, the meter will be pegged.

The selected frequency is applied to U4402 through U4401A. During loading, $\overline{Q}$ of U4412A and U4412B are high, which inhibit U4402 and U4403. When U4412A is clocked by U4411, successively clocking U4412B and U4422 is clocked by the 10.7 MHz IF, the counters are allowed to count upward from preset values for a period of 10 time-base pulses. The binary counts from U4402 and U4403 are applied to latch U4408 to drive the meter. Any non-zero count from U4404, U4405 or U4406 is applied through gates U4410, U4415B, U4420C and U4420D to either U4407A (if U4406, Pin 2 is low) or U4407B (if U4406, Pin 2 is high).

When the tenth time base pulse arrives, U4412A is clocked to a high Q state. In RF mode, this inhibits the counter chain and initiates the end-of-count process. In audio mode, it inhibits the counter chain while U4412B sets the counters to count down and changes the signal from the reference to the unknown frequency. The counters then count downward for the next ten time base pulses, then U4412A is again clocked to a high $\overline{Q}$ state. Now the end-of-count process is initiated for the audio mode.

The end-of-count process starts when U4413A is clocked by either U4412A or U4412B, and its $\overline{Q}$ output goes low for 15 µs. As $\overline{Q}$ goes high, U4408 is clocked, latching the count from U4402 and U4403 to DAC U4409. Simultaneously, U4407A and U4407B are clocked, and if any output from U4404, U4405 or U4406 is high, resulting from a frequency error that exceeds meter capacity, U4407A or U4407B will apply a high potential to the meter driver circuit. As $\overline{Q}$ of U4413A returns high, it also clocks U4413B, resulting in a 15 µs pulse output in which Q goes high and $\overline{Q}$ goes low to preload the counters from the logic network. Exclusive NOR gates U4418C and U4418, and inverters U4421C and U4421D prevent unwanted clocking of U4403, U4404, U4405 and U4406 during loading. With the next time base pulse, U4412A is clocked to high Q, low $\overline{Q}$, and the counting process repeats.

Inverter U4421A applies a high to the clear-direct pins of U4407A and U4407B when the RF signal is insufficient to break squelch, which prevents any possibility of overrange meter deflection.

I. Meter Driver Circuit

The meter driver circuit contains 8-bit DAC U4409, dual op amp U4419, multiplexers U4504A and U4504C, and associated components.

When U4408 is clocked, it transfers the final count from U4402 and U4403 to the DAC. The two current outputs from U4409 are applied to op amp U4419, which is configured as a current-to-voltage converter. Trimpot R4407 allows calibrating the input level to U4419 to produce a zero output voltage when a count of 128 is applied to U4409. The output voltage of U4419 is positive or negative, depending upon which output from U4409 draws the higher current. U4419 inverts the output of U4409 and provides a 10:1 gain to drive the meter and provide for the digital readout. When the frequency error exceeds meter capacity, either U4407A or U4407B applies a high to the corresponding input of U4419B to peg the meter.

The reference voltage for the DAC is established by R4508 and trimpot R4510 for the X10 scale of the Frequency Error Meter, and by trimpot R4509 for the $\overline{X3}$ scale. Multiplexer U4504B selects the scale, depending upon the setting of the FREQ ERROR Meter Range Control. When the carrier signal level is insufficient to break squelch, multiplexer U4504C couples the input of U4504B to ground. When the signal breaks squelch, U4504C then applies +6.9V to U4504B.

2-4-7 FUNCTION GENERATOR PC BOARD

The Function Generator produces six different tone configurations (sine wave, ramp, triangle, square, DCS and pulse), a separate square wave for audio error measurements, and three separate lines which indicate generated tone range (<100 Hz, <400 Hz and <1 kHz).

The tone output is fed to the front panel VAR Tone Selector Switch for use as either a modulation source on the Generate Audio PC Board or to the internal speaker for aural monitoring. The <100 Hz and <1 kHz signals are fed to the Digital Module, and the <400 Hz signal is fed to the Receive Audio PC Board.

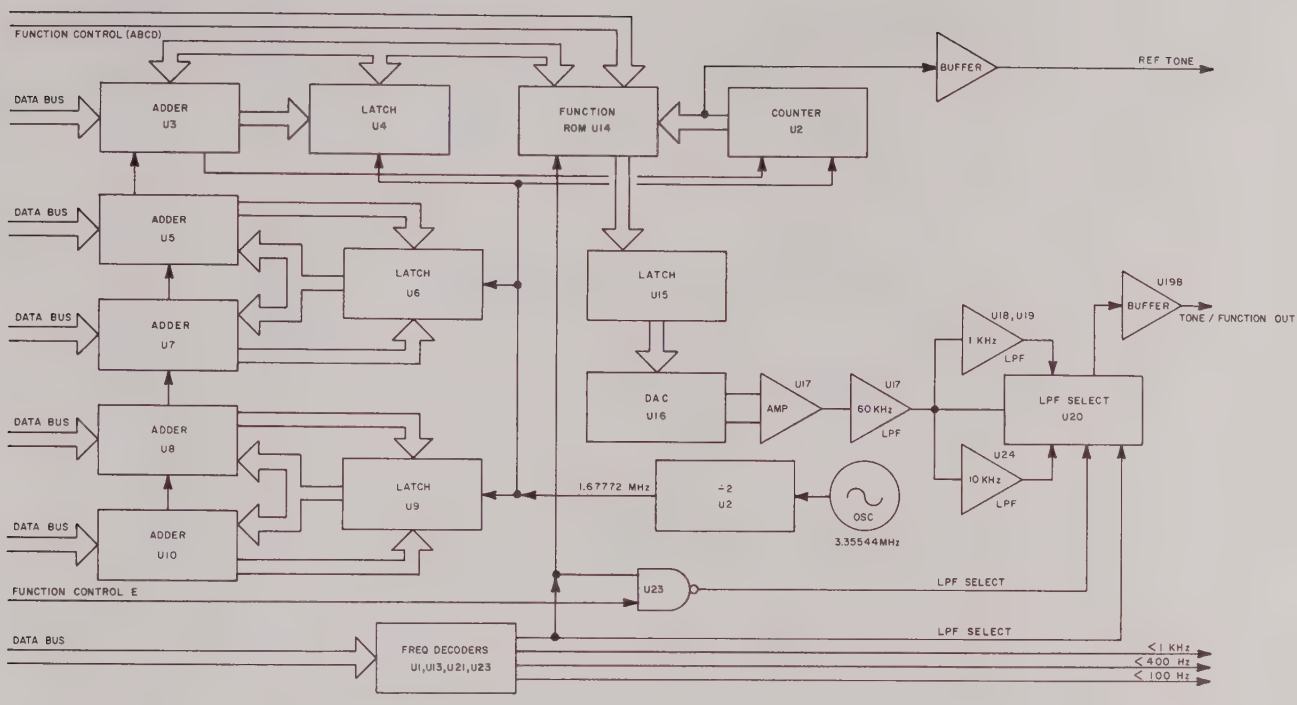


Figure 2-14 Function Generator PC Board Block Diagram

A. Oscillator Circuit

The reference oscillator contains 3.35544 MHz crystal Y3101, Q3102, trimcap C3110, and associated components. Q3101 buffers the signal, which then clocks binary counter U3102A. U3102A divides the frequency to 1.67772 MHz to clock the latches in the adder system.

B. Adder system

The adder system contains 4-bit binary adders U3103, U3105, U3107, U3108 and U3110, latches U3104, U3106 and U3109, and counter U3102B. One counter and one-half of a latch form a loop which combines data from the CPU and any carry-in from another adder with the output data from the latch. The sum becomes the input to the latch. When the latch is clocked by the oscillator, the sum becomes a new latch output, which creates a new sum for the adder. The carry-out is chained to the next adder, and the process is continued until the carry-out from U3103 is applied to U3102B. The 4-bit output data from U3102B and the three most significant bits from U3104 provide 128

binary codes which are applied to addresses 1 through 7 of ROM U3114. The most significant bit from U3102B is also applied to the bases of Q3103 and Q3104. These transistors produce a +12V square wave at the selected frequency to provide the reference tone to the audio frequency counter in the Digital Module.

C. ROM/DAC Circuit

ROM U3114 is programmed to produce binary codes to synthesize sine, square, ramp and triangle waveforms at a frequency selected through the CPU. The CPU controls these codes to also produce digitally controlled squelch (DCS) and Improved Mobile Telephone System (IMTS) pulse signals when these functions are selected. Addresses 7 through 11 of the ROM select the waveform to be synthesized, and addresses 0 through 6, providing 128 distinct timing codes, determine the relative phase position in the waveform cycle. From this information, the ROM produces an 8-bit output code corresponding to the amplitude required for the selected waveform at the particular phase position. Latch U3115, which is an 8-bit flip-flop, stores this code. When the oscillator clocks the adder system, it also clocks U3115. This latches the stored code from the ROM to DAC U3116 while simultaneously the adder system advances ROM addresses 0 through 6 to the next phase position, producing a new ROM output code. The coded input to U3116 turns on selected voltage dividers in the DAC, drawing a corresponding current. R3102 and R3103 are load resistors for the two current outputs from the DAC and with the resistors in the DAC, function as voltage dividers for op amp U3117A. U3117A compares the two voltage levels and produces a single output. R3103, being tied to ground, establishes symmetry to ground for the output signal. The resulting output from U3117A is an instantaneous voltage level corresponding to the amplitude required for the selected waveform at that particular phase position. As the oscillator continues clocking the adder system and the latch, the output voltage continues to change, describing the waveform throughout its cycle.

The signal from the ROM/DAC circuit passes through a two-stage 60 kHz low-pass filter consisting of U3117B, U3118A, and associated components. The signal is then sent to a 10 kHz low-pass filter, 1 kHz low-pass filter and multiplexer U3120. The 10 kHz low-pass filter is a two-stage filter consisting of U3124A and U3124B and associated components. The 1 kHz low-pass filter is a two-stage filter consisting of U3118B and U3119A and associated components. The output of all three filters are fed to multiplexer U3120 for selection. The selected signal is then fed to U3119B, which buffers the signal, then to pin 9 of P3102 and out to the front panel.

Function	Filter
Sine wave and DCS:	
Less than 819.2 Hz	1 kHz
819.2 thru 13106.2 Hz	10 kHz
13106.2 Hz or Greater	60 kHz
Square wave, Ramp, Triangle:	
Less than 819.2 Hz	10 kHz
819.2 Hz or Greater	60 kHz
PULSE	10 kHz

Table 2-1 Tone/Filter Selection for Function Generator

D. Frequency Range Logic

Because certain switching functions occur in the low-pass filter circuit and Receive Audio and Digital Modules resulting from frequency selections, a logic network provides the appropriate data. This circuit consists of 4-input NOR gates U3111A, U3111B, and U3113B, 8-input OR/NOR gate U3121, and NAND gates U3123A and U3123B. The NOR gates read the binary when all corresponding code lines are low.

U3121 reads all code lines for 409.6 Hz and above, and when all are low, supplies a low output to U3101A and a high to the Receive Audio Module. If any code line goes high in response to a frequency selection, the outputs are reversed.

U3101A reads the code lines for 102.4 Hz, 204.8 Hz, 409.6 Hz and the non-inverting output from U3121. When all of these lines are low (selected frequency is below 102.4), the output from U3101A to the Digital Module is high.

When the output of U3113B is low (indicating a frequency of 13,106.2 Hz or greater), it pulls down on the control line to U3120A through CR3103. This output also provides one input to U3123B.

U3101B reads the code lines for 819.2 Hz, 1638.4 Hz, 3276.8 Hz and 6553.6 Hz. It provides the second input to U3123B.

When both input lines to U3123B are high (i.e., the selected frequency is below 819.2 Hz), the output from U3123A is high. This output goes to the Digital Module and to U3123D in the low-pass filter circuit.

2-4-8 GENERATE AUDIO MODULE

NOTE: The Reference Designator Series assigned to the Generate Audio Module for the FM/AM-1200S is 62000. The Reference Designator Series assigned to the FM/AM-1200A is 3200. In the theory on the the following pages, the Reference Designator Series for the FM/AM-1200S is used. Any differences between the FM/AM-1200S and the FM/AM-1200A are shown in parentheses.

The Generate Audio Module receives audio signals from any or all of five sources: (1) 1 kHz fixed tone from the Digital Module; (2) a variable tone from the Function Generator; (3) through the MIC/ACC Connector; (4) through the EXT MOD Connector on the Front Panel or (5) DTMF from the DVM I/O PC Board. These signals are combined and amplified, with a tap from the output going to the TONE OUT Connector. For FM, the signal is sent directly to the 21.4 MHz VCO tuning line of the 10.7 MHz GEN/REC Module. For AM, the signal is routed through an AM modulator/leveler, which consists of two amplifiers and the GEN LEVEL FINE Vernier Control, and then to the 10.7 MHz GEN/REC Module.

The operating mode (Generate or Receive) of other modules is determined by an operating mode circuit in the Generate Audio Module. In the Generate Mode, a GEN command (+12 VDC signal) performs the following functions: (1) it enables the generate amplifiers in the IF Module and Output Amplifier; (2) in the 10.7 MHz GEN/REC Module, it enables the frequency divider and inhibits the receive-enable multiplexer; and (3) in the Receive Audio Module, it enables the Modulation Meter multiplexer in the deviation/percent modulation mode.

In Receive mode, an REC command (i.e., +12 VDC Signal) enables the receive amplifiers in the IF Module. An ANT ENABLE command (i.e., +12 VDC signal) energizes the Antenna Enable Relay, coupling the signal between the Antenna Connector and the IF Module. If the set is operating in the Generate Mode and a signal exceeding 100 mW is received at the T/R Connector, it is automatically switched to Receive mode, but the Antenna Enable Relay is not energized. Also, with the set in the Receive Mode, pressing the "Press-to-Talk" Key on the microphone automatically switches the set to the Generate mode and de-energizes the Antenna Enable Relay to route the generated signal from the IF block through the output amp.

The phase-lock indicator circuit consists of four logic NAND gates (two of which function as an oscillator), a transistor in the Generate Audio Module, related grounding circuits in the High Loop and Low Loop Synthesizers, and the GEN/LOCK Control on the Front Panel. When the appropriate frequency in each Synthesizer is equal to and in phase with its reference, neither grounding circuit conducts and the voltages applied to the inputs of the first gate in the indicator logic circuit are high. When neither input to the gate is grounded, the transistor supplies +5V power to the LED on the Front Panel,

indicating a phase-lock condition. If one or both inputs to the gate is grounded, or the GEN/LOCK Control is out of detent, the LED flashes, indicating an unlocked condition.

Audio signals from the Receive Audio Module low-pass filters are also routed to the Generate Audio Module for DCS (Digitally Coded Squelch) decoding and SINAD/Distortion Analysis switching.

In the FM/AM-1200S, the power sense goes through the GENERATE AUDIO PC BD to be buffered to a TTL level, and is output through the Motherboard to the DVM I/O PC Board.

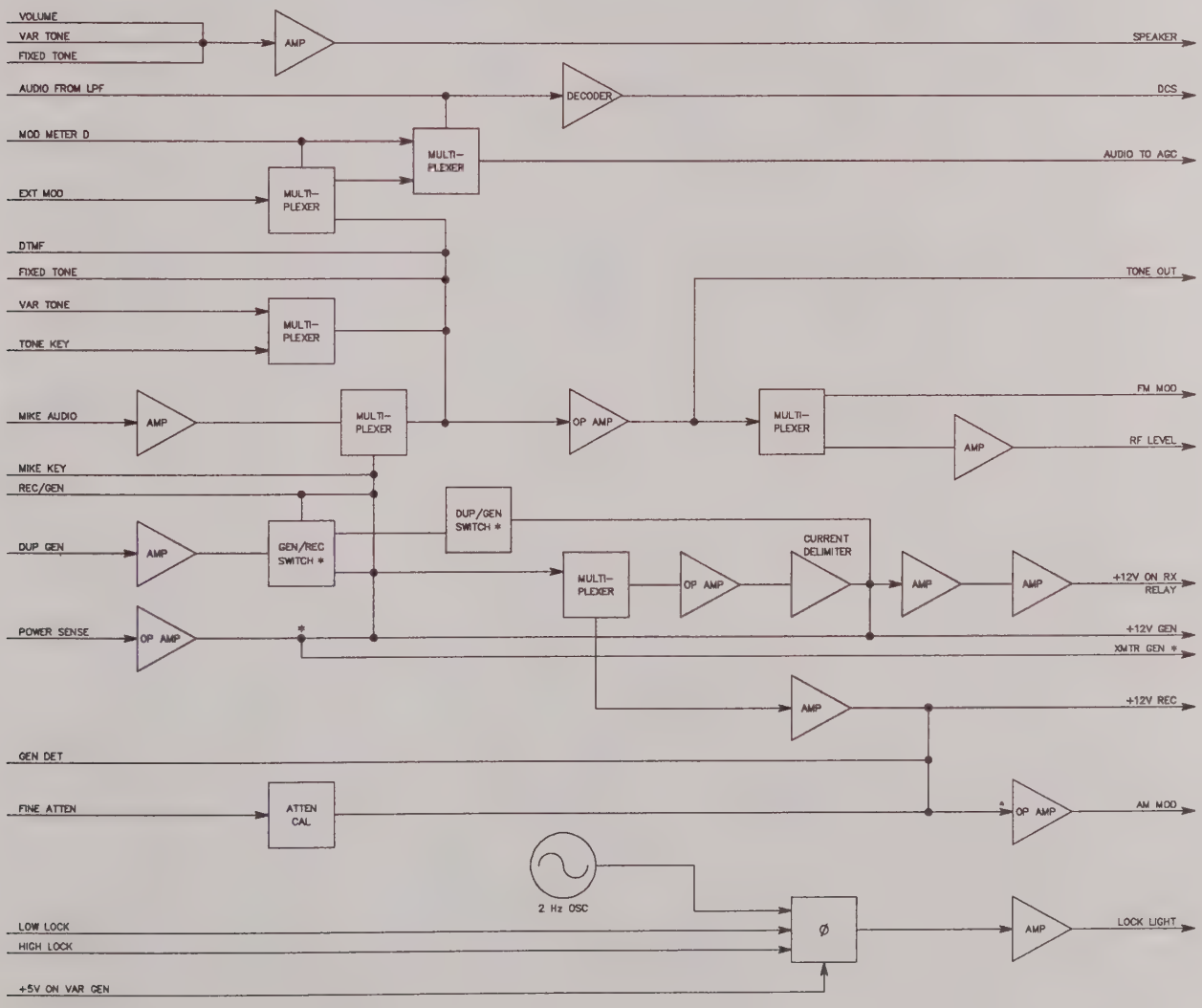


Figure 2-15 Generate Audio Module Block Diagram

A. Speaker Amplifier Circuit

The demodulated audio from the Receive Audio Module, 1 kHz fixed tone from the Digital Module, and the tone from the Function Generator are combined in the Generate Audio Module and fed to audio amp U62001. U62001 amplifies the combined signal and sends it to the Speaker.

B. Operating Mode Circuit

The voltage applied at pin 11 of multiplexer U62005 controls transistors Q62001, Q62002, Q62004 and Q62007. Q62001, a current limiting transistor, supplies the generate enable voltage; Q62002 supplies the receive enable voltage; and Q62004 supplies the voltage to energize the antenna relay. Output from op amp U62007 determines the output of Q62003, which, in turn, determines the output to Q62004.

When pin 11 of U62005 is low (i.e., generate or duplex generate mode is selected or the "Press-to-Talk" Key on the Microphone is pressed), pin 12 conducts, via pin 14 to ground. This turns on Q62007 and, subsequently, Q62001, which applies +11 VDC to the base of Q62003 and to enable the Generate Function. Q62003 is turned off, which turns off Q62004, and interrupts power to the antenna relay. The de-energized relay then conducts the RF signal from the IF Module to the Output Amplifier Module. When pin 11 of U62005C is high (i.e., Receive Mode is selected), pin 13 conducts through pin 14 to ground, turning on Q62002. Q62002 applies +12V to enable the receiver functions and to drive the AM modulator/leveler circuits to maximum attenuation of the signal generator VCO output in the 10.7 MHz Gen/Rec Module.

The Power Sense from the Receive Audio Module furnishes a positive voltage to pin 3 of op amp U62007. This voltage level is proportionate to the strength of any RF signal received at the T/R Connector. With no voltage applied to pin 3, the output of pin 6 is low, pulling down the bias voltage on Q62003, turning on Q62004 and energizing the antenna relay. This couples the ANTENNA Connector into the IF Module. If an RF signal exceeding 100 mW is applied at the T/R Connector, the voltage on pin 3 of Q62007 goes higher than on pin 2, and the output at pin 6 goes high. Q62003 and Q62004 are turned off, the antenna relay is de-energized, and the received signal from the T/R Connector is coupled into the IF Module. The high output from pin 6 of U62007 is also applied to pin 11 of U62005C. This causes U62005C to switch to Receive Mode if GENERATE is selected. It does not override the duplex generator or the microphone key.

When Duplex Generate Mode is selected, a high turns on transistor Q62006, which pulls down on pin 16 of U62010C and pin 11 of U62005C. This selects Generate Mode, regardless of any signal applied at the T/R Connector.

In Cellular Mode, the REC/GEN input line is high. This sets pin 11 of U62010 high, and pins 10, 12, 13 and 14 of U62010 low. Pin 10 of U62010 is only low when cellular mode is activated. This forces Q62003 and Q62004 low, which sets the +12V ON RECEIVE RELAY output (pin 29 of P62001) high.

C. Audio Switching Circuit

All audio signals supplied to the Generate Audio Module for modulation are combined and applied to pin 6 of op amp U62003B. The 1 kHz fixed tone and the DTMF tone go directly to the amplifier. Signals from the microphone, Function Generator, and any signal applied through the EXT MOD/SINAD Connector first go through switching circuits. The "Press-to-Talk" Key on the microphone pulls down on pin 9 of multiplexer U62009B, coupling the microphone audio signal at pin 4 to pin 5, before sending it to the amplifier. The Function Generator signal at pin 3 of multiplexer U62002C is normally coupled to pin 4, before it is sent to the amplifier. When pin 9 of U62002B is pulled low, the Function Generator signal is interrupted.

The output from pin 1 of U62003A goes to the TONE OUT Connector on the Front Panel and to pin 15 of de-multiplexer U62005A. When FM is selected, on the MODE Selector Control on the Front Panel, pin 10 of U62005A is low, and the signal at pin 15 is applied through pin 2 to the 10.7 MHz Gen/Rec Module. Selecting one of the AM Modes applies a high to pin 10, coupling the signal on pin 15 to pin 1 before applying it to pin 6 of modulator/leveler op amp U62004B.

D. Modulation Circuit

The output from pin 7 of op amp U62004B goes to the RF Level Attenuator Vernier Control on the Front Panel. Trimpot R62046 calibrates the control for -12 dB attenuation. From the potentiometer wiper, the signal returns to trimpots R62024 and R62027 for calibration. From R62024, the signal is applied to pin 2 of op amp U62004A and to the AM modulator circuit in the 10.7 MHz Gen/Rec Module. The generate level signal from the Output Amplifier is summed with the modulating signal at pin 2 of op amp U62004A, providing a positive offset proportionate to the RF level detected by the Output Amplifier. Accordingly, this biases the output of op amp U62004A and increases attenuation in the AM modulator circuit of the 10.7 MHz Gen/Rec Module until the RF level, at the level detector in the Output Amplifier, is 0 dBm. When the FM/AM-1200S/A is in Receive or Duplex mode, the +12V output from transistor Q62002 is summed with any modulation signal applied to pin 2 of op amp U62004A. This voltage drives the output at pin 1 to 12V, which drives the AM modulator circuit to maximum attenuation and blanks out the generator VCO signal in the 10.7 MHz Gen/Rec Module.

E. Phase-Lock Indicator Circuit

The NAND gates U62006C and U62006D, resistors R62042 and R62043, and capacitor C62018 form a 2 Hz oscillator. The oscillator output from pin 11 of U62006D is applied to pin 5 of U62006B.

While approximately +5 VDC is applied to pins 1 and 2 of U62002A, the output on pin 3 remains low. If either the High Loop or Low Loop is not phase-locked to the appropriate reference frequency, one of the inputs goes low, and pin 3 goes high. While pin 3 is low and the GEN/LOCK Control is in Lock position, the input to pin 6 is a constant low, making the output at pin 4 a constant high. When the input to pin 6 is high, the oscillating input to pin 5 causes the output at pin 4 to oscillate. The high output from pin 4 turns on transistor Q62005 to supply +5 VDC, either steady or pulsing according to the high or low state of pin 4 of U62006, to the LOCK Lamp LED on the Front Panel.

F. DCS Circuit

The LPF audio signal is routed to the DCS decoder U62009. If DCS is present in the received audio signal, U62009A detects it and U62009B will send the signal to the Interface PC Board.

G. Transmit Detection Line (FM/AM-1200S Only)

The power sense goes through GENERATE AUDIO PC BD to be buffered to a TTL level, and is output through the Motherboard to the DVM I/O PC Board. There the XMIT Detect goes to a dual 4-input multiplexer chip which switches the 10.7 MHz Module from the 15 kHz filter to the 200 kHz filter when RF power is applied to the T/R Connector.

2-4-9 10.7 MHz GEN/REC MODULE

In the Generate mode, the 10.7 MHz Gen/Rec Module utilizes a VCO tuned to 21.4 MHz to provide the carrier for RF signal generation. The output of the VCO is sampled by the Digital Module, which returns an analog tuning voltage to maintain the frequency at 21.4 MHz. When FM modulation is required, an audio modulation voltage from the Generate Audio Module is combined with the tuning voltage to produce frequency modulated output signal. A flip-flop divides the VCO output signal in half to produce the 10.7 MHz signal. This signal passes through an attenuator which, in the Generate AM mode, modulates the carrier with the audio modulation voltage from the Generate Audio Module. The signal is then sent to the IF Module and to the receiver circuit to allow the Receive Audio Module to monitor and display the signal on the Modulation and Frequency Error Meters.

In the Receive mode, the 10.7 MHz signal from the IF Module is fed to the receive enable circuit, two AGC controlled amplifiers, and one of

three bandpass filters. These filters have a center frequency of 10.7 MHz with bandwidths of 200 kHz (FM Wide and Mid), 15 kHz (FM Narrow and AM Norm) and 6 kHz (AM Narrow and SSB). The signal is amplified again by a third AGC controlled amplifier, then demodulated, with the AM and FM audio going to the Receive Audio Module and the 10.7 MHz carrier going to the Digital Module. When in the Receive SSB Mode, a flip-flop divides the 21.4 MHz output of the VCO to 10.7 MHz and, through a BFO level potentiometer, injects the beat frequency into the modulated signal just ahead of the AM demodulator.

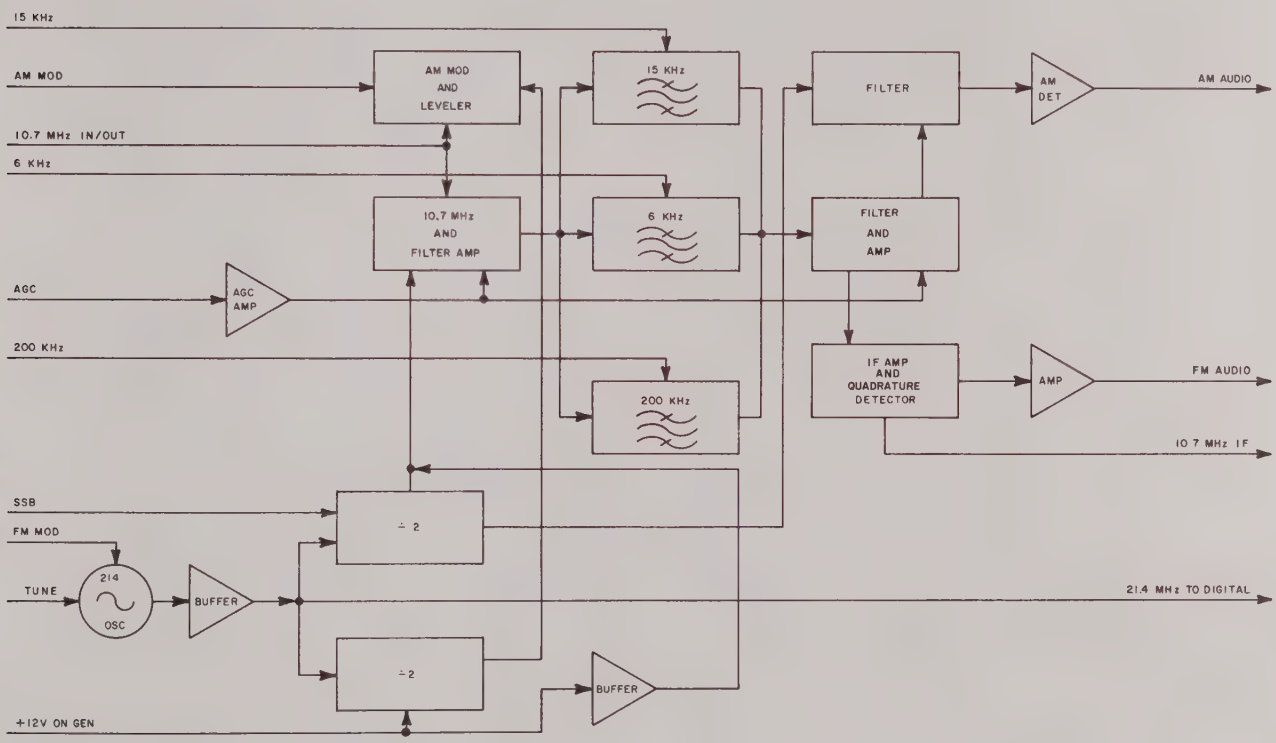


Figure 2-16 10.7 MHz GEN/REC Module Block Diagram

A. Receive Enable/Inhibit Circuit

The 10.7 MHz IF signal from the IF Module first enters the receive circuit through J4302, diode CR4301 and tuned filter FL4301 to the bandpass amplifier. Resistor R4384 loads the circuit to prevent oscillation. A positive bias normally turns on CR4301. However, in the Generate mode, +12V is applied to the base of transistor Q4307. Q4307 grounds the bias voltage, turning off CR4301. Capacitor C4348 couples a sample of the generated signal into the receiver circuitry for monitoring.

B. Bandpass Amplifier Circuit

The output from pin 3 of FL4301 is applied to the gate (pin 3) of FET Q4301. Filter FL4302 tunes the drain (pin 1) of Q4301 for the best AM envelope. The signal is then applied to the gate (pin 3) of FET Q4302. Filter FL4303 tunes the drain (pin 1) of Q4302 to 10.7 MHz. From FL4303, the signal is split and applied to three essentially identical bandpass filters.

Each filter consists of, in signal flow order, a blocking diode, a crystal filter, a transistor amplifier, a second crystal filter, and a second blocking diode. Diodes CR4308 and CR4312, 200 kHz crystal filters YFL4305 and YFL4306, RF transistor Q4310, and associated circuitry form the FM WIDE and FM MID filter; diodes CR4302 and CR4303, 15 kHz crystal filters YFL4301 and YFL4302, RF transistor Q4308, and related components form the FM NAR and AM NORM filter. The AM NAR and SSB filter consists of diodes CR4305 and CR4306, 6 kHz crystal filters YFL4303 and YFL4304, RF transistor Q4309, and affiliated components. To select one filter, a +12 VDC bias is applied to the two diodes and the collector of the transistor by the Front Panel MODE Selector Control, allowing the signal from FL4303 to reach pin 1 of the first crystal filter. The other two filters are then reverse biased with -5V to prevent conduction. The filter output at pin 3 is applied to the base of the transistor, producing the input to pin 1 of the second crystal filter. The output of the second filter at pin 3 then passes through the second diode of filter FL4304. From FL4304, the signal is coupled by capacitor C4319 to the gate of FET Q4311. The drain of Q4311 is applied through filter FL4305 to the AM and FM demodulator circuits. Transistors Q4303 and Q4304 control the gain of FETs Q4301, Q4302 and Q4311. As long as the AGC voltage from the Receive Audio Module signal control circuit is positive, the FETs apply maximum gain to the IF signal. As the AGC voltage becomes increasingly negative, Q4303 and Q4304 pull down proportionately on the voltage applied to the input gates of the three FET's, thus reducing their gain.

C. AM Demodulator Circuit

The output from pin 2 of FL4305 is AC coupled through capacitor C4328 to the base of RF transistor Q4312. When the SSB mode is selected, a 10.7 MHz BFO signal from the signal generator is also injected through inductors L4308 and L4309 and capacitors C4328, C4329 and C4331 to the base of Q4312. Q4312 and associated components amplify the signal, which is coupled through tuned filter FL4307 to an AM detector consisting of diode CR4304 and capacitor C4327. A bias voltage, supplied through resistor R4374, capacitor C4330, diode CR4315, and FL4307, keeps CR4304 turned on sufficiently to demodulate the signal linearly. The demodulated audio signal, applied to pin 5 of op amp U4303, is buffered by U4303 and asociated components.

The output at pin 7 is filtered by choke L4305 and capacitor C4344, then routed to the Receive Audio Module.

D. FM Demodulator Circuit

The output from pin 4 of FL4305 is coupled to the base of RF transistor Q4313. Q4313, limiting diodes CR4317 and CR4318 and associated components, form a limiting amplifier which strips off any AM and amplifies the remaining signal. The signal is then applied to pin 4 of U4302. U4302 is an IF amplifier with quadrature detector. Resistor R4378, choke L4320, and capacitors C4341, C4342 and C4380 form a tuned circuit for the detector. One output from pin 1 of U4302 is the demodulated FM audio. The IF carrier, at 10.7 MHz, is routed from pin 9 to the Digital Module through J4303.

E. Signal Generator

FET Q4305 and related timing components produce a frequency of 21.4 MHz. As the tuning voltage is varied by the Variable GEN Control on the Front Panel, the oscillator frequency varies a minimum of 10 kHz above and below 21.4 MHz. Variable choke L4312 adjusts the frequency to 21.4 MHz at 4.80 VDC, which is mid range of the GEN Control travel. Diode CR4310 is an AGC for the oscillator. After filtering by capacitor C4362, inductor L4319 and resistor R4362, the signal is buffered by transistor Q4306, then AC coupled through capacitor C4357 to J4304, and routed to the Digital Module for phase-locking to the Frequency Standard. The Digital Module then produces the tuning voltage for phase-locking the oscillator, or switches the variable generator tuning voltage to the oscillator when the GEN Control is out of the LOCK detent. In the FM mode, the modulating voltage from the Generate Audio Module is applied through pin 16 of J4301 to varactor CR4309.

The output signal from the VCO circuit at Q4306 is applied to pins 3 and 11 of dual flip-flop U4301. When SSB is selected, +12 VDC applied at pin 1 of U4301A allows the 21.4 MHz signal at pin 3 to clock the flip-flop, which produces a 10.7 MHz output at pin 5 (Q). Trimpot R4351 permits adjustment of the output (BFO) level. The signal is then applied to the AM demodulator circuit. When the generate function is selected, +12 VDC is applied to pin 13 of U4301. This allows the 21.4 MHz signal at pin 11 to clock the other flip-flop, producing a 10.7 MHz output at pin 9 (Q).

F. AM Modulator/Leveler Circuit

A filter consisting of capacitors C4368 and C4369, and choke L4314 shapes the square wave from pin 9 of U4301 into a sine wave. Diodes CR4313 and CR4314, chokes L4315 and L4316, capacitor C4370 and resistors R4352 and R4353 form a voltage

controlled attenuator. The modulating/leveling voltage from the Generate Audio Module biases the diodes, varying the attenuation of the 10.7 MHz signal accordingly. From the modulator/leveler circuit, the 10.7 MHz signal is routed through J4302 to the IF Module.

2-4-10 HIGH LOOP MODULE

The Dual VCO difference frequency of 90-1088 MHz is divided by a number programmed by the RF selection. The result is compared to the 500 kHz reference frequency from the Frequency Standard Module. A control circuit then steers the 1300-2298 MHz VCO to the frequency corresponding to the RF selection. Also, a second, rapid response control circuit steers the frequency of the 1210 MHz VCO to cancel noise produced by the 1300-2298 MHz VCO.

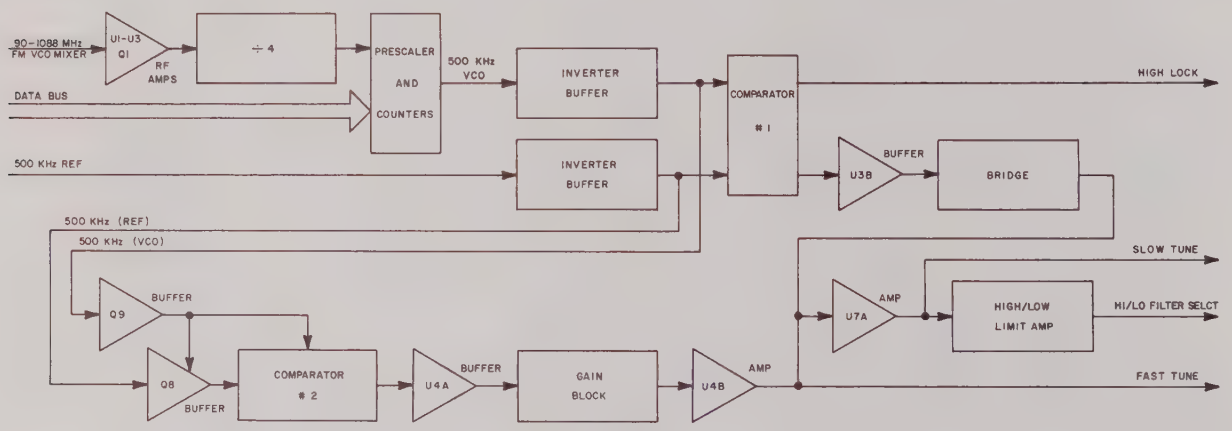


Figure 2-17 High Loop Module Block Diagram

A. Signal Amplifier

The 90-1088 MHz signal, produced in the dual VCO, is amplified by op amps U4101 through U4103 and RF transistor Q4101. Capacitors C4108, C4111, C4114, C4121 and C4123 provide DC isolation of the inputs and outputs of the amplifiers, while RF chokes L4101 through L4103 and associated capacitors, preventing crosstalk through the power supply. L4104, C4124 and C4127 provide RF isolation of the amplifier circuit from the +12V power source. The amplified signal is applied to the programmable divider network and the Duplex Generator Module.

B. Programmable DIVIDER Network

The programmable divider network divides the 90-1088 MHz signal by a selected number between 180 and 2176 to produce a 500 kHz

output. It consists of prescalers U4104 and U4107, programmed counters U4105, U4106 and U4109, quad NOR gate U4108, dual flip-flop U4110, and associated resistors, capacitors and diodes. BCD coding, initiated by the keyboard RF selection, loads the counter as follows: 2, 4 and 8 MHz sets U4105; 10, 20, 40 and 80 MHz sets U4106; and 100, 200, 400 and 800 MHz sets U4109.

The 90-1088 MHz signal from Q4101 is received by ÷4 counter U4104. U4104's output is then applied to ÷5/÷6 prescaler U4107, which clocks the three counters and U4110B. While a count is loaded into U4105, the output of U4108B is low, allowing U4107 to divide by six. When U4105 counts down to zero, U4108B goes high, and U4107 divides by five for the remainder of the counting period. U4108B, pin 5 also pulls up on pin 10 of U4105, stopping U4105 from counting until the next load cycle. U4107 will be forced to ÷5 during load operation as U4107, pin 2 is pulled high. U4105, U4106 and U4109 are programmed as down counters. When U4109 reaches zero count, the next clock pulse will bring pin 3 of U4109 high, clocking U4110. This brings pin 13 of U4108 low. When U4106 reaches count 7, pin 3 of U4106 will also go low bringing U4108, pin 9 low. As count 3 is reached, pin 20 of U4106 goes low. Pins 4 and 5 of U4108 are now both low, forcing pin 2 of U4108 high.

The next clock pulse (count 2) will clock U4110B, bringing Q (pin 15) high and $\overline{Q}$ (pin 14) low. U4110B $\overline{Q}$ loads counters U4105, U4106 and U4109. U4110B Q resets U4110A bringing $\overline{Q}$ high. This forces the Q input to U4110 low. The next clock pulse (count 1) removes the load condition from U4105, U4106 and U4109, allowing them to count normally. It takes nine clock pulses from U4107 after U4109 reaches zero to reset the system. Pins 4 and 5 of U4107 take the ECL outputs of U4110A, pin 3 and U4110B, pin 15 and converts them to a TTL output at pin 7 of U4107. U4107, pin 7 should be 500 kHz.

C. Frequency Comparator Circuit

The frequency comparator circuit compares the output frequency from the programmable divider network to a 500 kHz reference from the Frequency Standard. If the two square wave signals are not synchronized, the comparator circuit produces an out-of-lock indication and an integrator provides steering voltage to the 1300-2298 MHz VCO integrator circuit.

The reference frequency is applied to the clock at U4002B and the controlled frequency to the clock of U4002A. U4002 is a dual, negative edge triggered flip-flop. Depending upon the phase relationship of the two signals, the flip-flops vary the voltage on C4006, the input to op amp U4003B, to produce a correction voltage. When the signals are in phase, R4019 and R4021 set the input voltage at approximately +2.5V, resulting in a correction voltage of approximately zero.

flops are clocked simultaneously, U4001B instantly resets U4002A and U4002B, and capacitors C4005 and C4006 prevent any instantaneous systems responses. However, if one signal leads the other, the outputs of U4002A and U4002B will be opposites for the period of time one leads the other. This causes the output of U4001D to go high and allows the voltage applied to U4003B to be raised or lowered accordingly through CR4005 or CR4004.

With the output of U4001D high, Q4007 conducts, thus illuminating LED CR4106 on the divider board. It also pulls down on pin 2 of U62006A in the phase-lock indicator circuit in the Generate Audio Module, causing the LOCK Lamp LED on the Front Panel to flash.

When the voltage on pin 5 of U4003B deviates from normal, the output voltage varies directly from zero. This voltage is then applied to a bridge consisting of diodes CR4008, CR4009, CR4010 and CR4011. Any positive or negative voltage from U4003B, exceeding two diode gaps from zero, is applied to the 1300-2298 MHz VCO integrator circuit to correct its frequency. The effect of the bridge is to delay shifting the 1300-2298 MHz VCO for detailed noise while allowing the 1210 MHz oscillator to make the necessary shift to cancel the noise.

D. 1300-2298 MHz VCO Control Circuit

An integrator circuit containing Q4012 and op amp U4007A controls the voltage level applied to the 1300-2298 MHz VCO. Op amps U4008A and U4008B, with trimpots R4060 and R4061, set the high and low voltage limits, thus establishing the low and high frequency limits at approximately 1275 and 2300 MHz respectively. Op amp U4007B, calibrated by trimpot R4065, establishes the switching frequency of the High/Low-pass Filter, and supplies either +12V or -12V as required.

E. Phase Comparator

The phase comparator circuit contains two sample and hold circuits to compare the phase relationship of the programmable divider output signal to the 500 kHz reference signal, and an integrator circuit to supply a correction signal.

In the first sample and hold circuit, the reference signal is buffered by Q4002, then applied to the emitter of Q4001 and the collector of Q4003. The controlled signal is applied to the base of Q4005, which applies a corresponding sampling pulse to the bases of Q4001 and Q4003. For the duration of this pulse, if the reference signal is high, Q4003 conducts and charges C4002; if the reference is low, Q4003 conducts, and discharges C4002. The net charge held by C4002 is proportional to the phase relationship of the two signals.

The voltage at C4002 is buffered and inverted by Q4004 and Q4008, then applied to the source of Q4011. The sampling pulse from Q4005 is coupled by a delay network consisting of Q4006 and Q4009. When the gate of Q4011 goes high, the voltage at the source is coupled to the drain and held by C4010. Q4010 supplies a pulse 180° out of phase with the gate pulse to Q4011. This pulse is calibrated by trimpot R4032 and coupled to C4010 to null 500 kHz transition noise. The voltage level at C4010 is applied to op amp U4004A. The gain of U4004 is such that when the two signals are synchronized, its output level is zero volts.

F. 1210 MHz VCO Control Circuit

In order for the phase comparator to make corrections over the entire span of the 1300-2298 MHz VCO, the control signal from U4004A must vary considerably. To maintain an adequate response of the 1210 MHz VCO, the gain of op amp U4004B is controlled by the RF selection. Switches U4005A, U4005B, U4005C, U4006A, U4006B and U4006C, enabled by frequency select control lines (40, 80, 100, 200, 400 and 800 MHz), select various resistances which, in conjunction with R4044 and trimpot R4045, establish the correct gain for U4005B. The output of U4005B is filtered, then routed to the 1210 MHz VCO in the Dual VCO. An attenuated control signal is also applied through R4046, to the 1300-2298 MHz VCO control circuit to coordinate frequency changes required to phase-lock the programmable divider output frequency to the 500 kHz reference signal.

2-4-11 DUAL VCO MODULE

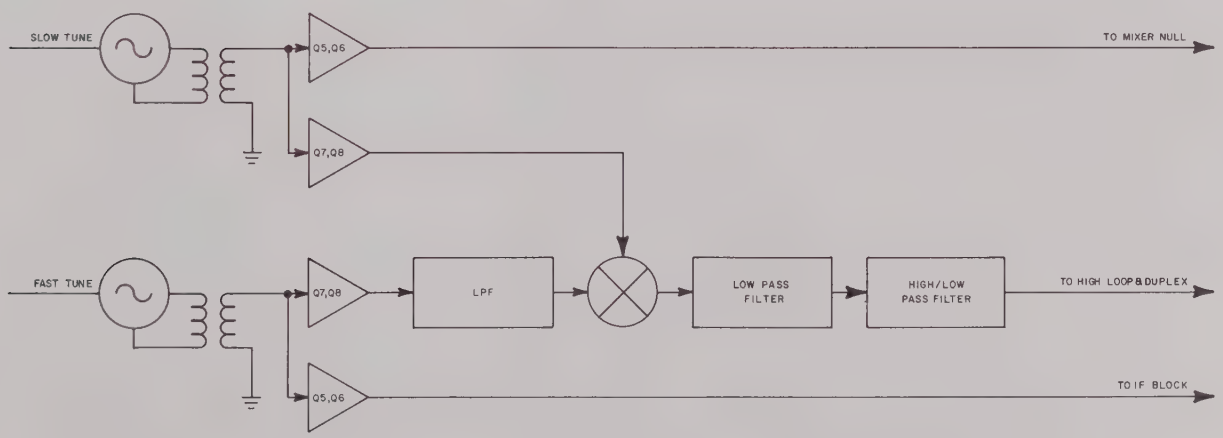


Figure 2-18 Dual VCO Module Block Diagram

The following theory of operation is provided to explain the interaction of the Dual VCO with other modules. It is not intended to provide sufficient theory for testing or repairing individual circuits within the module.

CAUTION: THE DUAL VCO IS NOT FIELD REPAIRABLE AND SHOULD BE RETURNED TO THE MANUFACTURER IF TESTS INDICATE THE MODULE IS FAULTY. ATTEMPTS TO REPAIR THE MODULE WITHOUT SPECIALIZED EQUIPMENT AND SPECIFIC KNOWLEDGE OF THE WORKINGS OF THIS MODULE, CAN DRASTICALLY ALTER ITS CHARACTERISTICS AND CAUSE THE MODULE TO BE UNSERVICEABLE.

The Dual VCO Module produces two of the three local oscillator frequencies required by the IF Module. These frequencies are also mixed to produce the difference frequency used by the High Loop Module to control the Dual VCO, and by the Duplex Module to produce the offset frequency when operating in the Duplex Mode.

The first VCO frequency is varied between 1300 MHz and 2298 MHz in 2 MHz increments by the High Loop in response to the megahertz portion of the RF selection (RF selection within each of the 2 MHz increments controls the Fast Low Loop frequency). The second VCO frequency is tuned to 1210 MHz, but this frequency is inversely modulated to cancel noise produced by the first VCO. The two frequencies are mixed in the Dual VCO, with the mixed frequency being filtered by two external filters and applied to the High Loop Module, then to the Duplex Generate Module. The High Loop compares the difference frequency (90 MHz to 1088 MHz) to a standard frequency and produces the tuning voltage for the 1300-2298 MHz VCO and the frequency modulating voltage for the 1210 MHz VCO. The tuned VCO outputs are then applied to the IF Module.

2-4-12 1120 MHz LOW-PASS FILTER

The 1120 MHz Low-pass Filter is a tubular in-line filter tuned to attenuate all frequencies above 1120 MHz by at least 40 dB. This allows only the 90-1088 MHz difference frequency from the 1300-2298 MHz VCO and 1210 MHz VCO in the Dual VCO Module to reach the High/Low-pass Filter. The filter is tuned and sealed at the factory and is not field repairable.

2-4-13 HIGH/LOW-PASS FILTER

The High/Low-pass Filter prevents harmonics of lower frequencies (which may pass through the 1120 MHz Low-pass Filter) from interfering with the High Loop frequency comparator. The 90-1088 MHz signal from the 1120 MHz Low-pass Filter is received at J602. Depending upon whether the 10 VDC control signal from the High Loop is negative or positive, when the signal is applied at FL601, diode switches route the signal through either a 450 MHz high-pass filter or a 520 MHz low-pass filter, respectively. The actual crossover frequency, established in the High Loop, varies from set to set, and is marked on the outside of each module when calibrated at the factory.

2-4-14 FAST LOW LOOP MODULE

The Fast Low Loop Module produces a frequency from 77.3 to 79.3 MHz. This VCO signal is applied to the Spectrum Analyzer (in the FM/AM-1200S) and the third LO Mixer in the IF Module.

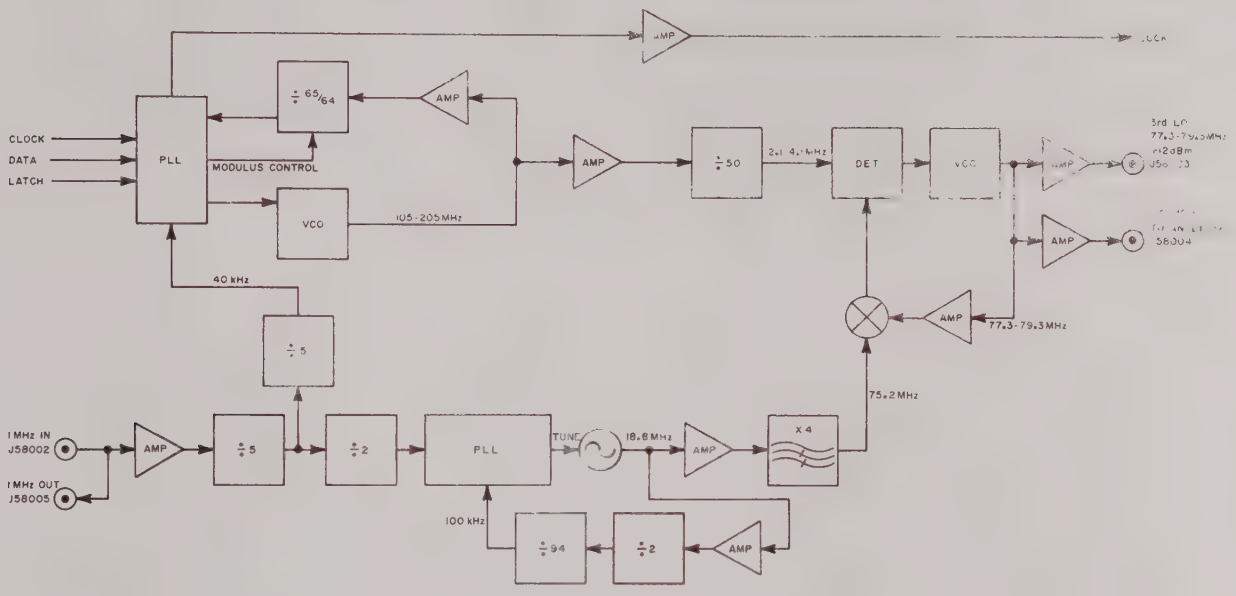


Figure 2-19 Fast Low Loop Module Block Diagram

A. Reference Divider Circuit

A 1 MHz reference, from the Frequency Standard Module, enters at J58002 and is output at J58005. A 1 MHz sample is sent through transistor Q57012 to U57016A where it is divided by 5. The 200 kHz is then sent to dividers U57016B and U57016C. U57016C divides the 200 kHz by 2 and feeds the signal to U57012 in the 18.8 MHz Phase-Lock Loop. The 200 kHz sent to U57016B is divided by 5 and used as reference to the 105-205 MHz Phase-Lock Loop.

B. 105-205 MHz VCO Circuit

The 40 kHz from U57016B is sent to U57006 Phase-Lock Loop and used as a reference. This reference frequency is compared to a 40 kHz input fed to U57006 from a ÿ64/ÿ65 prescaler, U57008. The serial data bus provides clock, data and latch inputs to U57006. The output from U57006 is fed through Phase Detector U57007A, B, D, circuitry to phase-lock the 105-205 MHz VCO. Output from Phase Detector U57007A, B, D determines the charge on capacitor C57048. U57009 and associated components form an integrator to supply the VCO steering voltage. The VCO circuit then feeds a 105-205 MHz back to a Dual Modulus prescaler, U57008 and to U57001 in the 77.3-79.3 MHz Phase-Lock Loop.

C. 18.8 MHz Oscillator

Phase Detector U57012 receives a 100 kHz fixed frequency from U57016C and 100 kHz signal from U57017. U57012 compares the two 100 kHz signals and sends a DC correction voltge from pin 13 to the 18.8 MHz Oscillator Circuitry. The 18.8 MHz Oscillator circuitry is made up of crystal oscillator Y57001, varactor CR57006, and associated components. An 18.8 MHz signal is fed in two directions. After amplification by Q57016, the 18.8 MHz goes through a Bandpass Filter tuned to the fourth harmonic, producing 75.2 MHz to MXR57001. The additional 18.8 MHz is amplified by Q57014 and sent to a 2 chip, U57016D. The 9.4 MHz from pin 13 on U57016D is fed through U57017 divided by 94, producing the 100 kHz entering U57012 at pin 3.

D. 77.3-79.3 MHz VCO

The 75.2 MHz sent to MXR57001 is mixed with 77.3-79.3 MHz from the 77.3-79.3 MHz VCO producing a difference output of 2.1 to 4.1 MHz. This signal is applied to a Phase Detector made up of U57004,U57003 and related components. A 105-205 MHz signal is input to pin 15 of U57001 a ÿ10 prescaler, then to U57002 to be divided by 5. The output of the Phase Detector circuitry is kept constant by the DC correction voltage on capacitor C57012. Output from C57012 is fed through Op Amp U57005 to the VCO circuitry. The VCO circuitry is made up of FET Q57002, varactor CR57003 and associated components. After passing through the VCO circuitry, the 77.3-79.3 MHz signal is applied through buffer amplifiers Q57004 and Q57005 to J58003 and J58004 respectively and to MXR57001.

2-4-15 MIXER NULL ASSEMBLY

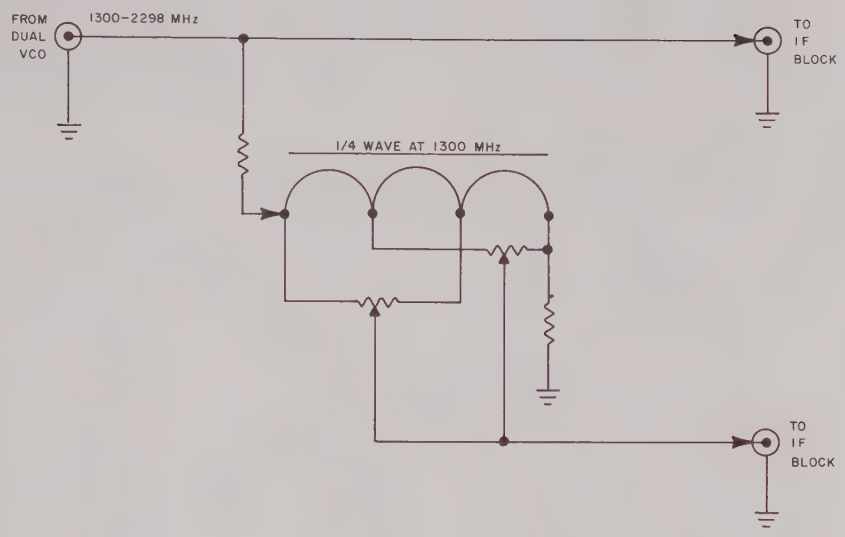


Figure 2-20 Mixer Null Assembly Block Diagram

The Mixer Null Assembly receives the 1300-2298 MHz signal from the Dual VCO Module, where it is split, with one signal being fed directly to the first mixer in the IF Module, and the other being routed to a phase shift circuit, whose output is 180° out of phase with the first mixer. Trimpot R9402 selects an amplitude of the 1300 MHz signal between the 0 and 180° points and Trimpot R9402 selects the signal amplitude between the 90° and 270° points. The two selected signal amplitudes are combined and fed to the IF Module where it is combined with the output of MXR9402. The level of this signal, as set by R9402 and R9403, reduces the LO feed-through level at the IF frequency of 1300 MHz.

2-4-16 IF BLOCK ASSEMBLY

The function of the IF Module, in the Receive Mode, is to select the signal source, then convert the selected RF to 10.7 MHz IF and reject all other frequencies. In the Generate Mode, the IF Module converts the generated 10.7 MHz IF to the selected RF and directs the signal to the Output Amplifier. One low-pass and two bandpass filters, three mixers, two amplifiers, and signals from three local oscillators accomplish this conversion. A separate Null Mixer Assembly is installed to reduce the level of the zero pulse.

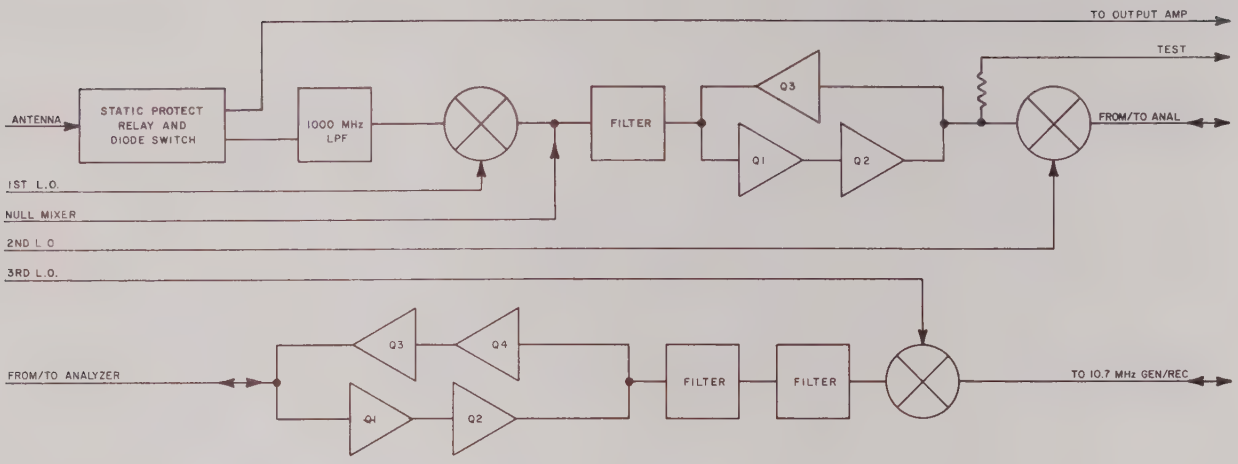


Figure 2-21 IF Block Assembly Block Diagram

A. Receive Mode

An RF signal from the antenna, received at J2201, first passes through static protect and diode switch circuits. R3801, CR3801 and CR3802 form the static protect. R3803, R3802, C3801, C3802, CR3803 through C3806, L3801 and L3802 form the diode switch. When the +12V antenna enable command is applied to the antenna enable circuit, the two resistors maintain a forward bias on the diodes to conduct the RF signal, while the two capacitors isolate the DC from the RF circuits and the two inductors isolate the RF from the power supply circuits. A constant gain amplifier is installed prior to relay K3801. The amplifier circuit consists of Q3801, C3803, C3804, and R3805 through R3808. The +12V antenna enable command activates the amplifier only when the FM/AM-1200S/A is in REC mode or when an FM/AM-1200S is in cellular mode.

The command also energizes the antenna enable relay, coupling the antenna circuit into the first IF mixer circuit. However, if the Receive Mode is selected and a signal is applied to the T/R Connector which exceeds 100 mW, power detector and switching circuitry interrupts the antenna enable command, switching the relay to couple the signal from the T/R Connector to the mixer circuit.

Low-pass microstrip filter, FL2211, limits the RF to less than 1000 MHz. MXR2202 then mixes the received signal with the 1300-2298 MHz signal from the Dual VCO. The mixer output is then combined with the noise cancellation signal from the Null Mixer Assembly. A 20 MHz bandpass filter at 1299 MHz, which consists of three tuned cavities in Z2201, passes only the difference frequency. Q2401, Q2402 and associated circuitry form a 1300 MHz amplifier which is enabled by the +12V receive

command when the Receive or Duplex mode is selected. MXR2201 then mixes this difference frequency with the 1210 MHz signal from the Dual VCO. In the FM/AM-1200S, the mixed signal is routed to the Spectrum Analyzer RF Module and then returned to J2208. In the FM/AM-1200A, the mixed signal is jumpered directly to J2208.

The mixer signal is amplified by Q2203, Q2204 and related components, then filtered by FL2201, FL2202, FL2203, FL2301 and FL2302 to 88-90 MHz. MXR2301 then mixes the signal with the 79.3000-77.3001 MHz signal from the Fast Low Loop Module. The resulting signal is then applied to the 10.7 MHz Gen/Rec Module.

B. Generate Mode

MXR2301 mixes the 10.7 MHz signal from the 10.7 MHz Gen/Rec Module with the 79.3000-77.3001 MHz signal from the Fast Low Loop Module. FL2301, FL2302, FL2201, FL2202 and FL2203 then pass the sum frequency of 88-90 MHz. Q2201, Q2202 and related components amplify the signal. In the FM/AM-1200S, the mixed signal is routed to the Spectrum Analyzer RF Module and then returned to J2209. In the FM/AM-1200A, the mixed signal is jumpered directly to J2209.

MXR2201 mixes the signal with the 1210 MHz signal from the Dual VCO Module. The signal is then amplified by Q2403 and related components. The three tuned cavity bandpass filters of Z2201 then pass the sum frequency of 1298-1300 MHz, which is then mixed by MXR2202 with the 1300-2298 MHz signal from the Dual VCO Module. 1000 MHz low-pass microstrip filter, FL2211, passes only the difference frequency, which is the selected RF. The signal is then routed through the unenergized antenna enable relay, K3801, and J2202 to the Output Amplifier.

2-4-17 OUTPUT AMPLIFIER MODULE

The Output Amplifier Module, in the Receive Mode, couples any signal received at the T/R Connector through a series of fixed attenuators to the IF Block, and also routes the signal through the Power Detector Circuit to the Receive Audio Module. In the Duplex Mode, the Duplex Module output is attenuated a total of 50 dB, then routed to the T/R Connector. In the Generate Mode, the Output Amplifier amplifies the signal received from the IF Block, routes it to the Step Attenuator, which returns it to the Output Amplifier for output to the T/R Connector.

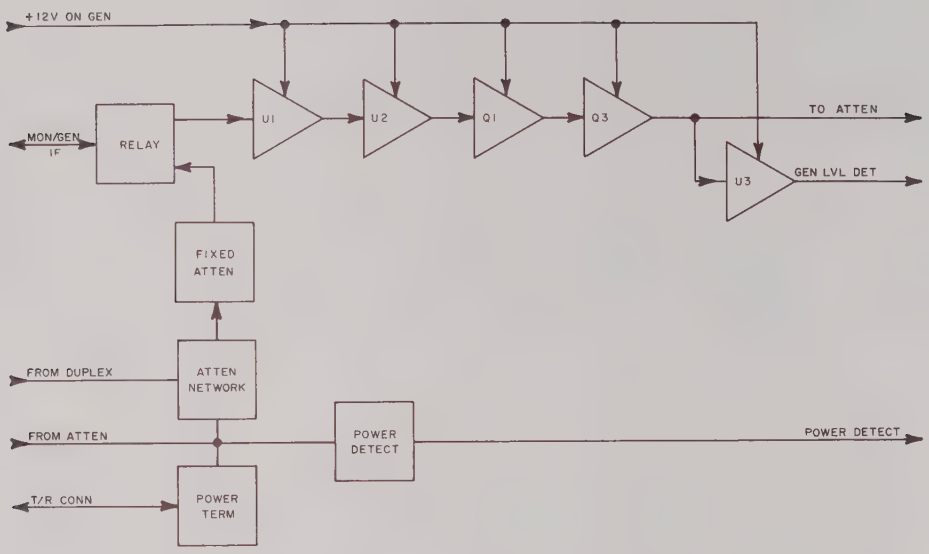


Figure 2-22 Output Amplifier Module Block Diagram

A. Receive Mode

In the Receive Mode, the output Amplifier Module couples any signal received at the T/R Connector through RN5101, where it is attenuated 20 dB. The signal is then split, with one signal going to the power detector circuit consisting of CR5108, C5124, trimcap C5127, L5107, R5128, R5129, R5134 and R5147. The Detector Circuit converts this signal to a DC voltage level corresponding to the signal power and supplies the result to the Receive Audio Module. The other signal is attenuated an additional 60 dB for a total of 80 dB attenuation by a series of voltage dividers using R5135 through R5146 and is then routed by relay K5101 through J5101 to the IF Block.

B. Generate Mode

In the Generate mode, +12V energizes mode relay K5101 and enables the generate amplifier and level detector circuits. The relay couples the RF signal from the IF Block to the amplifier circuit. Two amplifiers, U5101 and U5102, amplify the signal and apply it to the base of RF transistor Q5101 which, in turn, controls the base of RF transistor Q5103. Q5102 is a bias transistor used to adjust the base current of Q5103 to achieve a constant collector current in Q5103. The signal level at this point is nominally 0 dB. From the collector of Q5103, the signal is coupled through J5103 to the GEN LEVEL Step Attenuator and through CR5102 to the generate level detector circuit.

The Step Attenuator, while not a physical part of the Output Amplifier Module, is electrically an integral component. It attenuates the generated signal from 0-100 dB in 10 dB steps, allowing operator control of the signal level. (Vernier control from +1 to -11 dB is achieved by varying the signal. From the Step Attenuator, the signal is returned to the Output Amplifier where it is attenuated an additional 20 dB. The signal is then routed to the T/R Connector.

CR5102 and C5116 form a level detector which senses the level from Q1503. Amplifier U5103 then sends an analog DC signal to the Generate Audio PC Board. The AM modulation circuit uses this signal to adjust the modulator/leveler attenuator in the 10.7 MHz Gen/Rec Module, thereby affecting the level of the generated signal which is ultimately applied to the Output Amplifier. Trimpot R5114 allows calibration of the output from U5103 as necessary to obtain a level of 0 dB at J1503.

C. Duplex Mode

In the Duplex Mode, a -35 dBm signal from the Duplex Module is attenuated a total of 50 dB by the Output Amplifier, then routed through J5104 to the T/R Connector.

2-4-18 DUPLEX/TRACKER (FM/AM-1200S)

In the Duplex mode, the Duplex/Tracker utilizes two local oscillators, one an FM Modulator source at 310 MHz and the other with a frequency range from 350 MHz to 450 MHz as determined by the selected offset frequency. These two frequencies are combined at the second mixer, MXR12002, and the 40-140 MHz difference is selected. One signal is returned to the ÷64/÷65 Prescaler where it is prescaled from the Phase-Lock Loop. The Phase-Lock Loop internally divides the 20 kHz reference by 8 and compares the two signals. The other 40-140 MHz signal is mixed with the High Loop Module 90-1090 MHz Local Oscillator output in the third mixer, MXR12003. The signal from MXR12003 is then split, with one signal going to J12004 for output to the Output Amplifier. The other signal is routed to a Duplex/Track Level Select circuit, then output through J12003 to either the Duplex Connector or the Track Amp (Option 12), if installed.

In the Track Mode, available only with Option 12 installed (Tracking, software version 3.0-01 and Track Amp), a 105.3-117.3 MHz signal from the Analyzer RF Local Oscillator is received at J12005 and used as the swept input for the 1st Mixer, MXR12001. The tracking frequency is mixed with the Analyzer RF at MXR12001 and the difference is routed through an 89 MHz center, 12 MHz bandwidth Bandpass Filter to MXR12003. The output of MXR12003 is then split, with one signal going to J12004 for output to the Output Amplifier. The other signal is routed to the Duplex/Track Level Select circuit, then output through J12003 to the Tracker Amp.

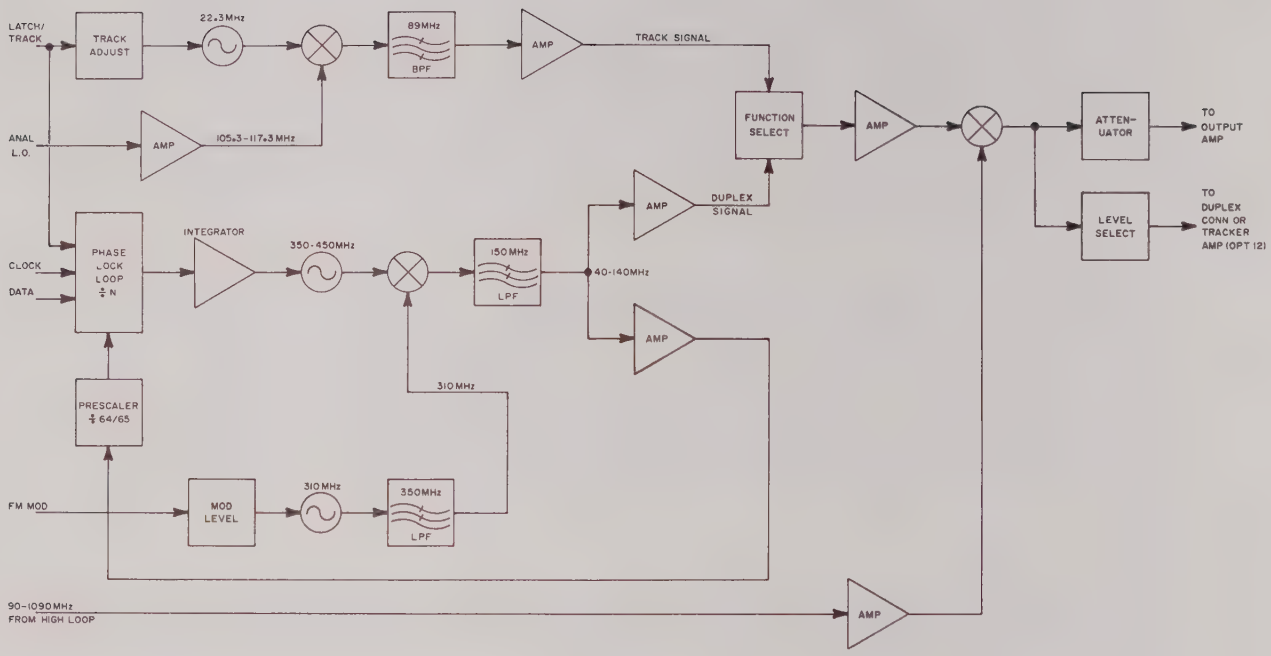


Figure 2-23 Duplex/Tracker Module Block Diagram (FM/AM-1200S)

A. Duplex Operation

1. 350-450 MHz Oscillator Circuit

In the Duplex Mode, a 20 kHz reference signal from the Digital Module is used in the ÷N Phase-Lock Loop, U12003, for comparison to the output signal of the ÷64/÷65 prescaler, U12004. This comparison is output through pin 6 of U12003 to pin 14 of U12007A for use in feeding correction voltage (error signal) to pin 6 of Integrator, U12008B. The integrator, which is held at a fixed bias by CR12002, R12032, R12033 and C12038 through pin 5, applies its correction voltage output through pin 7 to the 350-450 MHz Oscillator circuit (Q12006, CR12003, CR12005 and related components).

The frequency of the 350-450 MHz Oscillator, as determined by the programmed offset selected, is applied to pin 1 of integrated amp, U12009, which serves as a power driver, and is output to MXR12002.

2. 310 MHz Oscillator Circuit

FM information, received from pin 14 of J12001 is routed through R12067, the calibrated FM Level Adjust, to the 310 MHz Oscillator (Q12011, CR12010, CR12009 and related components). The Oscillator's output is routed through a 350 MHz Low-pass Filter (L12018 thru L12020, C12076 thru C12080 and R12074) to pin 1 of mixer MXR12002.

3. Mixer MXR12002

Mixer MXR12002 mixes the frequencies of the 350-450 MHz Oscillator and the 310 MHz Oscillator and outputs the resulting difference of 40-140 MHz through a 150 MHz Low-pass Filter (L12012 thru L12014, R12090, C12052 thru C12055). The signal is then split, with one signal going through amplifier Q12008 to the ÷64/÷65 prescaler, U12004, to provide output correction (error signal) through the Phase-Lock Loop, U12003. The other signal is used for a part of the Duplex Output signal.

4. Duplex Output

The 40-140 MHz output signal from MXR12002 is amplified through Q12007 and routed through CR12007 to the Duplex Level Adjust circuit (Q12009, R12052 thru R12057, R12048, C12062 thru C12065) and routed to the IF input of MXR12003. The LO input to MXR12003 is the selected 90-1090 MHz High Loop Local Oscillator output received through J12002 of the Duplex/Tracker module and amplified through U12010.

The output of MXR12003 is the programmed ±50 MHz offset generated signal off the selected receiver frequency. This output is then split, with one signal going to J12004 for relay through the Output Amplifier to the T/R Connector on the front panel. The other signal is routed to the Duplex/Track Level Select Switch, K12001, controlled through Q12010 from pin 14 of U12003. In the Duplex Low Mode, this signal is routed through a 25 dB pad and output at a -40 dBm level to J12003. In the "Duplex High" Mode, the signal is routed to J12003. In the "Duplex High" Mode, the signal is routed without adjustment through K12001 to J12003 at a -15 dBm level.

B. Tracker Operation

1. Analyzer RF Sweep

The sweep range of the Spectrum Analyzer as selected on the front panel of the FM/AM-1200S, determines the frequency of the 105.3-117.3 MHz signal received at J12005 of the Duplex/Tracker Module. This signal is amplified by Q12001 and used to sweep MXR12001.

2. Track Adjust

Data for the Tracking Operation of the Duplex/Tracker module is received as a 20-bit word. Seventeen bits of this information is the Duplex Data. Of the remaining bits, one bit, relayed through U12003 pin 14, is an enabling bit which selects either the Tracking Power Supply (U12005, C12033, C12034, R12025, R12026) or the Duplex Power Supply (U12006, R12027, R12028, C12035 and C12036); one bit, relayed through U12003 pin 15, selects output level selection through K12001; the twentieth bit enables the Track Adjust. This bit is activated when the operator presses either the right or left arrow key on the FM/AM-1200S keyboard while in the Track Mode. The Track Adjust bit enables U12002A through pin 2, which in turn disables the clock information normally received through U12002A pin 3. The Track Adjust enable information is in turn passed from U12002A pin 5 to U12002B, pin 12 and causes the charge on pin 8 of U12002B to go low. This in turn, enables the digitally controlled potentiometer, U12001, to act as a voltage divider. By continuing to press or hold down the right or left arrow key on the FM/AM-1200S front panel, the resistance through U12001 is increased or decreased accordingly. This changes the capacitance of Varactor CR12001 and allows the operator to "fine tune" Oscillator, Y12001, for maximum amplitude of the Tracking signal.

3. Tracking Signal

The output of the 22.3 MHz Oscillator circuit (Y12001, Q12003, CR12001 and related components) is used as the IF input of MXR12001. MXR12001 mixes the 105.3-117.3 MHz signal from the Analyzer RF with the 22.3 MHz signal from the oscillator and produces 83-95 MHz output through a 12 MHz Bandwidth, 89 MHz Center Bandpass Filter (T12001 thru T12004, L12001 thru L12003, C12005 thru C12009). This in turn, sends the signal to the Track Level Adjust circuit.

4. Tracking Output

The Track Level Adjust circuit (R12005 thru R12010, C12010, C12011 and Q12002) is used to calibrate the tracking output level. The signal passes through CR12006 and the Duplex Level Adjust circuit to the IF input of Mixer MXR12003. Then LO input of MXR12003 is the selected frequency of the High Loop Local Oscillator (90-1090 MHz) received at J12002 of the Duplex/Tracker module and amplified through U12010.

The output of MXR12003 is split, with one signal going to J12004 for relay through the Output Amplifier to the T/R Connector on the front panel. The other signal is routed to the Duplex/Track Level Select switch, K12001, controlled through Q12010 from pin 15 of U12003. In the Track Low Mode, this signal is routed through a 25 dB pad and output at a -40 dBm level to J12003. In the Track Med or Track High Mode, the signal is routed without adjustment through K12001 to J12003 at a -15 dBm level.

C. Tracker Amp

The Tracking signals from J12003 are routed to the Tracker Amp for further amplification if in the Track High mode and then routed to the Duplex Port on the FM/AM-1200S front panel.

1. Track Low and Track Medium Mode

Tracking information from the Duplex/Tracker Module is received at J70001 of the Tracker Amp. When the FM/AM-1200S is in the "Track Low" or "Track Med" Mode, these signals are routed through K60001 with no modification directly to J70002 for output to the Duplex Output connector on the FM/AM-1200S front panel.

2. Track High Mode

In the "Track High" Mode of operation, a +5V received through J70003 from the Motherboard activates the Tracker Amp by tripping the switching circuit (Q60001, Q60002, CR60001, R60001 thru R60003) which changes the routing of the Tracking signal through K60001. The tracking signal in the "Track High" Mode is routed through the Tracker Amplifier circuitry (U60001, U60002, L60002, L60003, R60004 thru R60008, C60003 thru C60006) which amplifies the Tracking signal, then routes it back through K60003 for output through J70002 at a -6 dBm level.

2-4-18a DUPLEX MODULE (FM/AM-1200A)

To produce the duplex RF signal, the Duplex Module uses two local oscillators. The frequency offset command, received from the processor, adjusts one VCO frequency through the phase-lock circuit. The modulated FM audio signal from the 10.7 MHz Gen/Rec Module modulates the other VCO frequency. The two output frequencies are mixed, with the difference frequency being mixed with the Dual VCO difference frequency. The final frequency is an FM signal at the selected RF plus or minus the selected offset frequency.

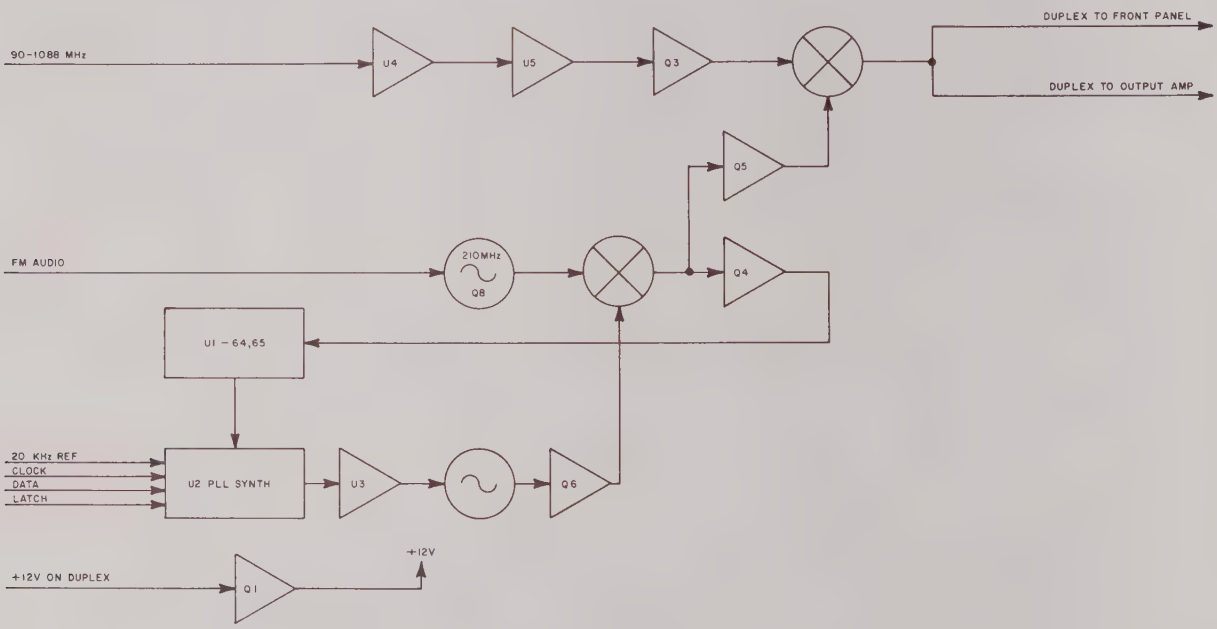


Figure 2-23a Duplex Module Block Diagram

A. Subregulator

The +12V VDC from the Power Supply is subregulated on the Duplex PC Board to operate the oscillators and phase-lock network. Zener diode CR1205 establishes the reference voltage for op amp U1206A. The output of U1206A is applied to the base of transistor Q1202. The collector voltage from Q1502 is sampled by U1206A through a voltage divider consisting of trimpot R1251 and resistors R1252 and R1253. Thus, U1206A changes its output as necessary for Q1202 to hold the collector voltage at the level required to balance the voltages at the input pins of U1206A.

B. 250-350 MHz Oscillator

The oscillator operating voltage is applied through RF choke L1212 to FETs Q1207 and Q1209. Varactor CR1202 and inductor L1211 form a tank circuit. The tuning voltage from the phase-lock integrator U1203B, isolated through R1246 and L1215, establishes the frequency of the oscillator. Diode CR1204, installed between the source and the gate of the two parallel FETs, provides AGC for the oscillator. The output signal passes through RF choke L1210, and is coupled by C1258 to the base of Q1206. Q1206 amplifies the signal to approximately +7 dBm, then C1257 couples the signal to the LO port of MXR1202.

C. 210 MHz Oscillator

The oscillator operating power of +11 VDC is supplied through R1222. Variable RF choke L1209 tunes FET Q1208 to 210 MHz. The modulated FM audio signal from the 10.7 MHz Gen/Rec Module is applied to varactor CR1201 to modulate the frequency of the oscillator. Diode CR1203, between the source and the drain of Q1208, provides AGC for the oscillator. RF choke L1208, provides circuit isolation, and L1207, L1213, C1242, C1243 and C1276 form a low-pass filter. R1228 and R1229 form an impedance matching pad for the RF port of MXR1202.

D. Offset Mixer and Filter

Mixer MXR1202 combines the frequencies from the 210 MHz VCO and the 250-350 MHz VCO. The combined signal is then filtered by a 150 MHz low-pass filter to pass only the difference frequency of 40-140 MHz. The filter consists of L1205, L1206, L1214, C1250, C1251, C1252 and C1277. From the mixer, the signal is applied to the phase-lock circuit and the duplex mixer circuit.

E. Phase-Lock Circuit

The 40-140 MHz signal from the offset mixer and filter is coupled through C1249 to transistor Q1204. The amplified signal is coupled through C1248 to dual modulus prescaler U1201. As long as pin 1 is low, U1201 divides by 65; when the control line from U1202 pin 8 to U1201 pin 1 is high, U1201 divides by 64. The output frequency from U1201 is applied to the frequency input pin of U1202.

U1202 is a serial input PLL frequency synthesizer that divides the input frequency by a programmed number from the processor, compares the result with the 20 kHz reference from the Digital Module, and produces two VCO steering voltages. When the offset signal is at the selected frequency, both control voltages from pins 3 and 4 of U1202, are high. One pin will be low, depending upon phase relationship, when the offset frequency is not phase-locked to the reference frequency.

Both control voltages from U1202 are applied to an integrator consisting of op amp U1203B and associated components. R1216 with C1228, and R1217 with C1227 are differentiating circuits to shape the square wave control signals into basically sawtooth waves. R1220, C1229 and C1264 from the output of U1203B to pin 6, and R1221, C1226 and C1274 from pin 5 to ground, slow the phase-lock response sufficiently to prevent cancellation of FM applied to the 210 MHz oscillator. The output of the phase-lock circuit at pin 7 of U1203B is applied to the tuning circuit of the 250-350 MHz oscillator.

F. Duplex Mixer Circuit

The 40-140 MHz offset signal, received from the offset mixer and filter, is amplified by Q1205. The output level is then calibrated by trimpot R1230 and applied to the IF port of MXR1201. The 90-1088 MHz signal from the High Loop is amplified by op amps U1204 and U1205 and transistor Q1203, and applied to the LO port of MXR1201. Power for the amplifiers is supplied by Q1201 when DUPLEX is selected on the MODE Control. The output from the RF port of MXR1201 is attenuated to -30 dBm for the Output Amplifier by R1209, R1210, R1213, and to -60 dBm for the DUPLEX Connector by R1208, R1209, R1211, R1212 and R1214.

2-4-19 RECEIVE AUDIO PC BOARD

An AGC circuit samples the AM audio level received from the 10.7 MHz Gen/Rec Module. It produces the control voltage for the AGC amplifiers in the 10.7 MHz Gen/Rec module and supplies the comparative signal to break squelch. Either FM or AM audio, as selected by the MODE Control, passes through the squelch gate multiplexer to one of three low-pass filters, 80 kHz, 12 kHz and 250 Hz. The filtered audio is then sent to the filter select multiplexers.

One multiplexer selects either the 80 kHz or 12 kHz filter output for signal routing. The signal then exits the Receive Audio PC Board on pins 2 and 9 of J63002 and is either bandpass filtered or non-filtered on the Interface I/P PC Board (FM/AM-1200S only). The signal returns to the Receive Audio PC Board on pins 4 and 7 of J63002 and continues through a range select circuit to the meter function circuit, which are controlled by the METER Control. The signal is then supplied to the Modulation Meter and the Digital Display.

The second multiplexer selects either the 12 kHz or 250 Hz filter output, which is fed to the Audio/SINAD switching network to the Generate Audio Module. When either SINAD or DIST is selected on the METER Control, any signal applied through the EXT MOD/SINAD Connector is switched into the audio circuit, which disconnects the internal audio signal. The selected signal is then returned to the Receive Audio Module. An AGC circuit controls the signal level and feeds into the Digital Module for frequency counting, and to the SINAD/Distortion circuit. The signal is then coupled through the meter function circuit for display on the Modulation Meter and on the Digital Display.

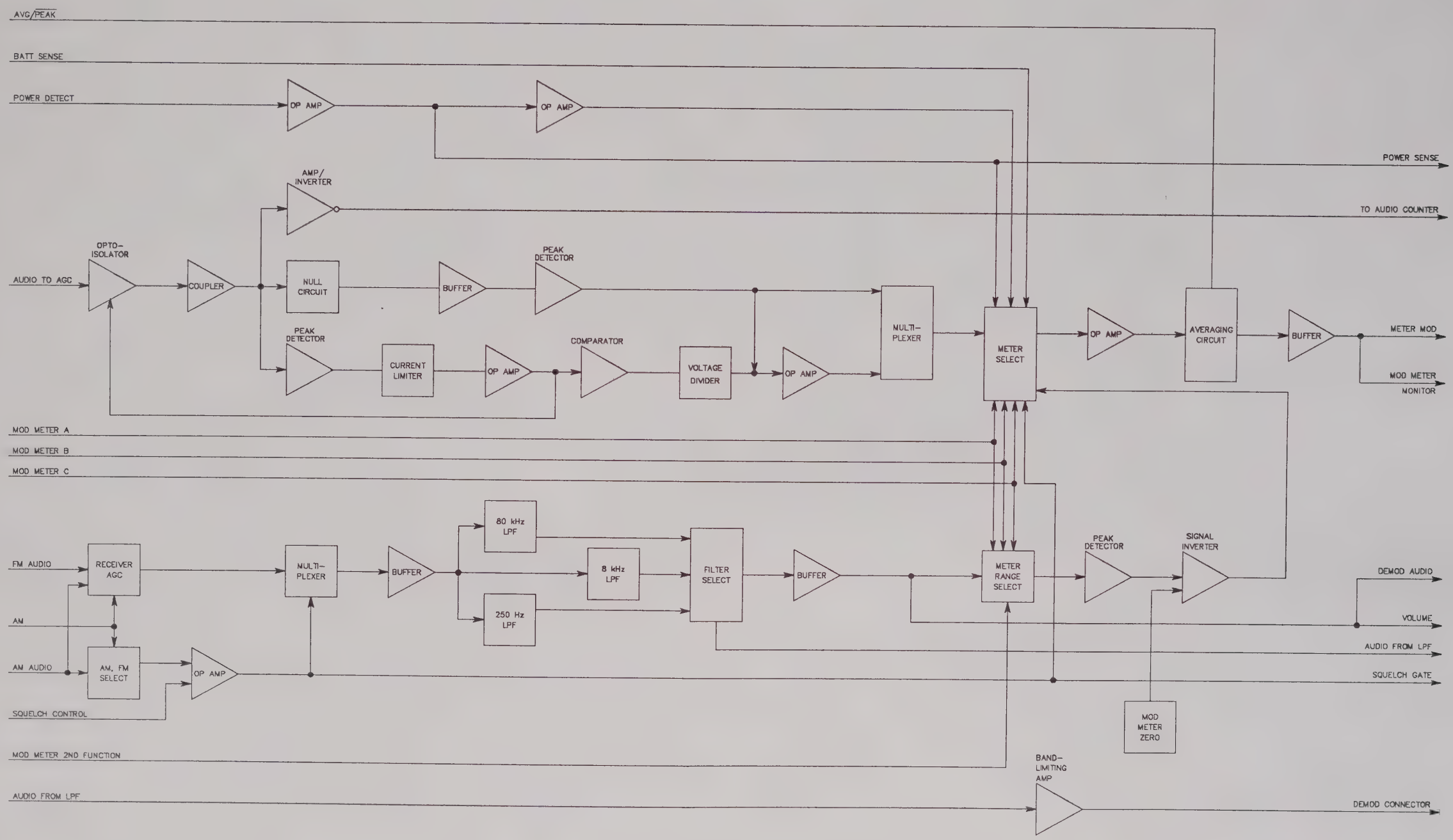


Figure 2-24 Receive Audio PC Board Block Diagram

A. Signal Control Circuit

The AM audio signal received from the 10.7 MHz Gen/Rec Module represents the carrier amplitude for FM, carrier amplitude plus audio modulation for AM, and Generator VCO amplitude plus audio modulation for SSB. This signal is applied through R63002 to op amp U63002A, which sets reference level approximately to 1.8 VDC by R63005 and R63007. When SSB is selected, multiplexer U63001C couples R63006 and CR63001 in parallel with R63002. When AM or SSB is selected, multiplexer U63001A couples C63004 in parallel with C63001. Thus, the slew rate for U63002A is set by R63002 and C63001 for FM, R63002, C63001 and C63004 for AM, and R63002, R63006, C63001 and C63004 for SSB. This allows U63002A to respond to the carrier amplitude, but not to audio modulation.

If the amplitude of the signal reaching U63002A is below the reference level, the output is a positive high, which is applied to the AGC amplifiers in the 10.7 MHz Gen/Rec Module, for maximum amplification of the RF signal. This results in an increased level to U63002A. When the signal equals the reference level, the output becomes negative, reducing the amplification by the AGC amplifiers, The stronger the RF received, the less amplification required. The result is a more negative output from U63002A and minimal AGC amplification.

CR63002 allows the negative output of U63002A to be applied to op amp U63003A, which buffers and inverts the signal. The output of U63003A goes to the meter function multiplexer, U63013, and to op amp U63002B. The reference voltage for U63002B is set by the SQUELCH Control. When the applied signal level exceeds the reference, U63002B supplies a high, which enables multiplexer U63022C to route the signal to the Digital Module.

The FM and AM audio signals are applied through trimpots R63083 and R63079, respectively, to multiplexer U63001B. The control voltage to U63001B is high when AM or SSB is selected on the MODE Control. In GEN Mode, +12 VDC is adjusted at R63136 (GEN AM % CAL). The selected audio signal is coupled through U63022C, when squelch is broken, to buffer U63018B. From U63018B, the signal is applied to three low-pass filters.

B. Low-Pass Filters

The three low-pass filters are identical except for resistance and capacitance (R-C) values. The low-pass filters are two-stage R-C networks with buffering following each stage to provide isolation.

The 80 kHz filter consists of resistors R63085 through R63088, capacitors C63015 through C63018, and op amps U63019A and U63019B. The output from U63019A is applied to multiplexer U63022A.

Resistors R63089 through R63092, capacitors C63019 through C63022 and op amps U63020A and U63020B form the 12 kHz filter. Its output is applied to U63022A and U63022B.

The 250 Hz filter uses resistors R63093 through R63096, capacitors C63023 through C63026 and op amps U63021A and U63021B. The output from U63021A is applied to U63022B and routed to the Generate Audio Module via pin 1 of J63001.

Selecting a signal of 409.6 Hz or less on the Variable Tone Generator activates pin 3 of J63001, which switches U63022B to the 250 Hz filter. The signal from U63020 is coupled through U63022A and sent via pins 2 and 9 of J63002 to the Bandpass Filter on the Interface PC Board. When FM WIDE is selected, pin 12 of J63001 is activated, causing the signal to be switched to the 80 kHz filter.

C. Range Select

The audio signal from the Bandpass Filter on the Interface PC Board is returned to pins 4 and 7 of J63002. The input at pin 4 of J63002 is band limited at U63026 by C63049. The amplified output is sent to the DEMOD Connector via pin 26 of J63001.

The input at pin 7 is buffered by op amp U63018A, which sends the signal through the VOLUME Control via pin 17 of J63001 to the speaker amp in the Generate Audio Module, through R63099 to range select multiplexer U63016, for the 2 kHz/10% range, and through a voltage divider consisting of R63100, R63101, R63104 and R63132 for additional range selection.

The 6 kHz/60% range taps the signal between R63100 and R63101 and goes directly through U63016. The 20 kHz/200% Range taps the signal between R63101 and R63104 to pin 12 of multiplexer U63024A. The 6 kHz/60% range taps the signal between R63104 and R63132 before it goes through pin 13 of U63024A. U63024A normally couples the 20 kHz/200% range to U63016; however, when the 6 kHz/60% range is selected on the METER Control, pin 28 of J63001 is activated, which enables U63024A to select the 6 kHz/60% range. The selected signal from U63024A is fed through pin 15 of U63016. The output of U63016 is coupled through buffer U63014A to a peak detector consisting of dual op amp U63015A and U63015B, and associated components.

The output from U63015B is a negative DC voltage equal to the peak voltage of the selected test signal, which is applied to the inverting side of op amp U63023B.

U63010, R63068 through R63071, R63121 through R63124 and U63017 make up a selectable voltage divider network for zero reference levels during modulation measurements. U63010 selects one of four pots (R63068 through R63071) to supply the voltage divider

(R63121 through R63124). U63017 selects the appropriate voltage for the desired modulation range. The selected range is then applied to the non-inverting input of U63023B. The output of U63023B is proportioned to the positive DC level, at selected ratios, to the audio signal level received at the Receive Audio Module.

D. AGC Circuit

The signal from the Audio/SINAD switching circuit in the Generate Audio Module is AC coupled by C63029, through opto-isolator U63004, to op amp U63005A. The output of U63004A goes three places: to the SINAD/Distortion circuit; to op amp U63008, where it is amplified, inverted and routed to the audio counter in the Digital Module; and through C63010 to op amp U63009A.

Op amps U63009A, U63009B and associated components, form a peak detector. The signal is applied to the inverting input of U63009A. CR63007 couples the positive component to the non-inverting input of U63009B, and CR63008 couples the negative component to the inverting input. The output from U63009B is a positive DC voltage equal to the peak voltage of the input signal.

R63026 applies -12 VDC to the inverting input of op amp U63005B, which applies positive output to the SINAD/Distortion circuit and to the LED in opto-isolator, U63004. As the LED increases in brilliance, the resistance in U63004 decreases, decreasing attenuation of the test signal, resulting in greater gain through U63005A. The positive DC level from U63009B is summed with the -12 VDC at R63026, reducing the negative DC level applied to U63005B. When U63005B output decreases, the brilliance of the LED in U63004 is also reduced, which then increases in resistance and ultimately decreases the gain at U63005A. C63005 establishes the slew rate of U63005B, while CR63006 limits its output to 0.6 VDC in the event the test signal level exceeds the AGC controllable level.

E. SINAD/Distortion Circuit

The signal received from op amp U63005A passes through an R-C notch filter consisting of C63006, C63007, C63027, C63028, R63017 through R63023 (R63018 and R63020 are trimpots), and buffer op amp U63006B. The filter is tuned to reject only a frequency of 1000 Hz (1 Hz at -50 dB). From U63006B, the signal is routed to the Oscilloscope for video presentation, and to a peak detector for meter display. The peak detector consists of op amps U63007A and U63007B and associated components.

The signal enters the inverting input of U63007A. The positive component of its output is coupled through CR63010 to the non-inverting input U63007A and the negative component is coupled through CR63011 to the inverting input. The output of U63007B, a positive DC voltage proportional to the signal level from the notch filter, is calibrated by trimpot R63050. It is then applied to the low-enabled input of multiplexer U63024B and through op amp U63023A for input to U63024B. From U63024B, the signal is applied to multiplexer U63013.

The input to the SINAD/Distortion circuit from op amp U63005B is applied to the non-inverting input of comparator op amp U63006A, which supplies reference voltage through voltage divider resistors R63042 and R63043. If the test signal level at opto-isolator U63004 is insufficient to reduce the output of U63005B to approximately 9 volts, or less, U63006A combines a high positive DC level with the output of the peak detector to "peg" the meter.

F. Power Monitor

The DC voltage from the power detector in the amplifier is applied to op amp U63012B. When no signal is present from the output amplifier, R63045 applies negative bias to U63012B. The negative reference voltage from R63055 is applied to the inverting input of U63012B, with trimpot R63054 used to calibrate hysteresis. CR63013 limits the output to a positive level. The output from U63012B is fed the operating mode circuit in the Generate Audio Module and the power monitoring circuits in the Receive Audio Module. R63060, R63061 and trimpot R63062 furnish 150W to multiplexer U63013. For the 15W power supply, the signal is amplified by op amp U63012A, then divided by R63066, R63067 and trimpot R63065 before it is applied to U63013.

G. Meter Function Circuit

All signals displayed on the Modulation Meter are routed to multiplexer U63013. Battery voltage input can be adjusted at R63003 (BATT CAL). The output of U63013 is applied directly to the low-enabled pin of multiplexer U63024C and through an averaging circuit, consisting of op amp U63011 and associated components, to the high-enabled point of U63024C. From U63024C, the signal is buffered by op amp U63014B, before it is output to the Modulation Meter and the DVM I/O PC Board.

2-4-20 ANALYZER RF MODULE (FM/AM-1200S ONLY)

The IF signal received from the IF module is passed through a bandpass filter, mixed with the output of a sweep oscillator, and filtered a second time, to 22.3 MHz. Between sweeps, the oscillator output is mixed with the output frequency of the Low Loop Module. The difference frequency is phase-locked to a 1 MHz reference from the

Frequency Standard to establish a center frequency for the sweep, which changes according to the Low Loop Frequency. The sweep control voltage then causes the oscillator to sweep from below to above its center frequency. An onboard subregulator circuit provides +11V, -11V and +6.9V.

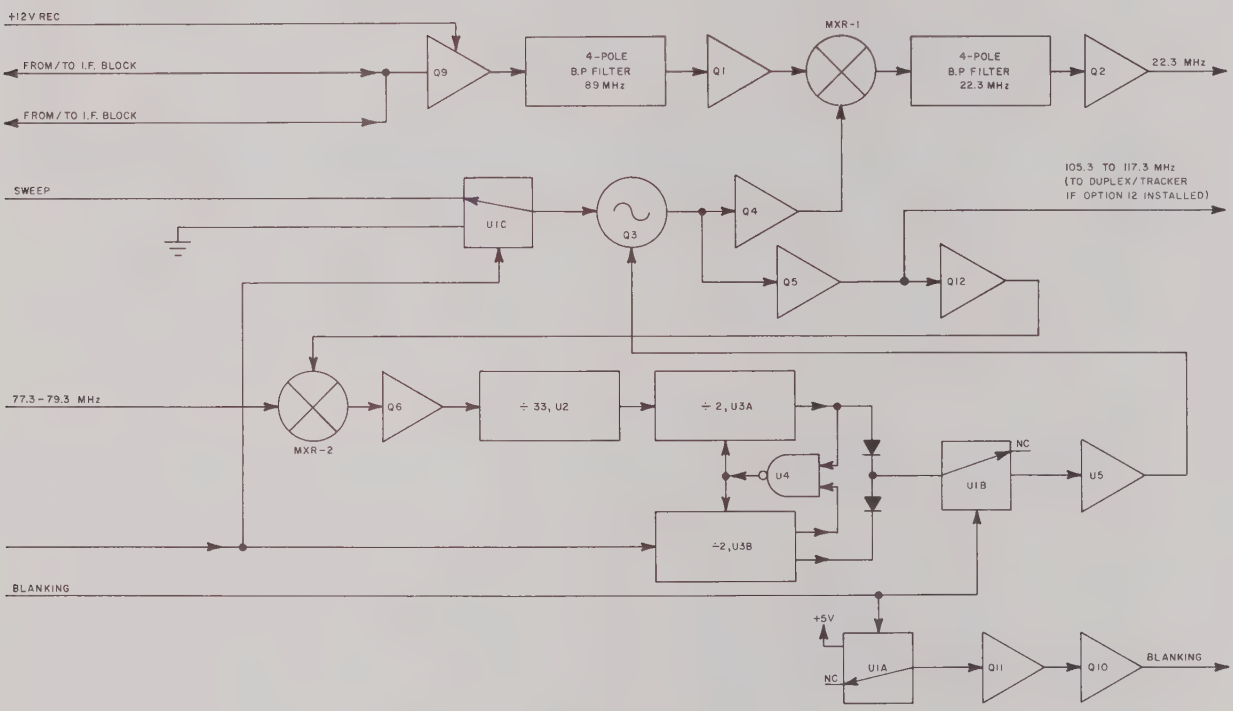


Figure 2-25 Analyzer RF Module Block Diagram

A. Subregulator Circuit

The +11V subregulator consists of emitter-follower Q407, op amp U406, +6.9 V reference zener diode CR406, and a voltage divider using R441, R442 and trimpot R443 to sample the collector voltage of Q407 for comparison to the reference.

The -11V subregulator, which is similar to the +11V subregulator, consists of op amp U407, emitter-follower Q408 and a voltage divider using R439, R440 and trimpot R451. U407 uses +11V as a reference, and the supply is -12V.

Zener diode CR401 and resistor R410 reduce the regulated +11V to +6.9V for the sweep oscillator and phase-lock circuits. Zener diode CR407 and resistor R463 reduce the +12V supply to +5V.

B. Sweep Oscillator Circuit

FET Q403 is tuned by variable inductor L415 and varactor CR402 to oscillate at a center frequency of 110.3 to 112.3 MHz. The phase lock circuit control voltage applied to CR402 varies the center frequency according to the Fast Low Loop output frequency when an analyzer blanking signal is applied. When the blanking signal is removed, multiplexer U401C applies the sweep control voltage to the tuning circuit. This voltage, which is a ramp starting negative and progressing to equally positive, pulls the frequency below center, then drives it equally above center. The next blanking signal opens the sweep control line and snaps the oscillator back to center frequency. The output level of Q403 is controlled by CR403. The signal is then filtered by L416, C423 and R421, coupled through C424 and C430 to buffers Q404 and Q405 respectively. From Q404, the signal is applied to IF Mixer MXR401; from Q405, the signal is further buffered by Q412, then applied to MXR402 in the phase/frequency comparator circuit. In FM/AM-1200S, the output from Q405 is tapped at R462 and routed through R466 to J407 for output to the Duplex/Tracker Assembly when the Tracking Generator (Option 12) is installed.

C. Phase/Frequency Comparator Circuit

MXR402 mixes the output of the sweep oscillator with the 79.3 to 77.3 MHz output from the Low Loop. A low-pass filter consisting of L418, L419, C434, C435 and C436 then passes the difference frequency to a tuned amplifier, Q406. A tank circuit consisting of L421 and C450, tunes the collector at Q406 to 33 MHz, which is the difference between the sweep oscillator center frequency of 112.3 to 110.3 MHz and the Low Loop frequency of 79.3 to 77.3 MHz. Prescaler U402 is programmed to divide by 33, producing a 1 MHz output. The 1 MHz output from prescaler U402 clocks flip-flop U403A and the 1 MHz reference clocks U403B. The corresponding Q outputs of the flip-flops are connected to pins 9 and 10 of NAND gate U404C, with the gate output from pin 8 applied to reset both flip-flops. The Q output of U403A charges capacitor C443 through diode CR404. The $\overline{Q}$ output from U403B discharges C443 through CR405. Thus, if the two input frequencies are in phase, the charge on capacitor C443 stays constant. However, if the inputs are not in phase, the charge on C443 is a DC correction voltage to pin 4 of multiplexer U401B. During analyzer blanking, multiplexer U401B couples the voltage level at C443 to op amp U405.

U405, C444 and associated components form a sample-and-hold integrator circuit for tuning the center frequency of the oscillator. During blanking, the only tuning voltage is from U405, which is applied to varactor CR402. During sweep, U405 receives no input from the phase comparator, so C444 stores and holds the previous level. This allows U405 to continue, during the sweep, to furnish the same voltage as during the preceding blanking period, causing CR402 to hold this level as the center frequency level while the sweep voltage varies the frequency during the sweep period. During the next blanking period, U405 resets the center frequency control voltage and returns the oscillator to that frequency, and the charge level of C444 is adjusted accordingly for the next sweep.

D. IF Mixer Circuit

In the generate mode the 89 MHz signal from the IF Module enters at J406 and is attenuated by R454 to prevent overdriving the analyzer display. In the receive mode, +12V from the Generate Audio Module turns on Q409, which allows the 83-95 MHz signal to bypass R454. In either mode, the signal is then coupled to a 4-pole, 12 MHz bandpass filter, consisting of FL401 through FL404 and associated components. The signal is then amplified by Q401, and mixed with the sweep oscillator signal in MXR401. A 22.3 MHz IF bandpass filter, consisting of FL405 through FL408 and associated components, then passes only the 22.3 MHz signal. From the 22.3 MHz IF bandpass filter, the signal is amplified by Q402, then coupled to the Analyzer IF Module through J401.

E. Oscillator Blanking Circuit

Power for the 33 MHz oscillator in the Analyzer IF Module is supplied through Q410 for control purposes. When the analyzer blanking signal is applied at pin 12 of J402, it enables multiplexer U401A, applying +5V to Q411. This turns on Q411, which pulls down on the base of Q410, shutting off the oscillator power.

2-4-21 ANALYZER IF MODULE (FM/AM-1200S ONLY)

The Analyzer IF Module mixes the 22.3 MHz signal from the Analyzer RF Module with 33 MHz from a local oscillator to produce a 10.7 MHz IF. The signal is then filtered to a 3 kHz or 300 Hz bandwidth for narrow dispersion selections before being mixed with a 9.5 MHz signal from a second local oscillator. A low-pass filter then passes the 1.2 MHz difference frequency for amplification which is applied to the Analyzer Log Amp Module.

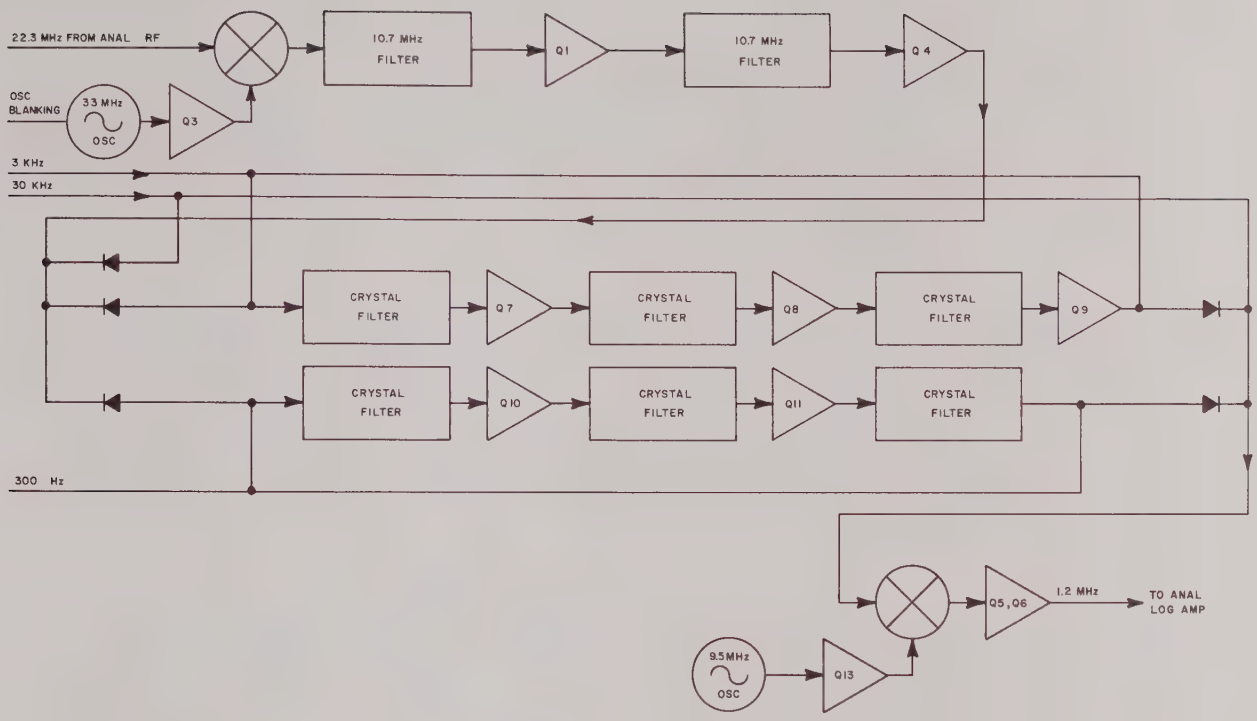


Figure 2-26 Analyzer IF Module Block Diagram

A. 33 MHz Oscillator

The 33 MHz oscillator contains Q502, 33 MHz crystal Y501 and associated components. +12 volts from Q410 in the Analyzer RF Module is applied to the 33 MHz oscillator. As Y501 oscillates at its resonant frequency, the signal is amplified by Q502. The pulses produced at the emitter of Q502 are applied to the base of Q503. Q503 then buffers the 33 MHz for MXR501. When blanking occurs, the oscillator power is interrupted, which disables the 33 MHz oscillator.

B. 10.7 MHz Mixer Circuit

A low-pass filter consisting of C575, C579, and L517, filters any induced RF from the VCO in the Analyzer RF Module from the 22.3 MHz IF. MXR501 then combines the 22.3 MHz IF with the 33 MHz level oscillator output producing the 10.7 MHz IF. The 10.7 MHz IF then passes through a 4-pole, 600 kHz bandpass filter consisting of FL501 through FL504, is amplified by Q501, then filtered by a second 4-pole, 600 kHz bandpass filter consisting of FL505 through FL508.

C. Bandwidth Filter Circuit

When a dispersion range of 50 kHz or greater per division is selected on the HORIZONTAL Sweep Control, +12V is applied to forward bias CR504 and CR507, coupling the 10.7 MHz IF from Q504 directly to MXR502. CR505, CR506, CR508 and CR509 are reverse biased to isolate the 300 Hz and 3 kHz filters. 30 kHz bandwidth filtering for these dispersion selections is in the Analyzer Log Amplifier Module.

For dispersion selections of 5 kHz, 10 kHz and 20 kHz per division, +12V is applied to forward bias CR506 and CR508 and reverse bias CR504, CR505, CR507 and CR509, directing the signal through the 3 kHz filter. The three-stage filter circuit contains three crystals, YFL501, YFL502 and YFL503, each with two trimcaps for signal amplitude and shape, followed by amplifying transistors, Q507, Q508 and Q509, respectively. Trimpot R543 adjusts the total gain of three transistors to compensate for filter losses.

When the HORIZONTAL Sweep Control is in the 1 kHz or 2 kHz per division dispersion position, +12V forward biases CR505 and CR509 and reverse biases CR504, CR506, CR507 and CR508 to direct the signal through the 300 Hz filter. This circuit contains six matched crystals, YFL504 through YFL509, in three paired stages. A fixed amplifier, using Q510, follows the first stage and an adjustable amplifier, using Q511 and trimpot R559, follows the second stage. Total gain from the amplifiers is adjusted to compensate for filter losses.

D. 9.5 MHz Oscillator Circuit

Y511 is a 9.5 MHz crystal which controls the base voltage of Q512. The signal produced, is amplified by Q513 and coupled through C553 to MXR502.

E. 1.2 MHz Mixer Circuit

MXR502 combines the 10.7 MHz IF signal with the 9.5 MHz signal. A low-pass filter consisting of C536, C544 and L512 passes only the 1.2 MHz difference frequency. The signal is then amplified by Q505 and Q506 to 30 dB above the level received at the Antenna or T/R Connector and coupled through C522 and J503 to the Analyzer Log Amp Module.

2-4-22 ANALYZER LOG AMPLIFIER MODULE (FM/AM-1200S ONLY)

The logarithmic amplifier (log amp) converts the non-linear amplitude of the swept IF signal into a linear output for the analyzer vertical drive. In addition to containing the log amplifier, this module also contains the 30 kHz bandpass filter due to space limitations in the Analyzer IF Module.

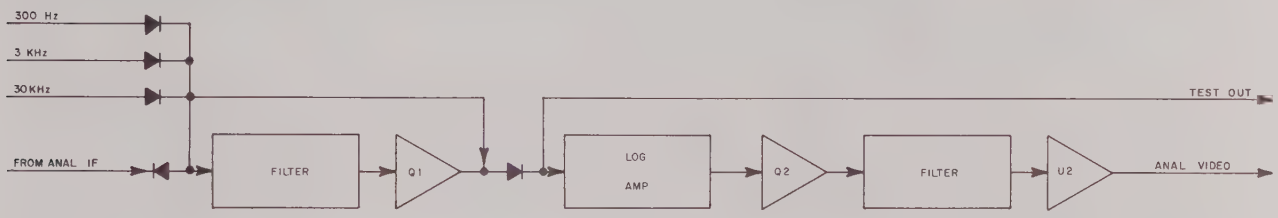


Figure 2-27 Analyzer Log Amp Block Diagram

A. 30 kHz Bandpass Filter Circuit

When any analyzer dispersion range is selected on the HORIZONTAL Sweep Control, +12V forward biases CR804 and CR807 and reverse biases CR805 and CR806. This directs the 1.2 MHz IF through a 6-pole, 30 kHz bandpass filter, consisting of FL801 through FL806, and an amplifier to restore filter loss. Trimpot R809 calibrates the gain produced by Q801. J803 is a test port for the IF signal, which should be 10 dB above the received signal level.

B. Log Amp Circuit

The log amp circuit contains log amp IC U801, transformer T801 and two tuned amplifier stages. The 1.2 MHz IF is applied directly to U801, through trimpot R812, to the base of Q804 in the first amplifier stage. Trimpot R818 sets the gain of Q804 which, in turn, drives Q803. Q803 is tuned to 1.2 MHz by L810 and C834, with its output level limited by CR809 and CR810 to one diode gap above and below ground. This level is applied to U801 and to the base of Q805 in the second amplifier stage. The second stage, consisting of Q805, Q806 and associated components, is identical to the first stage, and is applied only to U801. All three trimpots in this circuit interact with the trimpots in the analyzer vertical drive circuit.

The output of U801 consists of two summations, linearly representing the logarithmic inputs. Each summation contains two outputs, Y, $\overline{Y}$ and Z, $\overline{Z}$ which are equal in amplitude but opposite in polarity. The Y and Z outputs are applied to one terminal of the primary of T801 and the $\overline{Y}$ and $\overline{Z}$ outputs are applied to the other terminal. T801 blocks the DC potential, couples the linearized output to the analyzer vertical drive circuit, and isolates the drive circuit from the log amp circuit.

C. Analyzer Vertical Drive Circuit

Emitter-follower Q802 is biased by +5.1V, which passes through the secondary winding of T801. This allows the output from the log amp, U801, to be coupled with the bias for Q802. The gain of Q802 is set by R821 and thermistor TR801. L808 and C824 tune the amplifier to 1.2 MHz. DC blocking capacitor C825 couples the RF signal to a rectifier/detector circuit.

+5.1 VDC is applied to the rectifier/detector circuit through a voltage divider consisting of R828, CR815 and trimpot R832 to adjust the base line level. The positive component of the signal pulse passes through AM detector CR814 to charge C828, which is discharged through R833 and trimpots R830 and R832. The circuit is tuned with L809, C826 and C827.

The reference level for op amp U802B is calibrated with R829 and trimpot R831. The output level from the rectifier/detector circuit, which is calibrated by R830, is applied to U802B for amplification. From U802B, the signal is routed through J801, pin 1 to the Scope Control Module.

All trimpots in the analyzer vertical drive and log amp circuits are interactive.

2-4-23 SCOPE POWER AND CONTROL ASSEMBLY

2-4-23-1 SCOPE CONTROL PC BOARD (FM/AM-1200S ONLY)

The Oscilloscope Control Board controls the sweep rate and the horizontal and vertical deflection for the Oscilloscope and Spectrum Analyzer functions. For the Oscilloscope function, it contains the sweep trigger and the vertical drive circuits. The analyzer sweep circuit also provides calibration adjustments for centering and dispersion. All mode and range selections are achieved by two ganged, rotary switches mounted on the Oscilloscope Control Board and extending through the Front Panel.

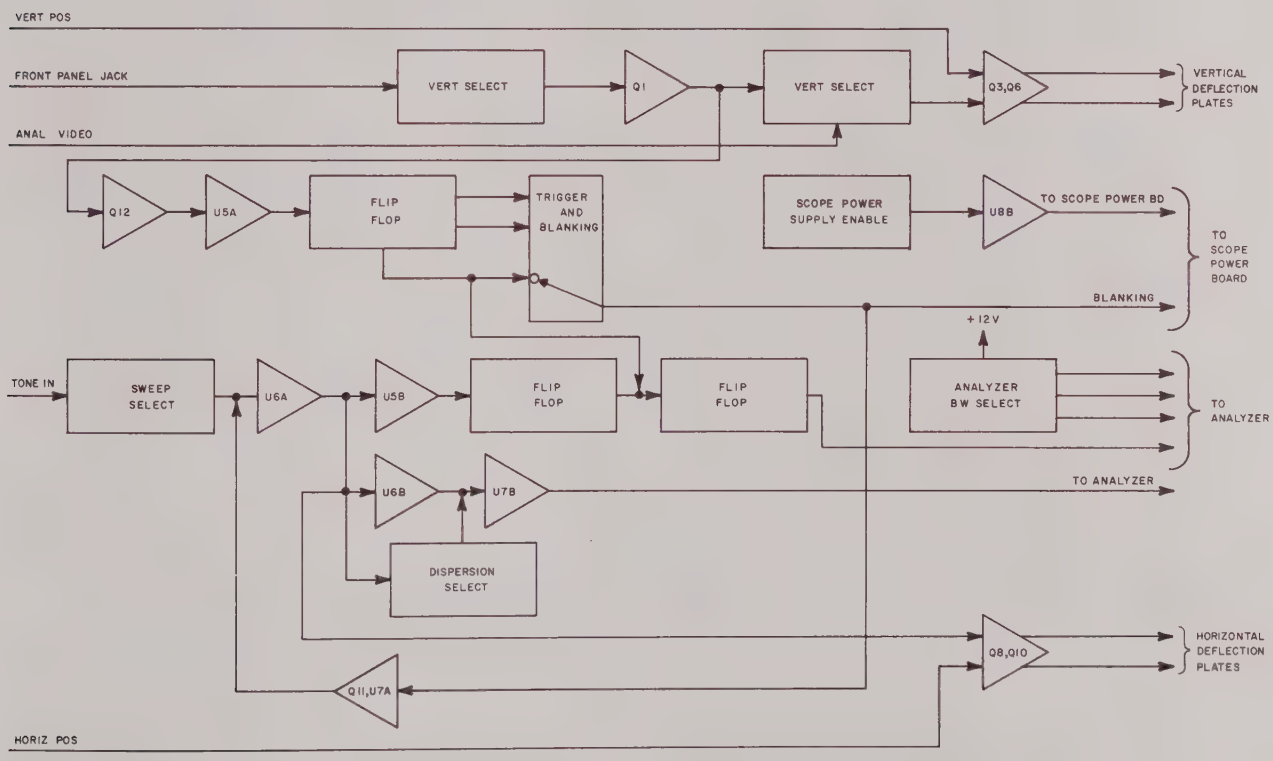


Figure 2-28a Scope Control PC Board Block Diagram (FM/AM-1200S Only)

A. Scope Enable Circuit

Op amp U208B functions as a comparator to provide a high output to the Oscilloscope Power Supply Board when S201 (VERTICAL Attenuator Selector) is in the "OFF" position. In any other position, S201 allows +12V to be applied to pin 6 of U208B, exceeding the reference voltage of +7V at pin 5, which allows the Oscilloscope Power Supply to operate. In the "OFF" position, S201 grounds the +12V control.

B. Horizontal Drive Circuit

The sweep rate is set by a switch, consisting of Q211 and op amp U207A, a ramp generator using a constant current source, Q202 and associated components, and one capacitor, either C218, C219, C220, C221 or C228 as selected by S202. When Q211 is turned on, op amp U207A pulls the ramp voltage to -0.5V; when it is turned off, the ramp voltage increases at the rate determined by the selected capacitor and the constant current drawn through Q208. Buffer U206A applies this ramp signal to the horizontal deflection circuit, the analyzer sweep divider circuit, and op amp U205B. U205B is configured as a comparator, which is calibrated by R244, R245 and R293 to trigger when the output of U206A reaches +0.5V. When U205B sets flip-flop U203B, the high Q output performs four functions. First, it supplies the reset trigger for U209A to reset the trigger function. Second, it charges C217 in the free-run timer until the timer resets U203B, pulling Q low. Third, it supplies a high through multiplexer U204 to blank the Oscilloscope and, simultaneously, turns on Q211, terminating the sweep. When the free-run timer resets U203B, blanking signal ends and Q211 turns off, allowing the next sweep to commence. Fourth, it clocks flip-flop U203A to blank the Spectrum Analyzer until its blanking timer, consisting of R297 and C233, resets U203A. As R248 (Sweep Vernier Control) is rotated ccw the base voltage of Q202 increases. This increase in base voltage decreases the current flow through Q202, slowing the sweep rate. R248 is bypassed by U202B when in analyzer operation.

When S202 (Horizontal Sweep Selector) is in the "TONE" position, Q202 is coupled to R250 to provide a constant current. Any tone applied to the modulator circuit of the Generate Audio Module is then applied to the sweep generator circuit and its amplitude generates the horizontal component of the trace. S202 also switches U204 to the Tone mode, which applies -7V to the oscilloscope blanking circuit in the Oscilloscope Power Supply to prevent blanking, and to the base of Q211, keeping it turned off.

C. Horizontal Deflection Circuit

The horizontal deflection circuit consists of a buffer amplifier and a differential amplifier. The sweep signal from buffer U206A is applied to buffer U208A. R271 allows calibrating the gain of U208A so the trace sweeps exactly the width of the screen. The output of U208A biases Q209 in the differential amplifier. The horizontal position reference signal, as established with the front panel HORIZ POS Control, is applied to the base of Q208. Q210 and associated components form a constant current source drawing equally on Q208 and Q209. As the bias voltages differ between Q208 and Q209, the current flow through them varies inversely, causing the horizontal deflection plate voltages to vary proportionately to the difference in the bias voltages.

When S202 is not in one of the ms/DIV positions (Oscilloscope operation), U202C routes the horizontal position control signal through a voltage divider to attenuate the effect of the control.

D. Input Attenuation Circuit

An external signal applied through the SCOPE Connector, routed through the AC-DC Switch, is applied to pin C of S201. Demodulated audio signals from the Receive Audio Module are applied through R201 to pin B and to a voltage divider consisting of R202 and R203. The signal level is divided by four through the voltage divider and applied to pin A of S201. Depending upon the Front Panel selection of S201, the signal applied at pin A, B or C is coupled to the appropriate input attenuator at pin D, E or F.

The ÷1 circuit connects pins C and D of S201, providing no attenuation. C202 and R281 provide input impedance for the Oscilloscope. The X10 circuit consists of C203, C204, R205 and R206, and connects pins C and E of S201. The X100 and X1000 is a ladder circuit consisting of C201, C205, C206, R207, R208 and R209. The circuit links pin K to pin M to select the divide-by-100 circuit, and pin L to pin M to select the divide-by-1000 circuit. All attenuators provide approximately 17 pF capacitance and 1 MΩ resistance for Oscilloscope input impedance.

The distortion residual from the Receive Audio Module is applied through a 10:1 voltage divider consisting of R210 and R211 to pin N of S201.

E. Oscilloscope Vertical Drive Circuit

From S201 pin M, the selected signal is passed across a limiter consisting of CR201 and CR202 before it is applied to the gate of FET Q201A. Q201 is a dual FET manufactured on the same substrate. Q201A is a current follower while Q201B is a constant current source calibrated by R215. As the input signal amplitude varies, changing the current flow through Q201A accordingly, the current flow through R216 and R217 varies as to maintain a constant current through Q201B. The signal which is received from the attenuators in the form of voltage is converted to current through R216 and R217 by Q201A, Q201B and related components. The signal is attenuated approximately 4 dB, and applied to the vertical deflection preamp, U201A. The gain of U201A calibrated by R221, is approximately +24 dB, making the net gain of the circuit approximately +20 dB.

F. Vertical Deflection Circuit

Vertical deflection is accomplished with a differential amplifier consisting of discrete transistors Q203 through Q207, and related components. A vertical position reference signal, between -12 VDC and +12 VDC as established with the Front Panel VERT POS Control, is applied to the base of Q206. S202 (HORIZONTAL Sweep Selector) applies a signal from the vertical drive circuit of either the Oscilloscope or Spectrum Analyzer to the base of Q205. Q207 and associated components form a constant current source drawing current through the two amplifiers Q203/Q205 and Q204/Q206. As the bias voltages differ between Q205 and Q206, the current flow through them varies inversely, causing the vertical deflection plate voltages to vary proportionately to the difference in the bias voltages.

When S202 is not in one of the ms/DIV positions, switch U202A routes the vertical position control signal through a voltage divider to attenuate the effect of the control.

G. Scope Trigger Circuit

The signal from the oscilloscope drive circuit is buffered by Q212, with C231 and C232 removing any DC component, leaving only the AC components referenced to ground potential. This signal is applied to pin 3 of op amp U205A. U205A functions as a Schmitt trigger and provides a high output for the positive portions of the signal. U205A clocks D-type flip-flop U209A with the leading edge of the pulse, providing a positive only, non-selectable trigger. The high $\overline{Q}$ output from U209A charges C216 and switches multiplexer U204 to couple the $\overline{Q}$ output to its output at pin 3. This turns off Q211 and allows the sweep to commence. When the sweep is finished and U205B sets U203B, the high Q from U203B resets U209B. The next trigger pulse from U205A again sets U409A, and the cycle repeats. C216 holds U204 in the trigger mode for at least one-half second to provide the ability to trigger on low frequencies or partial waveforms. If no trigger is received during this period, U204 will revert to the free-run mode.

H. Analyzer Sweep Circuit

The output from U206A to the analyzer sweep circuit is amplified by op amp U206B and U207B to an output from -7V to +7 VDC with S202 in the 1 MHz/DIV position. R260 allows calibration of this output. For other dispersion positions, S202 provides a ground path through one of three voltage dividers for U206B, and through one of two voltage dividers for U207B. R298 provides a DC offset voltage to be summed with the sweep signal before routing it to the Analyzer RF Module.

2-4-23-2 SCOPE CONTROL PC BOARD (FM/AM-1200A ONLY)

The Oscilloscope Control Board controls the sweep rate and the horizontal and vertical deflection for the oscilloscope functions. All mode and range selections are achieved by two ganged, rotary switches mounted on the Oscilloscope Control Board and extending through the Front Panel.

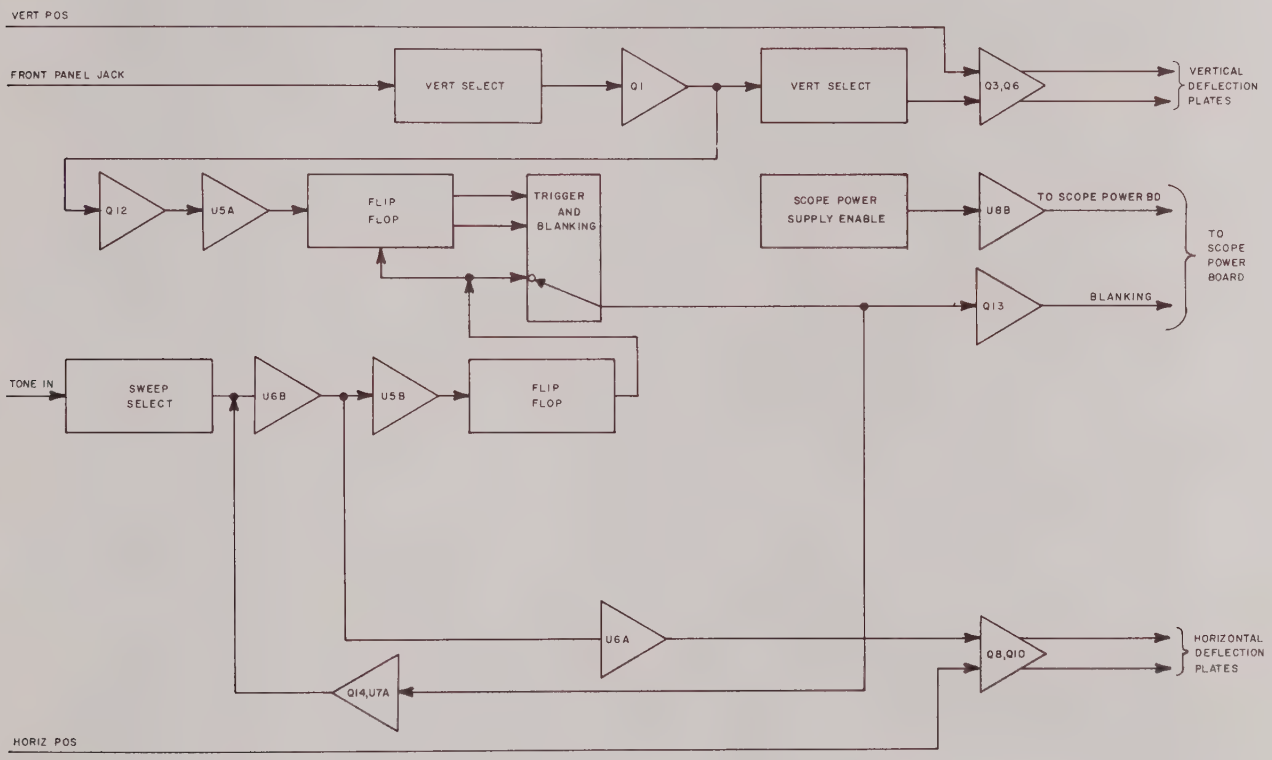


Figure 2-28b Scope Control PC Board Block Diagram (FM/AM-1200A Only)

A. Scope Enable Circuit

Op amp U208B functions as a comparator to provide a high output to the Oscilloscope Power Supply Board when S201 (VERTICAL Attenuator Selector) is in the "OFF" position. In any other position, S201 allows +12V to be applied to pin 2 of U208A, exceeding the reference voltage of +7V at pin 3, which allows the Oscilloscope Power Supply to operate. In the "OFF" position, S201 grounds the +12V control.

B. Horizontal Drive Circuit

The sweep rate is set by a switch, consisting of Q214 and op amp U207A, a ramp generator using a constant current source, Q202 and associated components, and one capacitor, either C218, C219, C220, C221 or C222 as selected by S202. When Q214 is turned on, op amp U207A pulls the ramp voltage to -0.5V; when it is turned off, the ramp voltage increases at the rate determined by the selected capacitor and the constant current drawn through Q202. Buffer U206B applies this ramp signal to the horizontal deflection circuit and op amp U205B. U205B is configured as a comparator, which is calibrated by R244, R245 and R293 to trigger when the output of U206A reaches +0.5V. When 205B sets flip-flop U203B, the high Q output performs three functions. First, it supplies the reset trigger for U203A to reset the trigger function. Second, it charges C217 in the free-run timer until the timer resets U203B, pulling Q low. Third, it supplies a high through multiplexer U204 through FET Q2013 to terminate the sweep. When the free-run timer resets U203B, the blanking signal ends and Q214 turns off, allowing the next sweep to commence. As R248 (Sweep Vernier Control) is rotated ccw, the base voltage of Q202 increases. This increase in base voltage decreases the current flow through Q202, slowing the sweep rate.

When S202 (Horizontal Sweep Selector) is in the "TONE" position, Q202 is coupled to R250 to provide a constant current. Any tone applied to the modulator circuit of the Generate Audio Module is then applied to the sweep generator circuit and its amplitude generates the horizontal component of the trace. S202 also switches U204 to the Tone mode, which applies -7V to the oscilloscope blanking circuit in the Oscilloscope Power Supply to prevent blanking, and to the base of Q214, keeping it turned off.

C. Horizontal Deflection Circuit

The horizontal deflection circuit consists of a buffer amplifier and a differential amplifier. The sweep signal from buffer U206B is applied to buffer U206A. R271 allows calibrating the gain of U206A so the trace will sweep exactly the width of the screen. The output of U206A biases Q209 in the differential amplifier. The horizontal position reference signal, as established with the front panel HORIZ POS Control, is applied to the base of Q208.Q210 and associated components form a constant current source drawing equally on Q208 and Q209. As the bias voltages differ between Q208 and Q209, the current flow through them varies inversely, causing the horizontal deflection plate voltages to vary proportionally to the difference in the bias voltages.

D. Input Attenuation Circuit

An external signal applied through the SCOPE/DVM Connector, routed through the AC-DC Switch, is applied to pin C of S201. Demodulated audio signals from the Receive Audio Module are applied through R201 to pin B and to a voltage divider consisting of R202 and R203. The signal level is divided by four through the voltage divider and applied to pin A of S201. Depending upon the Front Panel selection of S201, the signal applied to pin A, B or C is coupled to the appropriate input attenuator at pin D, E or F.

The ÷1 circuit connects pins C and D of S201, providing no attenuation. C202 and R281 provide input impedance for the Oscilloscope. The X10 circuit consists of C203, C204, R205 and R206, and connects pins C and E of S201. The X100 and X1000 is a ladder circuit consisting of C201, C205, C206, R207, R208 and R209. The circuit links pin K to pin M to select the divide-by-100 circuit and pin L to pin M to select the divide-by-1000 circuit. All attenuators provide approximately 17 pF capacitance and 1 MΩ resistance for Oscilloscope input impendance.

The residual distortion from the Receive Audio Module is applied through a 10:1 voltage divider consisting of R210 and R211 to pin N of S201.

E. Oscilloscope Vertical Drive Circuit

From S201 pin M, the selected signal is passed across a limiter consisting of CR201 and CR202, then applied to the gate of FET Q201A. Q201 is a dual FET manufactured on the same substrate. Q201A is a current follower while Q201B is a constant current source calibrated by R215. As the input signal amplitude varies, changing the current flow through Q201A accordingly, the current flow through R216 and R217 varies to maintain a constant current through Q201B. The signal which is received from the attenuators in the form of voltage is converted to current through R216 and R217 by Q201A, Q201B and related components. The signal is attenuated approximately 4 dB, and applied to the vertical deflection preamp, U201A. The gain of U201A, calibrated by R221, is approximately +24 dB, making the net gain of the circuit approximately +20 dB.

F. Vertical Deflection Circuit

Vertical deflection is accomplished with a differential amplifier consisting of discrete transistors Q203 through Q207, and related components. A vertical position reference signal, between -12 VDC and +12 VDC as established with the Front Panel VERT POS Control, is applied to the base of Q206. S202 (HORIZONTAL Sweep Selector) applies a signal from the vertical drive circuit of the Oscilloscope to the base of Q205. Q207 and associated components form a constant current source drawing current through the two amplifiers Q203/Q205 and Q204/Q206. As the bias voltages differ between Q205 and Q206, the current flow through them varies inversely, causing the vertical deflection plate voltages to vary proportionally to the difference in the bias voltages.

G. Scope Trigger Circuit

The signal from the oscilloscope drive circuit is buffered by Q212, with C231 and C232 removing any DC component, leaving only the AC components referenced to ground potential. This signal is applied to pin 3 of op amp U205A. U205A functions as a Schmitt trigger and provides a high ouput for the positive portions of the signal. U205A clocks D-type flip-flop U203A with the leading edge of the pulse, providing a positive only, non-selectable trigger. The high Q output from U203A charges C216 and switches multiplexer U204 to couple the Q-not-A output to its output at pin 3. This turns off Q214 and U205B to set U203B. The high Q from U203B then resets U203A. The next trigger pulse from U205A again sets U203A, and the cycle repeats. C216 holds U204 in the trigger mode for at least one-half second to provide the ability to trigger on low frequencies or partial waveforms. If no trigger is received during this period, U204 will revert to the free-run mode.

2-4-23-3 SCOPE POWER SUPPLY PC BOARD

The only power required by the CRT Power PC Board is +12 VDC, supplied through the Oscilloscope Control Board. An oscillator, controlled by a scope enable command, produces timing square waves to power the transformer circuit. The transformer supplies all voltages required by the CRT.

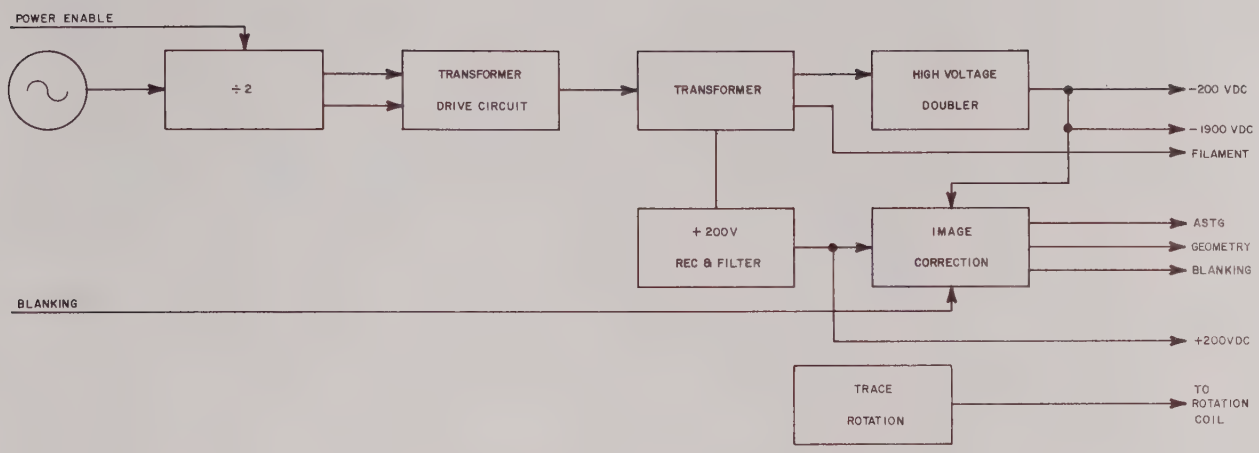


Figure 2-29 Scope Power Supply PC Board Block Diagram

A. Oscillator Output Circuit

A 90 kHz oscillator is formed by NOR gates U301A and U301B, which clock J-K flip-flops U302A and U302B simultaneously. With +12 VDC applied to the J and K inputs of U302A, the Q and $\overline{Q}$ outputs alternate between high and low. Q of U302A provides the J and K inputs to U302B. Since U302B changes state only when J and K are high (U302A Q is high), its frequency is half that of U302A. Only with U302A Q and U302B $\overline{Q}$ both low, NOR gate U301D provides a high to the transformer circuit. Likewise, when U302A $\overline{Q}$ and U302B Q are both low, U301C provides a high to the transformer circuit.

When the VERTICAL Attenuator Selector on the Front Panel is in the "OFF" position, the Oscilloscope Control Board supplies a high command to the reset terminal, pin 4, of U302A to inhibit the oscillator circuit output to the Transformer circuit.

B. Transformer Circuit

Power is supplied through a filter consisting of C304, C305 and toroid L301 to the center tap of the primary winding of transformer T301. R325 normally grounds the gate of FET Q305. When U301D output goes high, Q301 applies power to the gate of Q305. Q305 grounds one end of the primary winding. Similarly, U301C controls Q303, which supplies the gate voltage to FET Q306. When Q303 is off, R324 grounds the gate of Q306. Q306 grounds the opposite end of the primary winding. The effective power applied to the primary winding of T301 is then 24 VAC.

The high voltage secondary winding produces 1000 VAC. This is rectified and doubled by CR301 and CR302, C306 and C307. The resulting -2000 VDC is then applied to the CRT grid and to a voltage divider consisting of fixed resistors R307, R311, R313, R314 and R315 and potentiometers, R308 and R312. R308 provides -1900 VDC for the cathode (intensity) and R312 provides -1500 VDC for the focus of the beam. The secondary winding provides 6.3 VAC for the CRT filament. This 6.3 VAC is riding a -1900 VDC offset.

The middle voltage secondary winding output is rectified by CR303 through CR306, and filtered by R310 and C309 through C312 to supply +200 VDC to the image correction circuit, and to the Oscilloscope Control Board for horizontal and vertical deflection.

C. Image Correction Circuit

The +200 VDC from the transformer circuit is reduced to approximately +100 VDC, set by trimpot R316 for calibration of CRT astigmatism (vertical component of the beam). Q308 is an emitter-follower which furnishes approximately +100 VDC for the CRT geometry (horizontal component of the beam). R317 calibrates the base voltage of Q308.

D. Display Blanking Circuit

While the display trace is displayed on the CRT screen, Q309 applies the display blanking to the geometry supply from Q308. When the trace is not displayed (i.e., during retrace), the beam is shifted off the screen without suppressing its intensity. During the blanking command from the Oscillsocope Control Board, Q307 conducts, pulling down on the emitter of Q309 and simultaneously applying voltage to its base. This turns off Q309, allowing the voltage on the display blanking and the base of Q309 to drop to approximately +10.8 VDC. When the blanking command is removed, Q307 turns off, allowing the display blanking line to float. Q307 simultaneously removes the base voltage to Q309, allowing it to conduct. This snaps the display blanking line back to its original level and returns the beam to the CRT screen.

E. Rotation Circuit

R322 applies a 0-12 VDC level to the rotation coil of the CRT to align the trace with the horizontal axis of the screen graticule. If the range of R322 is insufficient to fully align the trace, rotation of connector P/J301 by 180° reverses the polarity of the coil. The trace can then be aligned using R322.

2-4-24 KEYBOARD

The keyboard is a 4 X 6 Matrix PC Board with 24 independent momentary pushbutton switches. Two buses (4-bit and 6-bit) connect the CPU to the keyboard. The CPU forces all 4 lines of the 4-bit bus low simultaneously. When a key is pressed, an interrupt is generated which causes the CPU to strobe the 4-bit bus lines. This low will be detected by one of the lines on the 6-bit bus, to determine which key is depressed.

2-4-25 DISPLAY PC BOARD

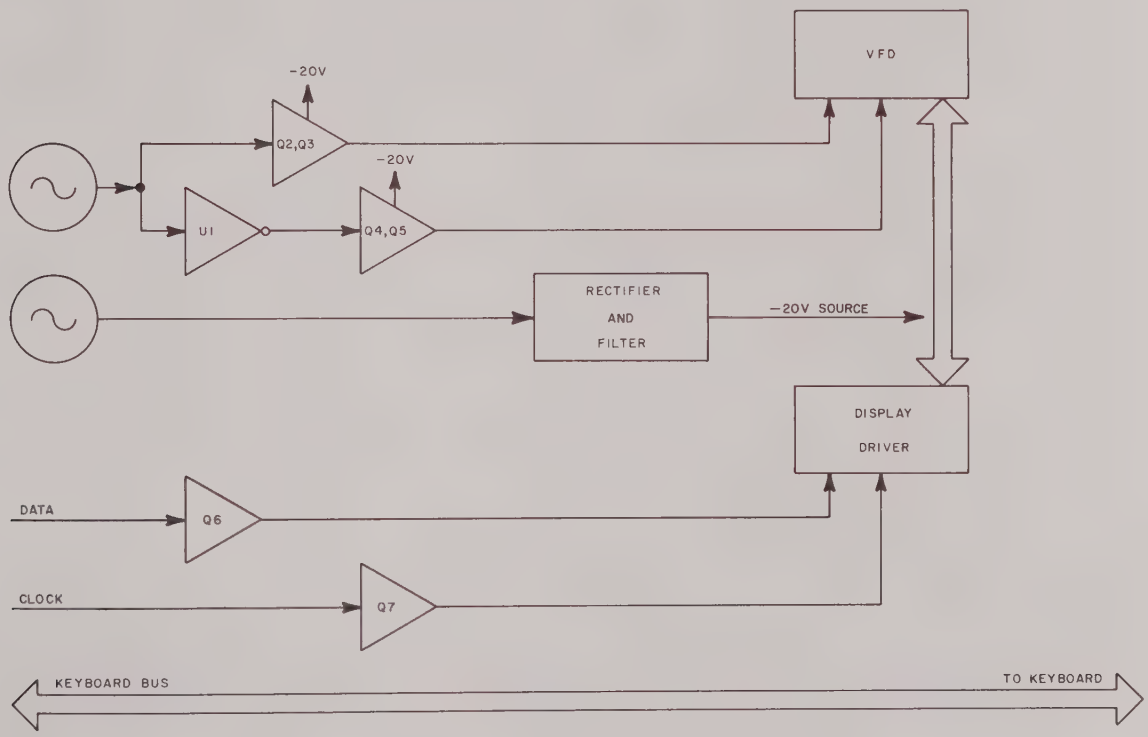


Figure 2-30 Display PC Board Block Diagram

A 16-character Vacuum Fluorescent Display (VFD), DS1401, and its driver, U1403, are installed on the Display Board and mounted on the Front Panel. The Keyboard is also assembled with the Display Board.

Power to operate the VFD and the driver chip is furnished by an onboard power supply which converts -12 VDC to -3 VDC and -20 VDC. An oscillator switches these two voltages across the two power pins of DS1401 to produce approximately 30 VAC. Timer U1402 is connected between -12 VDC and ground. R1411, R1412 and C1409 establish the R-C time constant for a stable operation, producing -12V pulses. C1410 couples the pulses to -12 VDC supplied through CR1401, to produce -12V pulses riding on

-12 VDC. C1411 filters this supply to approximately -20 VDC. R1404, R1405, C1405 and inverters U1401E and U1401F form an oscillator which drives switching transistors Q1402 and Q1403 through inverter U1401A and transistors Q1404 and Q1405 through U1401C and U1401D. Q1401 regulates the -20 VDC to -3 VDC, which is applied to the collectors of Q1402 and Q1404, with -20 VDC being applied to the collectors of Q1403 and Q1405. As the inverter switches the transistors on and off, -3 VDC and -20 VDC (minus losses) are alternately switched between pins 1 and 37 of DS1401. This produces the effect of -15 VAC to DS1401.

A clock signal from the CPU is supplied to U1403 through level converting transistor Q1407. Data is furnished through level converting transistor Q1406. When U1403 is clocked, it shifts existing data one place to the left and presents the new data in the just vacated right-hand position.

2-4-26 FUNCTION SWITCH PC BOARD

The Function Switch PC Board contains the front panel meters, squelch and volume controls, tone select and level controls, and four rotary switches for selecting meter function, mode, frequency error range, and modulation. All switching lines are routed through the motherboard and all can be processor controlled. This board also contains the LOCK Lamp and the SIG Indicator Lamp, which indicate respectively that the RF system is locked on frequency and that the input signal is greater than the squelch level.

2-4-27 RS-232C TO GPIB INTERFACE

PC Board RS-232c Serial Data (-10V to +10V) is converted to serial data (0V to +5V) in U65001 and enters U65004 where the serial data is converted to parallel GPIB data format. U65004 accesses address decoder (U65006) for it to select combinations of U65008, U65009 and U65010. U65009 sends instructions to both U65004 and U65010. U65008 is a scratch pad RAM used for storing results of intermediate calculations. U65010 is a GPIB interface control used to gather and send GPIB information out onto the main data bus via U65011 through U65014.

2-4-28 CELLULAR OPTION PC BOARD (FM/AM-1200S ONLY)

The Supervisory Audio Tone (SAT), Signaling Tone (ST) and Manchester data from the Unit Under Test (UUT) pass through a voltage follower (U96001A) and are attenuated by programmable attenuators U96002 and U96008. Supervisory Audio Tone is the only signal that passes through the programmable filter (U96010). This tone is approximately 6 kHz, which is rectified by U96011A and DC converted by R96025 and C96016. This DC signal is compared to circuitry between pins 3 and 6 of U96012. If the level is above approximately 0.5V, then pin 6 of U96012 goes low

and the SAT DETECT line goes low. If no SAT is present, pin 6 of U96012 is +12 VDC and CMOS inverter presents +5 VDC on SAT detect line.

Signaling Tone and Manchester data are passed through programmable filter U96002 and the 10 kHz tone is rectified by U96004A, CR96005, CR96012 and R96007. The tone is converted to DC by C96006 and R96011. The tone is then compared to circuitry between pins 3 and 6 of U96005. If the level is above approximately 0.5V, pin 6 and the ST detect line go low. Signaling Tone and Manchester data are never present simultaneously. If Manchester data is present, the Manchester Clock is decoded by R96018, C96012, and U96014A. Manchester clock is presented to pin 67 of U96022 (XILINK Chip). U96022 converts Manchester serial data to parallel data and receives sync code data from U96021 to generate an INTB (Interrupt B) signal on pin 23. U96021 programs U96022. U96016 receives Manchester information and commands from Z280 on the encode/decode PC Board (option 11) to generate Manchester data for transmission. The generated Manchester data is encoded with a Manchester clock by U96017A and U96017B before it is sent to the programmable attenuator (U96020). The generated Manchester data is sent from pin 30 of J96001 (Tone Out) to the Generate Audio PC Board.

2-4-29 CELLULAR ENCODE/DECODE PC BOARD (FM/AM-1200S ONLY)

The Cellular Encode/Decode PC Board is used for cellular operation and for European encoding and decoding. The Z280 microprocessor (U59014) takes over and performs some handshaking with CPU through U59011 when using cellular operation and European encoding and decoding. U59004, U59005 and U59006 form a frequency counter for the demod Audio Module. U59007 is a ROM used to provide instructions for U59014. Signaling Tone and other tones for European encoding are generated by a tone generator consisting of U59002, U59003A, U59003B, U59003C, U59003D and U59016. MAX691 (U59018) ensures the FM/AM-1200S resets properly upon power up. It also is a "watchdog" which looks for any writing to RAM (U59008). If RAM was not written to in 1.6 seconds, the Supervisory Chip (U59018) issues a reset command.

SECTION 3 - PERFORMANCE EVALUATION

3-1 GENERAL

This section contains step-by-step test procedures for assessing the performance of the FM/AM-1200S/A. These procedures should be relied upon as the first step in the troubleshooting/maintenance process, when the operating condition of the set is in question. All procedures contained in this section are performed using the FM/AM-1200S/A front and rear panel controls, indicators and connectors and do not require the removal of the exterior case.

The test procedures contain several common headings which are defined below:

3-2-1	TEST PROCEDURE TITLE
PREREQUISITE:	Names of test procedures to be performed prior to performing current procedure.
SPECIAL ACCESSORY EQUIPMENT REQ'D:	List of any special accessory test equipment required to complete the test procedure.
INITIAL CONTROL SETTINGS:	Initial FM/AM-1200S/A front and rear panel control settings required to begin the test procedure. (Refer to Figure 1-2 on foldout page in Section 1 for front and rear panel control identification.)

3-1-1 PRE-OPERATIONAL CONSIDERATIONS

For maximum benefit of all operating procedures herein, it is strongly recommended that personnel:

A. Thoroughly read and understand all steps of procedure to be performed, prior to its completion.

B. Be familiar with the circuit or unit under test so some idea is perceived as to the power, frequency and waveform to be expected at each test point. This knowledge will aid the technician in performing the test procedure in a logical and efficient manner.

3-1-2 TEST EQUIPMENT REQUIREMENTS

Appendix B contains a comprehensive list of test equipment suitable for performing any of the procedures in this manual. Any other equipment meeting the specifications listed in the appendix, may be substituted in place of the recommended models.

NOTE: For certain procedures, the equipment listed in Appendix B may exceed the minimum required specifications.

3-1-3 CORRECTIVE MAINTENANCE PROCEDURES

The performance checks in this section will aid the operator/ technician in determining whether the FM/AM-1200S/A is functioning properly or if a failure condition exists. A failure condition will normally be reflected as either a calibration error or a malfunction. A calibration error is defined as a measurement or reading (relating to the unit being tested) that is not within prescribed tolerance (see Appendix A for unit specifications). In this condition, the set may outwardly appear to be functioning properly, despite the presence of a calibration error. A malfunction denotes a defective condition where a signal may be totally absent, grossly out of tolerance or where the unit itself (or any part thereof) is obviously not working properly.

In event a failure condition or calibration error is confirmed, the technician should take appropriate corrective action to return the set to its normal operating condition.

3-2 PERFORMANCE EVALUATION

3-2-1 RECEIVE MODE PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 RF Signal Generator
1 3 Foot Coax with BNC-to-BNC Connectors

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector Control	"REC"
41	SQUELCH Control	Fully ccw
3	MODULATION Select Control	"FM NAR"
4	MODULATION Meter Control	"6 kHz/%X10"
26	HORIZONTAL Sweep Selector Control	"1 MHz/Div" (1200S Only)
35	FREQ ERROR Meter Range Selector Control	"RF 10K"

STEP PROCEDURE

1. Adjust RF Signal Generator to 25.50 MHz, modulated with a 1 kHz tone with 5 kHz deviation at -40 dBm output.

2. Connect RF Signal Generator to ANTENNA Connector (34).

3. Using Keyboard (18), select "RF 025.5000" MHz and "2nd Function Meter".

4. Verify zero reading (±3% of full scale tolerance + Master Oscillator offset) on the FREQ ERROR Meter (36) and VFD (37).

5. Verify modulation readings on the MODULATION METER (1) and VFD (37) per Table 3-1:

CONTROL SETTING			FM/AM-1200S/A DISPLAY	
SIGNAL GENERATOR MODULATION	MODULATION SELECTOR (3)	METER RANGE SELECTOR (4)	MODULATION METER (1)*	VFD (37)*
5K FM	FM NAR	6	5	MD 5.XXX
5K FM	FM MID	6	5	MD 5.XXX
5K FM	FM WIDE	6		N/A
30% AM	AM NAR	6	5	MD 3.XXX
30% AM	AM NORM	6	5	MD 3.XXX
* Tolerance is 3% of full scale + Master Oscillator offset.				

Table 3-1 Control Settings with Modulation Meter and VFD Readings

6. Disconnect RF Signal Generator.

7. Set MODULATION Select Control (3) to "FM NAR" and adjust SQUELCH Control (41) to just squelch Receiver.

8. Adjust RF Signal Generator for no modulation and connect it to the Antenna Connector (34).

9. Select the following frequencies on the FM/AM-1200S/A and on the RF Signal Generator to verify receiver sensitivity of at least -101 dBm:

   255.5000 MHz
   455.5000 MHz
   855.5000 MHz

10. Set the frequency on the FM/AM-1200S/A and on the RF Signal Genera- tor to 999.9999 MHz to verify receiver sensitivity of at least -96 dBm.

11. Disconnect the RF Signal Generator.

12. Select RF of 151.0000 MHz on Keyboard (18) and set METER Range Selector Control (4) to "WATTS - PK 15".

13. Rotate SQUELCH Control (41) cw just enough to squelch the receiver.

14. Adjust RF Signal Generator for a signal of 151.0000 MHz at -90 dBm. Connect RF Signal Generator to ANTENNA Connector (34) of FM/AM-1200S/A to verify signal breaks squelch.

15. Decrease the RF Signal Generator output sufficiently to squelch the receiver.

16. Increase the signal level until it just breaks squelch. Record this level.

_____ dBm

NOTE: This level should be less than -101 dBm.

17. Verify adjacent channel rejection (ACR) by reducing the signal level to squelch the receiver and increasing the level until it just breaks squelch at each of the frequencies set to the bandwidths shown in Table 3-2. The ACR levels shown are relative to the level recorded in Step 16.

SIGNAL GENERATOR FREQUENCY (MHz)	FM/AM-1200S/A FREQUENCY (MHz)	MODULATION SELECTOR	ACR
151.0270	151.0000	FM NAR	+40 dB
151.3000	151.0000	FM MID	+40 dB

Table 3-2 Adjacent Channel Rejection Settings

18. Disconnect RF Signal Generator.

19. Set the following FM/AM-1200S/A controls:

	CONTROL	SETTING
3	MODULATION Select Control	"SSB"
18	Keyboard	"RF 000.0100 MHz"
40	VOLUME Control	cw as needed

20. Verify a stable tone of approximately 1 kHz from the Speaker.

21. Set the following FM/AM-1200S/A controls:

	CONTROL	SETTING
3	MODULATION Select Control	"FM NAR"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
8	1 kHz Tone Level Control	Fully ccw
18	Keyboard	"RF 10.0000 MHz"

22. Connect coax between ANTENNA Connector (34) and External Reference Connector (45).

23. Verify FREQ ERROR Meter (36) reading of zero.

24. Use Table 3-3 to verify Frequency Error Meter readings for the ranges indicated:

FREQ ERROR METER Range Selector Control (35)	FREQUENCY (MHz)	FREQ ERROR Meter (36)	TOLERANCE
RF 10K	010.0100 009.9900 009.9870	-1.00 +1.00 Pegged +	600 Hz 600 Hz
RF 1K	009.9970 009.99990	Pegged + +1.00	 60 Hz
RF 100	009.9999	+1.00	6 Hz
RF 3K	010.0030 009.9970	-3.0 +3.0	18 Hz 18 Hz
RF 300	009.9997	+3.0	1.8 Hz
RF 30	010.0000	0	18 Hz

Table 3-3 Frequency Error Verification Chart (RF)

25. Set FM/AM-1200S/A controls as follows:

CONTROL		SETTING
39	Mode Selector Control	"GEN"
4	MODULATION Meter Control	"6 kHz/%X10"
7	1 kHz Tone Selector Switch	"ON"
8	1 kHz Tone Level Control	"5 kHz Deviation"

26. Use the Keyboard (18) and the FREQ ERROR METER Range Selector Control (35) to verify the range and frequency combinations shown in Table 3-4 within the indicated tolerances.

FREQ ERROR METER Range Control (35)	FREQUENCY Selector (SINE)	FREQ ERROR Meter (36)*
AUDIO 300	TONE 01000.0 TONE 01300.0 TONE 00700.0	0 -3.0 +3.0
AUDIO 30	TONE 01030.0 TONE 00970.0	-3.0 +3.0
AUDIO 3	TONE 01003.0 TONE 00997.0	-3.0 +3.0
*Tolerance is 3% of Full Scale ± 1% of Tone.		

Table 3-4 Frequency Error Meter Verification (Audio)

27. Remove coax and disconnect test equipment.

3-2-2 GENERATE MODE PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Spectrum Analyzer
1 Function Generator
1 Microwattmeter
1 Modulation Meter
1 Frequency Counter

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTING
22	PWR/OFF/BATT Switch	"PWR"
32	GEN/LOCK Control	"LOCK"
39	MODE Selector Switch	"GEN"
3	MODULATION Select Control	"FM WIDE"
4	MODULATION Meter Control	"6 kHz/%X10"
5	VAR Tone Selector Switch	"OFF"
6	VAR Tone Level Control	Fully ccw
7	1 kHz Tone Selector Switch	"OFF"
8	1 kHz Tone Level Control	Fully ccw
9	RF level Attenuator Control	"-30 dBm"
10	RF Level Attenuator Vernier Control	Fully ccw

STEP PROCEDURE

1. Connect Frequency Counter to T/R Connector (11).

2. Use the Keyboard (18) to select the frequencies shown in Table 3-3 to verify frequency accuracy with the Frequency Counter.

FREQUENCY (MHz)	FREQUENCY TOLERANCE (Hz)*	
	OPTIONAL TCXO (.2 ppm)	OPTIONAL OVEN (.05 ppm)
000.5000	000.10	00.025
002.5000	000.50	00.125
012.5000	002.50	00.625
042.5000	008.50	02.125
142.5000	028.50	07.125
342.5000	068.50	17.125
642.5000	128.50	32.125
999.9999	200.00	50.000

* Tolerance measurable ± accuracy of Frequency counter.

Table 3-5 Generate Frequency Accuracy

3. Disconnect Frequency Counter.

4. Connect Spectrum Analyzer to T/R Connector (11).

5. Select each of the frequencies in Table 3-5 to verify tolerance within 2.5 dB at both -30 dBm and -110 dBm.

6. Select 500.0000 MHz RF on Keyboard (18).

7. Rotate the RF Level Attenuator Vernier Control (10) through its entire range to verify the output level shifts at least 11 dB.

8. Connect Spectrum Analyzer to DUPLEX Connector (14).

9. Select the following control settings on the FM/AM-1200S/A:

CONTROL	SETTING
39 MODE Selector	"DUP"
18 Keyboard	"RF 150.0000 MHz"

10. Use the Keyboard to select each of the offset frequencies in Table 3-6. Verify the correct output frequency and level.

OFFSET FREQUENCY (MHz)	DUPLEX FREQUENCY (MHz)	DUPLEX HIGH OUTPUT LEVEL (dBm)	DUPLEX LOW OUTPUT LEVEL (dB from Duplex High)
+ 1.0000	151.0000	-15 (±10 dB)	-20 TO -30 (±10 dB)
- 2.0000	148.0000	-15 (±10 dB)	-20 TO -30 (±10 dB)
+ 5.5000	155.5000	-15 (±10 dB)	-20 TO -30 (±10 dB)
-10.0000	140.0000	-15 (±10 dB)	-20 TO -30 (±10 dB)
+15.5500	165.5500	-15 (±10 dB)	-20 TO -30 (±10 dB)
-20.0000	130.0000	-15 (±10 dB)	-20 TO -30 (±10 dB)
+35.0000	185.0000	-15 (±10 dB)	-20 TO -30 (±10 dB)
-49.9900	100.0100	-15 (±10 dB)	-20 TO -30 (±10 dB)

Table 3-6 Duplex Offset Output Frequencies and Levels

11. Connect Spectrum Analyzer to T/R (11).

12. Verify output level of -85 dBm (±10 dB).

13. Disconnect all test equipment.

SECTION 4 - CALIBRATION

4-1 GENERAL

This section contains calibration procedures for the following FM/AM-1200S/A front panel indicators and internal modules:

CALIBRATION PROCEDURE	CALIBRATION PROCEDURE TITLE	PAGE NO
4-2-1	Mechanical Zero of Meters	4-5
4-2-2	Power Supply Calibration	4-7
4-2-3	Frequency Standard Calibration	4-9
4-2-4	Function Generator Calibration	4-11
4-2-5	High and Fast Low Loop Calibration	4-13
4-2-6	Digital Module Calibration	4-21
4-2-7	10.7 MHz Generator/Receiver Calibration	4-23
4-2-8	Modulation Meter Calibration	4-33
4-2-9	Generate Signal Calibration	4-39
4-2-10	Oscilloscope/Analyzer Calibration (FM/AM-1200S Only)	4-43
4-2-11	Oscilloscope Calibration (FM/AM-1200A Only)	4-49
4-2-12	DVM I/O Calibration	4-53

These procedures should be performed as a result of one or more of the following conditions:

A. If, during the course of normal operation, the FM/AM-1200S/A fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".

B. If a module is found to be defective and requires significant repair or replacement.

C. If the recommended annual calibration is due.

4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when troubleshooting "live" circuits. When performing the calibration procedures in this section, be sure to observe the following precautions:

WARNING: AS LONG AS THE BATTERY IS INSTALLED OR EXTERNAL AC OR DC POWER IS APPLIED, A 12 VDC POTENTIAL EXISTS AT VARIOUS POINTS ON THE REAR PANEL, REGARDLESS OF THE FRONT PANEL POWER SWITCH POSITION.

WARNING: TO AVOID SERIOUS SHOCK HAZARD WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN A POCKET OR BEHIND YOUR BACK. AS LONG AS THE BATTERY IS INSTALLED OR EXTERNAL AC OR DC POWER IS APPLIED, A 12 VDC POTENTIAL EXISTS AT VARIOUS POINTS ON THE REAR PANEL, REGARDLESS OF THE FRONT PANEL POWER SWITCH POSITION.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE TROUBLE- SHOOTING AND/OR REPAIRING LIVE CIRCUITS. FOR ADDED INSULATION, PLACE A RUBBER BENCH MAT UNDER ALL POWERED BENCH EQUIPMENT, AS WELL AS A RUBBER FLOOR MAT BENEATH THE TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

4-1-2 DISASSEMBLY REQUIREMENTS

To perform any of the calibration procedures in this section (with the exception of 4-2-1, Mechanical Zero of Meters), the exterior case must be removed from the FM/AM-1200S/A. Those modules which must be removed and disassembled for calibration are identified in the setup of the procedure.

4-1-3 TEST EQUIPMENT REQUIREMENTS

A list of test equipment required to perform each calibration procedure is provided with the procedure. The minimum equipment specifications to meet these requirements are listed in Appendix B.

4-1-4 CONTROLS AND CALIBRATION POINTS

The various front and rear panel controls, connectors and indicators specified in the calibration procedures are followed by an item number. Figure 1-2 shows the location of each of these items. Calibration points for the Spectrum Analyzer Module are shown on the individual PC Board drawings in Section 7. All other calibration points are identified in Figure 4-10.

4-1-5 UPON COMPLETION OF CALIBRATION PROCEDURES

The procedures contained in this section are complete for the system specifically addressed. Upon completion of a given procedure, the entire calibration procedure may be terminated. Control settings, operating commands, and test equipment connections do not carry over from one procedure to another, and are not assumed at the start of any procedure. Always disconnect all test equipment and reconnect any cables, harnesses, etc., which may have been disconnected or removed while conducting a procedure, upon its completion.

4-2 CALIBRATION PROCEDURES

Before making any calibration adjustments, always observe the signal measurement. If the measurement is within the tolerances given, do not proceed with that specific adjustment. (The only time an adjustment is required for a measurement within tolerance is when a subsequent interactive adjustment is insufficient and the procedure explicitly requires repeating previous steps.) Normally, when an adjustment is required, the technician should attempt to obtain a precise measurement, and should not be satisfied with an adjustment that is just within tolerance.

IF THIS MODULE IS REPAIRED OR REPLACED / THE FOLLOWING CALIBRATION PROCEDURES MUST BE PERFORMED	MECH ZERO OF METERS (4-2-1)	POWER SUPPLY (4-2-2-)	FREQUENCY STANDARD (4-2-3)	FUNCTION GENERATOR (4-2-4)	HIGH-LOOP LOW-LOOP (4-2-5)	DIGITAL MODULE (4-2-6)	10.7MHz GEN/REC (4-2-7)	MODULATION METER (4-2-8)	GENERATE SIGNAL (4-2-9)	O'SCOPE ANALYZER FM/AM-1200S ONLY (4-2-10)	O'SCOPE FM/AM-1200A ONLY (4-2-11)	DVM I/O (4-2-12)
POWER SUPPLY	1	●	1	1	1	1		1,4	1	1	1	1
FREQUENCY STANDARD PC BD			●		1	1		1,4		1	1	
OUTPUT AMPLIFIER MODULE								1,4	●			
IF MODULE								1,4	●	●	●	
DUAL VCO MODULE					●			4	●	1	1	
1120 MHz LOW PASS FILTER					●			1,4	1			
HIGH/LOW PASS FILTER					●			1,4	1			
HIGH LOOP MODULE					●			4	●	1	1	
LOW LOOP MODULE					●			1,4	●	1	1	
10.7 MHz GEN/REC MODULE							●	4	●			
RECEIVE AUDIO PC BD						1		4	●	2		●
GENERATE AUDIO PC BD				1					●			
FUNCTION GENERATOR PC BD				●		1			1			
DIGITAL MODULE				1		●			●			●
DUPLEX GENERATOR									3			
O'SCOPE CONTROL PC BD										●	●	
CRT POWER SUPPLY PC BD										●	●	
ANALYZER RF MODULE										●		
ANALYZER IF MODULE										●		
ANALYZER LOG AMP MODULE										●		
ENCODE/DECODE PC BD												●

● CALIBRATION REQUIRED

1 CALIBRATION REQUIRED ONLY IF MODULE FAILS PERFORMANCE EVALUATION

2 COMPLETE STEPS 29 THRU 31 IN CALIBRATION PROCEDURE 4-2-8.

3 COMPLETE STEPS 17 THRU 21 IN CALIBRATION PROCEDURE 4-2-9.

4 COMPLETE 10.7MHz GEN/REC CALIBRATION PRIOR TO MODULATION METER CALIBRATION

Figure 4-1 Module Replacement & Alignment Requirements

4-2-1 MECHANICAL ZERO OF METERS

PREREQUISITES: None

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Small Slotted Screwdriver

INITIAL CONTROL SETTINGS: See Figure 1-2

CONTROL		INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"OFF"
2	Modulation Meter Zero Adjustment	As is
38	Frequency Error Meter Zero Adjustment	As is

STEP PROCEDURE

1. Set FM/AM-1200S/A in an upright position, resting on rear panel.

2. Adjust Modulation Meter Zero Adjustment (3) as required to position the MODULATION METER (1) needle directly over the "0" on the meter scale. Gently tap on meter face plate to ensure that the needle is not sticking and that it settles to "0".

3. Adjust Frequency Error Meter Zero Adjustment (38) as required to position the FREQ ERROR Meter (36) needle directly over the "0" on the meter scale. Gently tap on meter face plate to ensure that the needle is not sticking and that it settles to "0".

4. Check all knobs on front panel for the following:

   a. Correct alignment to front panel.

   b. Correct range stops.

   c. Knobs are securely tightened to control shafts.

   d. Knobs are close to front panel, but do not bind.

4-2-2 POWER SUPPLY CALIBRATION

PREREQUISITES: None

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool
1 Digital Multimeter
1 Battery Load Simulator (See Appendix D)

INITIAL CONTROL SETTINGS: See Figure 1-2

CONTROL	INITIAL SETTING
22 PWR/OFF/BATT Switch	"OFF" (Battery Power Off)

CALIBRATION POINTS: See Figure 4-10

STEP PROCEDURE

1. With external power disconnected, remove test set from its case.

2. Connect test set to appropriate AC line supply, then place test set on its Rear Panel (Front Panel facing up). Place PWR/OFF/BATT Switch (22) in "PWR" position.

3. On the Battery Charger PC Board, verify voltage between FL3903 and ground (FL3901) is a minimum of +14 VDC.

4. Verify voltage at FL3907 is +12 VDC (±0.1V). Adjust R1520 (+12V ADJ), as needed, to bring the voltage into tolerance.

5. Verify the following voltages are within the indicated tolerance:

TEST POINT	VOLTAGE
FL3904	+5.1 VDC (±0.2V)
FL3905	-12 VDC (±0.5V)
FL3906	+40 to +50 VDC

NOTE: Adjust R1520, as needed, to bring the voltage into tolerance for FL3905 and FL3906. Adjust R1537 as needed, to bring the voltage into tolerance for FL3904.

6. Disconnect the battery and connect a Battery Load Simulator across the pins of J1702. Set Battery Load Simulator for 300 mAmps.

STEP	PROCEDURE

7. Verify the voltage across the Battery Load Simulator is +14.4 VDC (±0.1V). Adjust R1604 (CHARGE ADJ), as needed, to bring the voltage into tolerance. Repeat Steps 6 and 7 as necessary.

8. Disconnect all test equipment.

4-2-3 FREQUENCY STANDARD CALIBRATION

PREREQUISITIES: Power Supply Calibration Procedure (4-2-2)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool

1 Digital Multimeter

1 Frequency Counter

INITIAL CONTROL SETTINGS: See Figure 1-2

CONTROL	INITIAL SETTING
22 PWR/OFF/BATT Switch	"PWR"

CALIBRATION POINTS: See Figure 4-10

STEP	PROCEDURE

1. After a 15-minute warmup period (30-minutes for Opt-02), connect frequency counter to the 10 MHz External Reference Connector (45) and a digital voltmeter to pin 2 (wiper) of R3501, REF CAL potentiometer (13).

2. Verify frequency is 10 MHz (±0.1 Hz) and voltage is +5.5 VDC (±2.0V) or +2.5 VDC (±1.0V) if Oven Oscillator is installed. Adjust R3501, as needed, for correct frequency. If frequency cannot be corrected within the voltage tolerance, proceed with Steps 3 through 5.

3. Reset voltage at pin 2 of R3501 to +5.5 VDC (no tolerance) for TCXO or +2.5 VDC (no tolerance) for Oven Oscillator.

4. Remove adjustment access screw from the TCXO or Oven Oscillator. Adjust the Oscillator to 10 MHz (±0.5 Hz, nominally ±0.1 Hz). Replace adjustment access screw.

5. If further fine adjustment is required, adjust R3501 as required to obtain a frequency of 10 MHz (±0.1 Hz).

6. Disconnect all test equipment.

4-2-4 FUNCTION GENERATOR CALIBRATION

PREREQUISITES: Power Supply Calibration Procedure (4-2-2)
Frequency Standard Calibration Procedure (4-2-3)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool
1 Frequency Counter
1 Distortion Analyzer
1 Digital Multimeter
1 Tone Generator Extender Board
1 150Ω 1/2 W Resistor

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector Control	"REC"
40	VOLUME Control	Fully ccw
41	SQUELCH Control	Fully ccw
5	VAR Tone Selector Switch	"OFF"
6	VAR Tone Level Control	Fully ccw
7	1 kHz Tone Selector Switch	"OFF"
8	1 kHz Tone Level Control	Fully ccw

CALIBRATION POINTS: See Figure 4-10

STEP	PROCEDURE

1. Connect 150Ω, 1/2 W resistor across TONE OUT Connector (17) on Front Panel. Connect Digital Multimeter and Distortion Meter across the resistor.

2. Set 1 kHz Tone Selector Switch (7) to "INTL" and rotate 1 kHz Tone Level Control (8) to obtain 2.5 VRMS. Verify distortion is less than 0.5%.

3. Set 1 kHz Tone Selector Switch (7) to "OFF" position and VAR Tone Selector Switch (5) to "INTL".

4. Use Keyboard (18) to select TONE of 5000.0 Hz SINE.

5. Adjust VAR Tone Level Control (6) to obtain 2.5 VRMS.

6. Connect Frequency Counter to TONE OUT Connector (17) and verify frequency is 5000.0 Hz (±0.5 Hz). If frequency is within tolerance, go to Step 8.

7. Set the PWR/OFF/BATT Switch (22) to the "OFF" position and proceed as follows:

   a. Disconnect the Ribbon Cable from J3101 and remove the Function Generator PC Board from the FM/AM-1200S/A.

   b. Connect an Extender Cable to J3101.

   c. Set PWR/OFF/BATT Switch (22) to "PWR" position.

   d. Verify test set is in the TONE mode, producing a 5000.0 Hz sine wave at 2.5 VRMS across the 150Ω resistor.

   e. With the Frequency Counter connected to the TONE OUT Connector (17), adjust C3110 on the Function Generator PC Board to obtain a frequency of 5000.0 Hz (±0.5 Hz).

   f. Remove the Extender Cable and reset the Function Generator PC Board into the test bed, reconnecting the Ribbon Cable to J3101.

8. With the Distortion Analyzer connected across the 150Ω resistor, verify distortion is less than 0.7%.

9. Use Keyboard (18) to select TONE, 1000.0 Hz SINE.

10. Verify the signal level is 2.5 VRMS. Adjust VAR Tone Level Control (6), if necessary, to obtain desired reading.

11. Verify distortion is less than 0.7%.

12. Disconnect Distortion Analyzer.

13. Set the FM/AM-1200S/A controls as follows:

	CONTROLS	SETTING
39	MODE Selector Control	"GEN"
3	Modulation Select Control	"FM MID"
5	VAR Tone Selector Switch	"INTL"
6	VAR Tone Level Control	"4 kHz Deviation"
24	VERTICAL Attenutor Selector Control	"2 kHz/Div"
26	HORIZONTAL Sweep Selector Control	"0.1 ms/Div" (FM/AM-1200S) "100 µs/DIV" (FM/AM-1200A)

14. Use Keyboard (18) to verify Sine, Ramp, Square and Triangle waveforms are displayed on both VFD (37) and CRT (31).

4-2-5 HIGH LOOP AND FAST LOW LOOP CALIBRATIONS

PREREQUISITES: Meter Zero Calibration Procedure (4-2-1)
Power Supply Calibration Procedure (4-2-2)
Frequency Standard Calibration Procedure (4-2-3)

SPECIAL ACCESSORY EQUIPMENT REQ'D: See Appendix B for Test Equipment Requirements

1 Non-conducting Tuning Tool
1 Frequency Counter
1 Digital Multimeter
1 Synthesized Spectrum Analyzer
1 TF-30: Tune Fixture (see Appendix D)
1 2 to 3 Foot Coax Cable w/SMB-SMB Connectors
2 2 to 3 Foot Coax Cable w/BNC-SMB Connectors
1 BNC Tee Connector
1 Male-Male SMB Connector
1 Coax Jumper SMB-SMB Female Connectors
1 Coax w/Alligator Clip or Banana Adapter

INITIAL CONTROL SETTINGS: See Figure 1-2

CONTROL	INITIAL SETTING
22 PWR/OFF/BATT Switch	"PWR"

CALIBRATION POINTS: See Figure 4-10

4-2-5-1 CALIBRATION

STEP	PROCEDURE
1.	Disconnect P/J1902 and P/J1903 on the Dual VCO Module.
2.	Connect Frequency Counter to J1902.
3.	Verify frequency is 1210 MHz (±1 MHz). Adjust C2003 on the Dual VCO Module, as needed, for correct frequency.

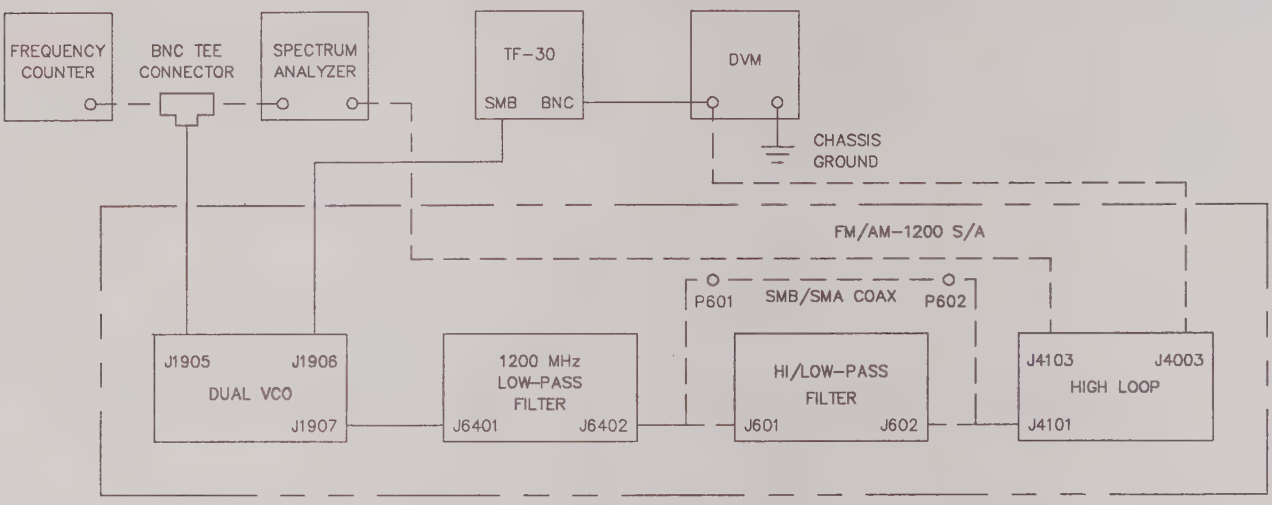


Figure 4-2 High Loop Calibration Test Setup

4. Connect Equipment and Modules per Figure 4-2.

5. Select RF 299.0000 MHz on FM/AM-1200S/A Keyboard (18).

6. Adjust the TF-30 to obtain the following VCO frequencies. Record the corresponding DC voltages:

   a. 2330 MHz, V: _____

   b. 1275 MHz, V: _____

7. Disconnect the Digital Voltmeter (DVM) from the TF-30. Connect the DVM to J4003 on the High Loop Module.

8. Tune the VCO below 1598 MHz. Verify the DC voltage of J4003 corresponds with the voltage recorded in Step 6.a. for 2330 MHz. Adjust R4061 (HIGH LIMIT) on the High Loop Module, as needed, for correct voltage.

9. Tune the VCO above 1800 MHz. Verify the DC voltage of J4003 corresponds with the voltage recorded in Step 6.b. for 1275 MHz. Adjust R4060 (LOW LIMIT) on the High Loop Module, as needed, for correct voltage.

10. Verify the VCO output level at J1905 is +5 to +12 dBm. Verify VCO mixed output at J1907 > -30 dBm (-27 to -25 dBm, typical).

11. Disconnect all test equipment.

STEP	PROCEDURE

12. Reconnect P/J1905, P/J1906 and P/J4003. Verify the PHASE-LOCK Indicator (DS4001) on the High Loop Module remains off.

13. Connect DVM to FL601 on the Hi/Low-pass Filter and connect the Spectrum Analyzer, using an SMB Tee Connector, to J4101.

14. Set RF to 450 MHz on the FM/AM-1200S/A and 540 MHz on the Spectrum Analyzer. Verify approximately +10 VDC on the DVM and the signal level displayed on the Spectrum Analyzer is above -35 dBm.

15. Reset RF to 490 MHz on the FM/AM-1200S/A and 580 MHz on the Spectrum Analyzer. Verify voltage changes to approximately -10 VDC and the signal level displayed on the Spectrum Analyzer is above -35 dBm.

16. If the voltages and signal levels in Steps 14 and 15 are good, disconnect the jumper between P601 and P602, then connect P/J601 and P/J602 and continue at Step 20; otherwise, adjust R4065 ccw until approximately -10 VDC is obtained on the DVM.

17. Reset the RF to 450 MHz on the FM/AM-1200S/A and 540 MHz on the Spectrum Analyzer. Check for approximately +10 VDC and -35 dBm.

18. If either the voltage or the signal level is off, readjust R4065 and repeat this procedure from Step 14.

19. Disconnect the jumper between P601 and P602; then connect P/J601 and P/J602. Increase the frequency in 10 MHz steps to 490 MHz on the FM/AM-1200S/A. Verify the voltage changes from +10 VDC to -10 VDC and the signal level on the Spectrum Analyzer remains constant, except momentarily, where the cross-over from a positive to a negative voltage occurs.

20. Verify the signal level on the Spectrum Analyzer is at least -35 dBm at 290 MHz and at 890 MHz.

    NOTE: These frequencies correspond with 200 MHz and 800 MHz on the FM/AM-1200S/A.

21. Disconnect the Spectrum Analyzer from J4101 and reconnect P/J4101.

22. Connect Spectrum Analyzer to J1902 on the Dual VCO Module. Verify the output is 1210 MHz from +5 to +12 dBm (see Figure 4-3).

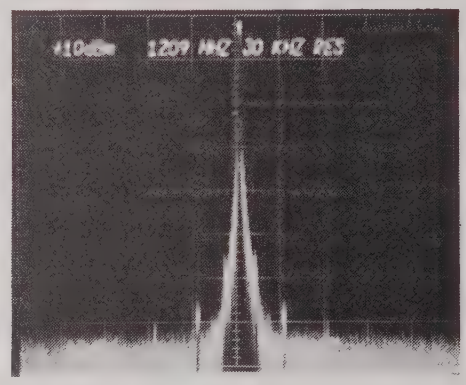


Figure 4-3 DUAL VCO 1210 MHz Output

23. Use the Keyboard (18) to select RF 998.0000 MHz.

24. Set the following controls on the Spectrum Analyzer:

CONTROL	SETTING
Center Frequency	1210 MHz
Scan Width	500 kHz/Div

25. Adjust R4032 (NULL ADJ) on the High Loop Module for the lowest sidebands level.

26. Disconnect the Spectrum Analyzer from J1902 on Dual VCO Module.

27. Reconnect P/J1902 and connect Spectrum Analyzer to J4103 on High Loop module.

28. (FM/AM-1200S ONLY)

    a. Set the following controls on the external Spectrum Analyzer:

CONTROL	SETTING
Center Frequency	600 MHz
Scan Width	100 MHz/Div
Scale	1 or 2 dB

    b. Verify 0 dBm (±5 dB) output level at 1088 MHz (see Figure 4-4).

    NOTE: This output level should read 998 MHz on the UUT.

    c. Reset the RF on the FM/AM-1200S to 50.0000 MHz.

d. Reset the following controls on the Spectrum Analyzer:

CONTROL	SETTING
Center Frequency	140 MHz
Scan Width	10 kHz/Div

e. Verify High Loop output level is 0 dBm (±5 dB).

f. Go to Step 30.

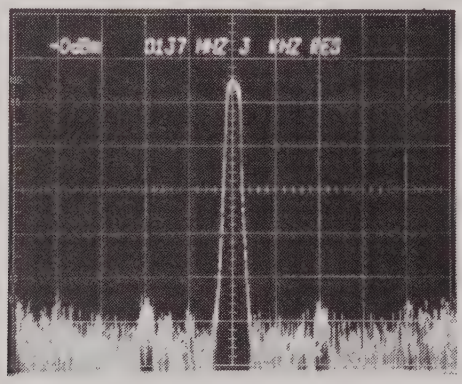


Figure 4-4 DUAL VCO 90 MHz to 1080 MHz Output

29. (FM/AM-1200A ONLY)

a. Set the following controls on the external Spectrum Analyzer:

CONTROL	SETTING
Center Frequency	600 MHz
Scan Width	100 MHz/Div
Scale	1 or 2 dB

b. Verify -20 dBm (±5 dB) output level at 1088 MHz (see Figure 4-4).

c. Reset the RF on the FM/AM-1200A to 50.0000 MHz.

d. Reset the following controls on the external Spectrum Analyzer:

CONTROL	SETTING
Center Frequency	140 MHz
Scan Width	10 kHz/Div

e. Verify High Loop output level is -20 dBm (±5 dB).

30. (ALL UNITS)

Adjust R4045 (GAIN ADJ) on the High Loop Module, as needed, to obtain flat sidebands.

31. Use Keyboard (18) to select the following frequencies. Verify at each frequency, the noise floor level rises not more than 6 dB on the sidebands. Repeat Steps 23 through 30 if this level is not obtained.

FREQUENCY OF FM/AM-1200S/A	SPECTRUM ANALYZER CENTER FREQUENCY
250.0000 MHz	340 MHz
450.0000 MHz	540 MHz
850.0000 MHz	940 MHz

32. Disconnect Spectrum Analyzer from J4103.

33. Connect Frequency Counter to J4103.

34. Verify digital operation on Frequency Counter with FM/AM-1200S/A frequency selection as follows:

FREQUENCY OF FM/AM-1200S/A	DUAL VCO OUTPUT FREQUENCY (J4103)
666.0000 MHz	756 MHz
998.0000 MHz	1088 MHz

4-2-5-2 FAST LOW LOOP CALIBRATION

CAUTION: TO PERFORM THE FOLLOWING CALIBRATION, THE FAST LOW LOOP MODULE MUST BE REMOVED FROM THE TEST SET AND THE PC BOARD REMOVED FROM ITS CANISTER. IT IS THE TECHNICIAN'S RESPONSIBILITY TO SEE THAT ALL DISCONNECTS AND RE-CONNECTS ARE CORRECT BEFORE PROCEEDING. DO NOT REMOVE SHIELDS FROM PC BOARDS.

STEP	PROCEDURE
1.	Set Spectrum Analyzer to measure 75.2 MHz.
2.	Connect Probe to pin 15 of MXR57001.
3.	Tune L57006 and L57007 to maximize 75.2 MHz signal.
4.	Disconnect Spectrum Analyzer.
5.	Verify voltage at TP57003 is between 1 and 3 VDC.
6.	Use Keyboard (18) to set FM/AM-1200S/A RF to 100.0000 MHz.
7.	Connect Frequency Counter to pin 15 of U57001 and Digital Voltmeter to TP57002.
8.	Verify voltage at TP57002 is 8.0 VDC (±0.25V) and frequency at pin 15 of U57001 is 205.0000 MHz.
9.	Adjust L57005, as needed, for proper voltage.
10.	Connect Frequency Counter to J58004 and Digital Voltmeter to TP57001.
11.	Verify voltage at TP57001 is 9.0 VDC (±0.25V) and frequency at J58004 is 79.3000 MHz.
12.	Adjust L58001, as needed, for proper voltage.
13.	Connect Frequency Counter to J58003.

14. Use Keyboard (18) to select the following frequencies. Verify each frequency on the Frequency Counter.

FM/AM-1200S/A Frequency	Counter
000.1000	79.2000 MHz
000.3000	79.0000 MHz
001.1234	78.1766 MHz
001.5678	77.7322 MHz
001.9999	77.3001 MHz

NOTE: Lock Indicator should remain off for all settings.

15. Disconnect all test equipment.

4-2-6 DIGITAL MODULE CALIBRATION

PREREQUISITES: Meter Zero Calibration Procedure (4-2-1)
Power Supply Calibration Procedure (4-2-2)
Frequency Standard Calibration Procedure (4-2-3)

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Non-Conductive Tuning Tool
1 2 to 3 Foot Coax Cable with BNC-to-BNC Connector

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT	"PWR"
5	VAR Tone Switch	"OFF"
7	1 kHz Tone Switch	"OFF"
35	FREQ ERROR Meter Range Selector Control	"10 kHz"
40	VOLUME Control	Fully ccw
41	SQUELCH Control	Fully ccw
39	MODE Selector	"REC"

CALIBRATION POINTS: See Figure 4-5

STEP	PROCEDURE
1.	Select RF 10.0000 MHz on Keyboard (18).
2.	Connect the coax cable to the ANT Connector (34) and the 10 MHz External Reference Connector (45).
3.	Verify Frequency Error Meter (36) reads "0". Adjust R4407 (ZERO) on the Digital Module, if necessary, to position the needle directly over the "0" point.
4.	Select RF 10.0100 MHz on the Keyboard (18).
5.	Verify Frequency Error Meter (36) reads full scale negative deflection (-1 on the upper scale). Adjust R4510 (X10 CAL) on the Digital Module, if necessary, to obtain the correct reading.
6.	Select RF 10.0030 MHz on the Keyboard (18).
7.	Rotate FREQ ERROR Meter Range Selector (35) to the 3K position.
8.	Verify Frequency Error Meter (36) reads full scale negative deflection (-3 on the upper scale). Adjust R4509 (X3 CAL) on the Digital Module, if necessary, to obtain the correct reading.
9.	Disconnect all test equipment.

4-2-7 10.7 MHz GENERATE/RECEIVE CALIBRATION PROCEDURE

PREREQUISITES:
- Mechanical Zero of Meters (4-2-1)
- Power Supply Calibration (4-2-2)
- Frequency Standard Calibration (4-2-3)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

- 1 Digital Multimeter
- 1 RF Signal Generator
- 1 Audio Distortion Analyzer
- 1 Modulation Meter (Optional)*
- 1 DC Coupled Oscilloscope (Optional)
- 1 Extender Cable

* Use if Modulation Meter on FM/AM-1200S/A is out of calibration.

REFERENCES:
- SECTION 6: 10.7 MHZ GENERATE/RECEIVE PC BOARD AND SCHEMATIC
- FIGURE 4-10: LOCATION OF CALIBRATION ADJUSTMENTS AND TEST POINTS

CAUTION: TO PERFORM THE FOLLOWING CALIBRATION, THE 10.7 MHZ GEN/RECV MODULE MUST BE REMOVED FROM THE TEST SET AND THE PC BOARD REMOVED FROM ITS CANISTER. IT IS THE TECHNICIAN'S RESPONSIBILITY TO SEE THAT ALL DISCONNECTS AND RE-CONNECTS ARE CORRECT BEFORE PROCEEDING. DO NOT REMOVE SHIELDS FROM PC BOARDS.

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTING
32	GEN/LOCK Control	"LOCK"
39	MODE Selector Control	"REC"
41	SQUELCH CONTROL	Fully ccw
3	MODULATION Select Control	"FM NAR"
5	VAR Tone Selector Switch	"OFF"
7	1 KHz Tone Level Control	"OFF"
18	Keyboard	"RF 10.7000 MHz"

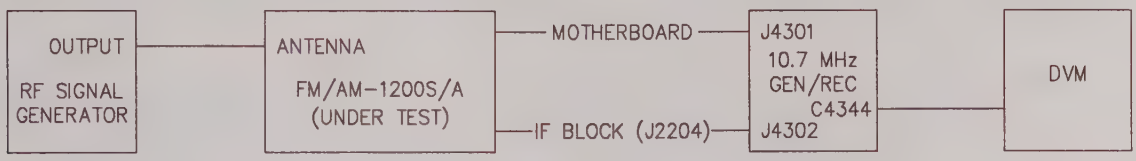


Figure 4-5 Setup for AM Detector Calibration

AM Detector Calibration

1. Disconnect coaxes and ribbon cables from the 10.7 MHz Generate/ Receive PC Board and remove the 10.7 MHz Generate/Receive Module from the FM/AM-1200S/A.

2. Connect the extender cable from the open end of the ribbon cable to J4301 and re-connect J2204 from the IF Block to J4302.

3. Attach a positive Voltmeter lead (and optionally a DC Coupled Oscilloscope) to C4344 on the 10.7 MHz Generate/Receive PC Board.

4. Jumper R4339 to ground to prevent AGC from interfering with the calibration.

5. Connect a coax from the RF Signal Generator to the ANTENNA Connector (34).

6. Select the following controls on the RF Signal Generator:

CONTROL	SETTING
FREQUENCY	10.7 MHz
Signal LEVEL	-90 dBm
MODULATION	CW

7. Set the FM/AM-1200S/A PWR/OFF/BATT Switch (22) to "PWR".

8. Adjust the AGC Trimpot (R4385), as needed, until the DC output begins to slew. The DC Voltmeter reading should have the ability to be slewed freely when the strength of the 10.7 MHz signal is varied.

9. Adjust FL4301 through FL4305 and FL4307 to maximum positive voltage.

   NOTE: If the DC voltage becomes saturated ("railed") during tuning (at about +7V), reduce the AGC level until the DC output begins to drop before continuing. It may be necessary to perform this adjustment several times.

10. Repeat Steps 8 and 9, as needed to maximize the level of the filters.

11. R4385 should be adjusted to display +6 VDC on the Voltmeter.

12. Reset the RF Signal Generator level to -110 dBm. Verify at least 2.5 VDC (4.0 VDC, typically) on DC Coupled Oscilloscope.

13. Reset the MODULATION Meter Control (4) to "FM MID". Verify the Voltmeter reading does not change.

14. Remove the Jumper from R4339, the Voltmeter lead from C4344 and the coax from the RF Signal Generator.

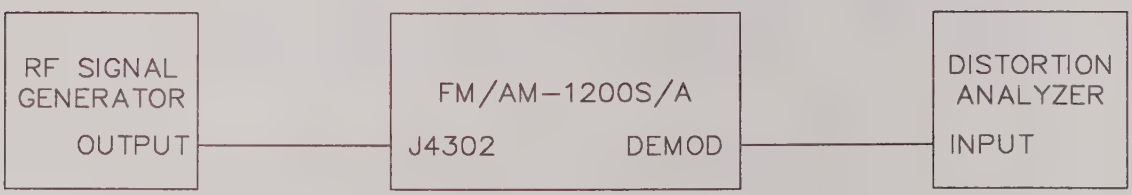


Figure 4-6 AM/FM Distortion Calibration Setup

FM Distortion Test

15. Set the following RF Signal Generator controls:

CONTROL	SETTING
FREQUENCY	10.7 MHz
AMPLITUDE	-40 dBm
MODULATION	50 kHz deviation, 1 kHz rate

16. Attach a coax from the output of the RF Signal Generator to J4302.

17. Set the following FM/AM-1200S/A controls:

	CONTROL	SETTING
18	Keyboard	"RF 10.7000 MHz" ENTER
24	VERTICAL Attenuator Selector Control	"20 kHz/%X10"
26	HORIZONTAL Sweep Selector Control	"0.1 ms/Div"
3	MODULATION Select Control	"FM MID"
32	GEN/LOCK Control	"LOCK"
39	MODE Selector Control	"REC"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
41	SQUELCH Control	Fully ccw

18. Attach a coax from the DEMOD Connector (16) to the input of the Distortion Analyzer.

19. Set the Distortion Analyzer to display Voltage.

20. Adjust L4320 for maximum RMS voltage reading on the Distortion Analyzer.

21. Verify 3 VRMS (±0.3V) reading on the Distortion Meter. Typical reading is 3.2 to 3.3 VRMS.

22. The signal appearing on the FM/AM-1200S/A Oscilloscope display should be a clean sine wave of 5 major divisions.

    NOTE: The Oscilloscope display may be inaccurate as the Oscilloscope on the FM/AM-1200S/A has not been calibrated prior to this procedure. An external Oscilloscope may be needed to verify a clean signal.

23. Set the Distortion Analyzer to display Voltage.

24. Verify distortion not more than 1.5% (1.3% to 1.5%, typical).

25. Reset MODULATION Select Control (3) to "FM NAR" and Vertical Attenuator Selector Control (24) to "2 kHz/%X10".

26. Reset MODULATION on RF Signal Generator to "5 kHz Deviation, 1 kHz Rate".

27. Set the Distortion Analyzer to display Voltage.

STEP	PROCEDURE

28. Adjust FL4303 and FL4304 for minimum distortion on the Distortion Analyzer.

    NOTE: These should be fine adjustments. Excessive adjustments to these components at this time may indicate problems in calibrating this board.

29. Verify 3.0% distortion or less (typical reading 1.6% to 2.0%).

30. Repeat Steps 17 through 29, making only minor adjustments, as needed.

AM Distortion Calibration

31. Reset the following FM/AM-1200S/A controls:

CONTROL	SETTING
3 MODULATION Select Control	"AM NORM"
24 VERTICAL Attenuator Selector Control	"2 kHz/%X10"
26 HORIZONTAL Sweep Selector Control	"0.1 ms/Div"
41 SQUELCH Control	Fully ccw

32. Reset MODULATION Control on the RF Signal Generator to 80% AM, 1 kHz rate.

33. Set the Distortion Analyzer to display Voltage.

34. Verify not more than 3.0% distortion. The signal on the FM/AM-1200S/A Oscilloscope should be a clean sine wave of 8 major vertical divisions.

    NOTE: Refer to note after Step 22.

35. Set the Distortion Analyzer to display Voltage.

36. Set the %MODULATION on the RF Signal Generator just enough to set the Modulation to 15% on the Distortion Analyzer.

    NOTE: This level may vary due to error in the Distortion Analyzer.

37. Set the MODULATION Select Control (3) on the FM/AM-1200S/A to "AM NAR".

38. Verify not more than 1% distortion on the Distortion Analyzer.

39. Disconnect the RF Signal Generator coax from J4302.

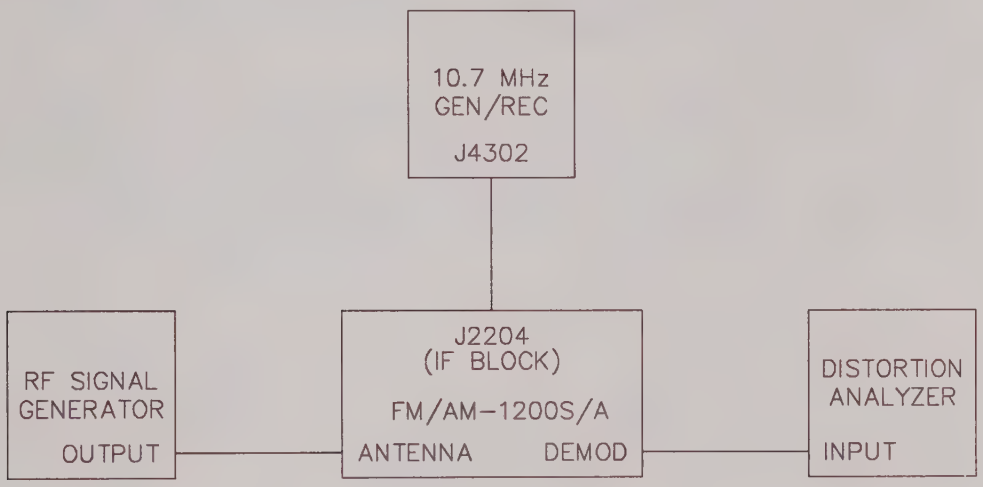


Figure 4-7 Squelch Calibration Setup

Squelch Test

40. Connect Coaxes from J2204 of IF BLOCK to the J4302 of 10.7 MHz Generate/Receive PC Board, J4303 to J4401 of Digital PC Board, and J4304 to J4502 of Digital PC Board.

41. Reset the following FM/AM-1200S/A controls:

CONTROL	SETTING
3 MODULATION Select Control	"FM NAR"
18 Keyboard	"RF 120.2000 MHz"
41 SQUELCH Control	Fully ccw

42. Set the following RF Signal Generator controls:

CONTROL	SETTING
MODULATION	CW
FREQUENCY	120.2 MHz
AMPLITUDE	-115 dBm

43. Adjust the SQUELCH Control (41) until the Signal (SIG) Indicator (42) in the upper right corner of the MODULATION METER (1) just breaks squelch.

44. Connect a coax from the RF Signal Generator to the ANT Connector (34).

45. Adjust R4385 to the point where the Signal Indicator (42) just breaks squelch.

46. Set the RF Signal Generator Level to -114 dBm to verify the Signal Indicator (42) turns on. Reset the RF Signal Generator level to -115 dBm. Verify the Signal Indicator in the MODULATION METER (1) turns off. Disconnect RF Signal Generator from ANTENNA Connector (34). Repeat Steps 43 through 46, as needed.

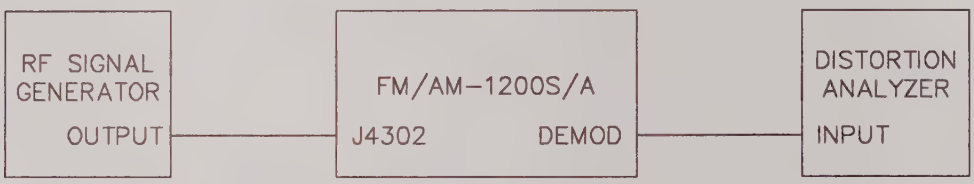


Figure 4-8 Receive Sensitivity Calibration Setup

Receive Sensitivity Test (10 dB SINAD)

47. Reset the following FM/AM-1200S/A controls:

CONTROL	SETTING
18 KEYBOARD	"RF 10.7000 MHz" ENTER
41 SQUELCH Control	Fully ccw

48. Attach a coax from J4302 to the Output Connector of the Signal Generator.

49. Set the following RF Signal Generator controls:

CONTROL	SETTING
FREQUENCY	10.7 MHz
AMPLITUDE	-90 dBm
MODULATION	3.3 kHz Deviation, 1 Hz rate

50. Attach a coax from the DEMOD Connector (16) to the Input Connector on the Distortion Analyzer.

51. Set the following Distortion Analyzer to read SINAD.

52. Decrease the RF Signal Generator level until the Distortion Analyzer reads 10 dB. Verify RF level is less than -101 dBm.

53. Remove the Distortion Analyzer coax from the FM/AM-1200S/A.

Figure 4-9 Phase-Lock/SSB/Modulation Calibration Setup

Phase-Lock

54. Connect ribbon cable from Motherboard to Ribbon Connector on 10.7 MHz Generate/Receive PC Board.

55. Connect Tee connector from external Spectrum Analyzer or external Frequency Counter to J4302 of 10.7 MHz Generate/Receive PC Board.

56. Connect J4502 of Digital PC Board to J4304 of 10.7 MHz Generate/Receive PC Board.

57. Reset the following FM/AM-1200S/A controls:

CONTROL	SETTING
26 HORIZONTAL Sweep Selector Control	"20 kHz/Div"
39 MODE Selector Control	"GEN"

58. Adjust L4312 to zero the Phase-Lock.

NOTE: Center peak on external Spectrum Analyzer (or external Frequency Counter) to midpoint horizontally on CRT display.

STEP	PROCEDURE

59. Adjust GEN/LOCK Control (32) to just bring GEN LOCK out of detent (i.e., GEN LOCK Switch just turns off). Signal should shift at least 2 major divisions left of the Vertical Center (typical is approximately 2.5 major divisions) graticule on external Spectrum Analyzer (or external Frequency Counter) display.

60. Rotate GEN/LOCK Control (32) fully cw. Signal should shift more than 2 major divisions right of the Vertical Center (typical is approximately 2.5 major divisions) graticule on external Spectrum Analyzer (or external Frequency Counter) display.

61. Readjust L4312, as needed, until signal is equidistant left or right of the Vertical Center Graticule as the GEN/LOCK Control is rotated fully cw and fully ccw.

62. Reset GEN/LOCK Control to LOCK. Signal should be horizontally centered on CRT. Repeat Steps 59 to 62, if needed.

SSB Calibration

63. Reset the following FM/AM-1200S/A controls:

	CONTROL	SETTING
32	GEN/LOCK Control	"LOCK"
39	MODE Selector Control	"REC"
41	SQUELCH Control	Fully ccw
3	MODULATION Select Control	"SSB"
18	Keyboard	"RF 0.0010 MHz" ENTER
24	VERTICAL Attenuator Selector Control	"2 kHz/%X10"
26	HORIZONTAL Sweep Selector Control	"1 ms/Div"

64. Display on external Spectrum Analyzer should appear as a full wave rectified sine wave. Adjust R4351 to maximize display (peak-to-peak). Display should be approximately 6 major divisions in height.

Modulation Check

65. Reset the following FM/AM-1200S/A controls:

	CONTROL	SETTING
39	MODE Selector Control	"GEN"
3	MODULATION Select Control	"FM MID"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"INTL"
4	Modulation METER Control	"60 kHz"
18	Keyboard	"120.2 MHz" 2ND METER

66. Adjust 1 kHz Tone Selector Switch (7) from minimum to maximum. Verify with an external Modulation Meter that the VFD (37) reads from zero to at least 50 kHz deviation.

67. Reset the following FM/AM-1200S/A controls:

	CONTROL	SETTING
3	MODULATION Select Control	"AM NORM"
4	Modulation METER Control	"20 kHz/%X10"

68. Adjust 1 kHz Tone Selector Switch (7) from minimum to maximum. Verify with an external Modulation Meter that the VFD (37) reads from zero to at least 100% modulation.

69. Disconnect all test equipment and connect all coaxes per system block diagram.

70. Verify only Steps 15 through 46 and Steps 54 through 64 with the 10.7 MHz Generate/Receive Module enclosed in its Canister.

NOTE: Adjustments cannot be made to 10.7 MHz Gen/Recv Module when enclosed in its canister, except L4312 (PHASE-LOCK).

4-2-8 MODULATION METER CALIBRATION

PREREQUISITES: Meter Zero Calibration Procedure (4-2-1)
Power Supply Calibration Procedure (4-2-2)
Frequency Standard Calibration Procedure (4-2-3)
10.7 MHz Generate/Receive Calibration Procedure (4-2-7)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool
1 RF Signal Generator with Attenuator
1 Oscilloscope
1 Distortion Analyzer
1 Digital Multimeter
1 Modulation Meter
1 5 Watt Transmitter
1 30 Watt Transmitter

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector	"GEN"
3	MODULATION Select Control	"FM NAR"
4	Modulation METER Control	"AVG 15"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
9	GEN LEVEL Vernier	Fully ccw
10	GEN LEVEL Attenuator	"-20 dBm"
18	Keyboard	"RF 120.2000 MHz"

CALIBRATION POINTS: See Figure 4-10

STEP	PROCEDURE
1.	Verify modulation reads zero on MODULATION METER (1). Adjust R3354 (POWER ZERO) on the Receive Audio PC Board, as necessary, to obtain zero reading.
2.	Connect 5 Watt Transmitter to T/R Connector (11).
3.	Key Transmitter and verify MODULATION METER (1) reads 5W Avg (see Specifications in Appendix A).
4.	Adjust R3365 (15W CAL) on the Receive Audio PC Board, as necessary, to obtain correct reading.
5.	Disconnect Transmitter.

STEP	PROCEDURE

6. Place Modulation METER Control (4) to "AVG 150" position.

7. Connect 30 Watt Transmitter to T/R Connector (11).

8. Key Transmitter and verify MODULATION METER (1) reads 30W Avg (see Specifications in Appendix A).

9. Adjust R3362 (150W CAL) on the Receive Audio PC Board, as necessary, to obtain correct reading.

10. Disconnect Transmitter.

11. Place Modulation METER Control (4) to "BATT" position.

12. Connect Multimeter to J1601, Pin 5 on Battery Charger PC Board. Verify reading on MODULATION METER (1) is the same as the Multimeter.

13. Adjust R3303 (BATT CAL) on the Receive Audio PC Board, as necessary to obtain correct reading.

14. Place MODULATION Select Control (3) to "FM NAR" position and Modulation METER Control (4) to "2 kHz" position.

15. Verify MODULATION METER (1) on FM/AM-1200S/A indicates zero. Adjust R3368 (FM GEN ZERO) on the Receive Audio PC Board, if necessary, to position the needle directly over the zero division mark.

16. Set the FM/AM-1200S/A controls as follows:

CONTROL		SETTING
3	MODULATION Select Control	"AM NORM"
4	Modulation METER Control	"6 kHz/%X10"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"INTL"

17. Connect an external Modulation Meter to the T/R Connector (11).

18. Adjust 1 kHz Tone Level Control (8) for a reading of 50% AM on external Modulation Meter.

19. Adjust R3436 (GEN AM% CAL) on the Receive Audio PC Board, if necessary, for a reading of 50% AM on the MODULATION METER (1).

20. Set 1 kHz Tone Selector Switch (7) to "OFF" position. Disconnect external Modulation Meter.

21. Set MODE Selector Control (39) to "REC" position.

22. Adjust RF Signal Generator to produce an unmodulated signal of 120.2 MHz at -50 dBm.

23. Connect the RF Signal Generator to the FM/AM-1200S/A ANT Connector (34).

24. Calibrate the modulation function of the MODULATION METER (1) as follows:

    NOTE: Refer to Table 4-1, Test Sequences 1 through 9.

    a. For each test sequence, set RF Signal Generator as shown in Table 4-1.

    b. Set FM/AM-1200S/A as shown in Table 4-1 for each test sequence. Verify the readings are within tolerance. Adjust the specified trimpot as required to obtain the correct reading.

25. Verify FM/AM-1200S/A demodulation distortion as follows:

    NOTE: Refer to Table 4-1, Test Sequences 10 through 12.

    a. Using Coax "Tee", connect Digital Multimeter to DEMOD Connector (16) of FM/AM-1200S/A.

    b. For each test sequence, set RF Signal Generator as shown in Table 4-1.

    c. Set FM/AM-1200S/A in each test sequence as shown in Table 4-1.

    d. Connect Distortion Meter to DEMOD Connector (16) of FM/AM-1200S/A, using the Coax Tee, and measure distortion. The observed distortion should be less than the maximum given in Table 4-1 for the appropriate test sequence.

26. Disconnect the RF Signal Generator.

27. Set the FM/AM-1200S/A controls as follows:

	CONTROL	SETTING
39	MODE Selector	"REC"
4	METER Selector	"DIST"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"INTL"
8	1 kHz Level Control	Fully cw

STEP	PROCEDURE

28. Connect coax cable from Tee on TONE OUT Connector (17) to EXT MOD/SINAD Connector (15).

29. Verify MODULATION METER (1) indicates minimum distortion (distortion must be ≤5%). Adjust R3318 (NULL No. 2) and R3320 (NULL No. 1) on the Receive Audio PC Board as necessary to obtain maximum deflection.

30. Adjust 1 kHz Tone Level Control (8) for 1.999 VRMS on Digital Multimeter.

31. Set 1 kHz Tone Selector Switch (7) in "OFF" position and VAR Tone Selector Switch (5) in "INTL" position. Using Keyboard (18) select a variable tone of 1800 Hz Sine wave.

32. Adjust the VAR Tone Level Control (6) for 0.199 VRMS on Digital Multimeter.

33. Place 1 kHz Tone Selector Switch (7) to "INTL" position and Modulation METER Control (4) to "DIST" position.

34. Verify MODULATION METER (1) displays 10% distortion. Adjust R3350 (SINAD CAL) on the Receive Audio PC Board, as necessary, to obtain correct reading.

35. Place 1 kHz Tone Selector Switch (7) to "OFF" position and adjust VAR Tone Level Control (6) for 0.500 VRMS on Digital Multimeter.

36. Place 1 kHz Tone Selector Switch (7) to "INTL" position and Modulation METER Control (4) to "SINAD" position. Verify MODULATION METER (1) reads 12 dB SINAD.

37. Disconnect all test equipment.

Table 4-1 Modulation Meter Calibration Requirements

RF SIGNAL GENERATOR				FM/AM-1200S/A							
TEST SEQ NO.	MOD MODE	TONE FREQ	MOD DEV/%	MODULATION SELECTOR SETTING	METER SELECTIVE SETTING kHz/%X10	METER READING	METER TOL. ±	ADJUST	DEMOD OUTPUT LEVEL VP-P	FM/AM-1200S/A DISTORTION LESS SIGNAL GENERATOR DISTORTION	REMARKS
1	FM	1K	0	FM NAR	2	0	0	R3369			
2	FM	1K	0	FM WIDE	2	0	0	R3380			
3	FM	1K	5K	FM NAR	6	5	±0.43 kHz	R3383			
4	Repeat Test Sequences 1, 2 and 3 as required to obtain proper readings										Sequences 1, 2 and 3 are interactive
5	FM	1K	1.5K	FM NAR	2	1.5	±0.135 kHz	None			Verify Only
6	FM	1K	50K	FM MID	60	5	±4.3 kHz	None			Verify Only
7	AM	1K	0	AM NORM	2	0	0	R3371			
8	AM	1K	80%	AM NORM	20	8	±10% AM	R3379			
9	Repeat Test Sequences 7 and 8 as required to obtain proper readings										Sequences 7 and 8 are interactive
10	FM	1K	5K	FM NAR	6				.85	<3%	Verify Only
11	FM	1K	20K	FM MID	60				8.5	<2%	Verify Only
12	AM	1K	80%	AM NORM	20				1.12	<4%	Verify Only

4-2-9 GENERATE SIGNAL CALIBRATION

PREREQUISITES:
Meter Zero Calibration Procedure (4-2-1)
Power Supply Calibration Procedure (4-2-2)
Frequency Standard Calibration Procedure (4-2-3)
Function Generator Calibration Procedure (4-2-4)
High Loop Calibration Procedure (4-2-5)
Digital Calibration Procedure (4-2-6)
Modulation Meter Calibration Procedure (4-2-8)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool
1 Microphone
1 Function Generator
1 Power Meter
1 Oscilloscope
1 Spectrum Analyzer
1 Modulation Meter

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector Control	"GEN"
32	GEN/LOCK Control	"LOCK"
3	MODULATION Select Control	"AM NORM"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
9	GEN LEVEL Attenuator	"-20 dBm"
10	GEN LEVEL Vernier	Fully ccw

CALIBRATION POINTS: See Figure 4-10

STEP PROCEDURE

1. Using Keyboard (18), enter "RF 120.2000" MHz.
2. Connect Spectrum Analyzer to T/R Connector (11).
3. Vary GEN LEVEL Vernier Control (10) smoothly throughout its full range and verify the output level observed on the Spectrum Analyzer tracks.
4. Connect Modulation Meter to T/R Connector (11).

5. Set the following FM/AM-1200S/A controls:

CONTROL		SETTING
9	RF Level Attenuator Control	Fully ccw
8	1 kHz Tone Level Control	To 50% AM of Modulation (±5%) on MODULATION METER (1)

6. Adjust R5114 (BALANCE), as necessary, through the access hole in the Output Amplifier Module, to obtain the desired reading.

7. Disconnect Modulation Meter and connect Power Meter to T/R Connector (11).

8. Use only the GEN LEVEL Vernier Control (10) to make the following output level settings and verify the output levels on the Power Meter are within 0.5 dB. If necessary, make the corresponding adjustments, listed below, to obtain the correct levels. Repeat these adjustments on the Generate Audio PC Board, as necessary, until all are within tolerance.

Setting	Adjustment
a. -31 dBm	R3224 (+1 CAL)
b. -42 dBm	R3246 (-12 CAL)
c. -37 dBm	R3227 (-7 CAL)

9. Rotate GEN LEVEL Vernier Control (10) to -31 dBm. Select the following RF's on the Keyboard (18) to verify the corresponding Power Meter readings are -31 dBm (±2.5 dB):

200 MHz	500 MHz	800 MHz	1 MHz
300 MHz	600 MHz	900 MHz	10 MHz
400 MHz	700 MHz	999 MHz	100 MHz

10. Connect Function Generator to EXT MOD/SINAD Connector (15).

11. Adjust Function Generator output for a 1 kHz tone at 0.5 VRMS. Verify MODULATION METER (1) shows 50% (±15%).

12. Set MODULATION Select Control (3) to "FM MID" position and Modulation METER Control (4) to "20 kHz/%X10" position.

13. Adjust Function Generator output to 1.5 VRMS at 1 kHz. Verify MODULATION METER (1) displays 15 kHz (4.5 kHz). Disconnect Function Generator from EXT MOD/SINAD Connector (15).

14. Connect Microphone to MIC/ACC Connector (19). Speak into Microphone and verify MODULATION METER (1) peaks no greater than 6 kHz deviation.

STEP	PROCEDURE

15. Rotate the GEN/LOCK Control (32) out of the detent. Verify the LOCK Lamp (33) flashes and the FREQ ERROR Meter (36) indicates a minimum error of -10 kHz.

16. Rotate the GEN/LOCK Control (32) fully cw and verify the FREQ ERROR Meter (36) indicates a minimum error of +10 kHz.

17. Rotate the GEN/LOCK Control (32) fully ccw into "LOCK" position. Verify the LOCK Lamp (33) becomes steady.

18. Set Spectrum Analyzer to 20 MHz/Div and connect to T/R Connector (11). Verify non-harmonic frequencies are a minimum of 40 dBc at the following frequencies:

    600 MHz 700 MHz 470 MHz 120 MHz

19. Rotate MODE Selector Control (39) to "DUP" position.

20. Verify +11 VDC is present on collector of Q1202. Adjust, as necessary, R1251 for proper level.

21. Using Keyboard (18) select RF 070.0000 MHz, set OFFSET to 00.0 and verify Spectrum Analyzer indicates -80 dBm (±5 dB).

22. Connect Spectrum Analyzer to DUPLEX Output Connector (14) and verify output level is -60 dBm (±10 dB). Adjust, as necessary, R1230 for proper level.

23. Connect Frequency Counter to DUPLEX Output Connector (14) and verify 70.000 MHz signal is present. Adjust, as necessary, L1209 for proper frequency.

24. Using BNC-to-BNC Coax Cable, connect DUPLEX Output Connector (14) to ANT Connector (34).

25. Set MODE Selector Control (39) to "DUP GEN" position and 1 kHz Tone Selector Switch (7) to "INTL" position. Adjust 1 kHz Tone Level Control (8) for 5 kHz deviation on MODULATION METER (1).

26. Set MODE Selector Control (39) to "DUP" position.

27. Verify 5 kHz deviation is displayed on MODULATION METER (1). Adjust R1224 (FM DEV CAL) on the Duplex module, as necessary, to obtain desired deviation.

28. Repeat Steps 25 through 27 until 5 kHz deviation is obtained on both scales of the MODULATION METER (1).

29. Disconnect all test equipment.

4-2-10 OSCILLOSCOPE/ANALYZER CALIBRATION (FM/AM-1200S ONLY)

PREREQUISITES:
- Meter Zero Calibration Procedure (4-2-1)
- Power Supply Calibration Procedure (4-2-2)
- Frequency Standard Calibration Procedure (4-2-3)
- Function Generator Calibration Procedure (4-2-4)
- High Loop Calibration Procedure (4-2-5)
- Digital Module Calibration Procedure (4-2-6)
- Modulation Meter Calibration Procedure (4-2-8)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool
1 Digital Multimeter
1 RF Signal Generator
1 DC Power Supply
1 Coax Cable, BNC-to-BNC

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector Control	"GEN"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"1V/DIV"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"TONE"
27	VERT POS Control	MIDRANGE
28	INT Control	MIDRANGE
29	FOCUS Control	MIDRANGE
30	HORIZ POS Control	MIDRANGE

CALIBRATION POINTS: See Figure 4-10

STEP	PROCEDURE

1. Verify trace on CRT is a SHARP ROUND DOT. Adjust, as required, Geometry Control, R317 and Astigmatism Control, R316 on Scope Power PC Board for a sharp round dot.

2. Using INT Control (28) and FOCUS Control (29), verify intensity and focus of trace can be properly adjusted. Alternately adjust R317 and R316, if necessary, for proper control of trace.

STEP	PROCEDURE

3. Set VERTICAL Vernier Control (23) to fully ccw position.

4. Rotate the HORIZONTAL Sweep Selector Control (26) to "0.1 ms/DIV". Verify the trace is parallel to the horizontal lines on the CRT (31). Adjust R322 on Scope Power PC Board, as required, to correct any nonparallel condition. If this adjustment cannot correct the nonparallel condition, reverse P301 on the Scope Power PC Board and readjust R322.

5. Position VERT POS Control (27) so that 0V is present at J203, pin 4. Then adjust R294 on Scope Control PC Board, as required, to properly position trace over major horizontal axis.

6. Rotate the VERTICAL Vernier Control (23) fully cw and verify the trace does not move. Adjust R215 (BAL) on Scope Control PC Board, as necessary, for proper trace operation.

7. Select RF 151.0000 MHz on the Keyboard (18). Rotate the MODE Selector Control (39) to "GEN" and the HORIZONTAL Sweep Selector Control (26) to "1 MHz/DIV".

8. Using HORIZ POS Control (30), center signal over major vertical axis.

9. Verify baseline is visible on CRT (31). Adjust R218 (ANAL VERT GAIN CAL) on Scope Control PC Board, as required, until baseline is visible on CRT (31).

10. Verify trace extends 1 minor division past the left edge of the CRT (31). Adjust R271 (HORIZ SIZE) on Scope Control PC Board, as required, for correct trace position.

11. Verify the trace extends 1 minor division past the right edge of the CRT (31). Adjust R293 on Scope Control PC Board, as required, for correct trace position.

12. Repeat Steps 10 and 11 as required for proper trace positioning on CRT (31).

13. Rotate MODE Selector Control (39) to "REC" position.

14. Adjust RF Signal Generator for 151.0000 MHz at -50 dBm, with no modulation. Connect Generator to ANTENNA Connector (34) and verify the signal displayed on the CRT (31) is centered on the vertical center line.

STEP	PROCEDURE

15. Adjust Signal Generator to 147.0000 MHz and verify signal is 4 divisions to the left of center on the CRT (31). Adjust Generator to 155.0000 MHz and verify signal is 4 divisions to the right of center. Adjust R260 on Scope Control PC Board, as required, for proper dispersion.

16. Place MODE Selector Control (39) to "GEN" position and HORIZONTAL Sweep Selector Control (26) to "1 kHz/DIV" position. Adjust R298 on Scope Control PC Board, as required, to center signal over major vertical axis.

17. Disconnect the Signal Generator and set the FM/AM-1200S controls as follows:

CONTROL		SETTING
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"1V/DIV"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"0.01 ms/DIV"
39	MODE Selector Control	"REC"
21	AC/GND/DC Switch	"DC"

18. Verify trace is centered over major horizontal axis.

19. Connect Power Supply to SCOPE Connector (20) and apply +4 VDC. Verify trace moves up 4 divisions. Adjust R221 (GAIN CAL) on Scope Control PC Board, as required, for correct deflection.

20. Rotate VERTICAL Vernier Control (23) fully ccw and verify the trace shows approximately 0.4V.

21. Set Scope VERTICAL Vernier Control (23) to "CAL" position.

22. Set AC/GND/DC Switch (21) to "AC" position and verify the trace returns to the center line.

23. Set AC/GND/DC Switch (21) to "GND" position and verify the trace does not move.

24. Disconnect the Power Supply and couple the TONE OUT Connector (17) to the SCOPE Connector (20) with a coax cable.

25. Set the FM/AM-1200S controls as follows:

CONTROL		SETTING
5	VAR Tone Selector Switch	"INTL"
6	VAR Tone Level Control	MIDRANGE
21	AC/GND/DC Switch	"DC"
25	Scope HORIZONTAL Sweep Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"1 ms/DIV"

26. Using Keyboard, select "TONE 1000.0 TRIANGLE". Adjust HORIZ POS Control to position first positive peak of signal on leftmost major vertical graticule. Verify each positive peak of the triangle waveform is positioned over each major vertical graticule. Adjust R247 (SWP CAL) on the Scope Control PC Board, if necessary.

27. Rotate the HORIZONTAL Sweep Selector Control (26) to each of the following positions and select the corresponding triangle waveform frequencies with the Keyboard (18). At each selection, verify the CRT (31) shows one cycle per division.

HORIZONTAL SELECTOR	TONE FREQUENCY
a. 10 ms	100 Hz (10%)
b. 1 ms	1,000 Hz (10%)
c. 0.1 ms	10,000 Hz (10%)

28. With the FM/AM-1200S set from Step 27.c., rotate the HORIZONTAL Vernier Control (25) fully ccw and verify a miminum of 10 cycles per division on the CRT (31). Return the HORIZONTAL Vernier Control (25) to the "CAL" (fully cw) position.

29. Set the FM/AM-1200S Controls as follows:

	CONTROL	SETTING
39	MODE Selector Control	"GEN"
3	MODULATION Select Control	"NAR"
4	Modulation METER Control	"6 kHz/%X10"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"INTL"
18	Keyboard	"RF 121.0000 MHz"
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"2 kHz/%X10"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"1 ms/DIV"

30. Adjust the 1 kHz Tone Level Control (8) for 4 kHz deviation on the MODULATION METER (1).

31. Verify the signal displayed on the CRT (31) is 2 divisions peak-to-peak. Adjust R201 (DEMOD CAL) on Scope Control PC Board, as required, for correct display.

32. Place PWR/OFF/BATT Switch (22) to "OFF" position, remove coax cable from TONE OUT Connector (17) to SCOPE Connector (20) and connect Signal Generator to ANT Connector (34).

33. Remove Analyzer Log Amp Assembly and apply power to test set.

34. Using VERT POS Control (27) center trace over major horizontal axis.

35. Place 1 kHz Tone Selector Switch (7) to "OFF" position, VERTICAL Attenuator Selector Control (24) to "1V/Div" position and HORIZONTAL Sweep Selector Control (26) to "1 MHz/Div" position.

36. Using HORIZ POS Control (30) center signal over major vertical axis.

37. Place MODE Selector Control (39) to "REC" position and set Signal Generator to 121.000 MHz @ -40 dBm.

38. Verify CRT (31) displays a signal level of -40 dBm. Adjust R830 (GAIN) and R831 (REF LVL) on Analyzer Log Amp PC Board alternately for desired signal level.

STEP	PROCEDURE

39. Adjust R832 (BASE LINE) to set bottom of the baseline noise floor level at -110 dBm on CRT (31) scale.

40. Repeat Steps 38 and 39 until the peak signal level is set at -40 dBm and noise floor level is set at -110 dBm on CRT (31).

    NOTE: If signal level and baseline noise floor cannot be obtained in Step 29, adjust R218 (ANAL VERT GAIN CAL) on Scope Control PC Board to obtain desired levels.

41. Set Signal Generator to -70 dBm. Adjust R818 (AMP 1 GAIN) on Analyzer Log Amp PC Board for a signal level of -70 dBm on CRT (31).

42. Set Signal Generator to -90 dBm. Adjust R824 (AMP 2 GAIN) on Analyzer Log Amp PC Board for a signal level of -90 dBm CRT (31).

43. Set Signal Generator to -30 dBm. Adjust R812 (LOG LINEARITY) on Analyzer Log Amp PC Board for a signal level of -30 dBm on CRT (31).

44. Repeat Steps 38 thru 43, as necessary to obtain required levels.

45. Set Signal Generator to -40 dBm. Verify signal level is -40 dBm on CRT. Adjust R522 (IF GAIN) on Analyzer IF PC Board, as required, to obtain desired level.

    NOTE: If it is necessary to adjust R543 and/or R559 in the following steps, remove the Analyzer IF PC Board from its "can" and move the Analyzer Log Amp module forward one slot. Then reconnect all coaxes and the ribbon cable. Be sure to insulate the exposed board.

46. Rotate HORIZONTAL Sweep Selector Control (26) to "20 kHz/Div" Position and verify signal level is -40 dBm on CRT (31). Adjust R543 (3 kHz LVL ADJ) on Analyzer IF PC Board, as required, to obtain desired level.

47. Place HORIZONTAL Sweep Selector Control (26) to "1 kHz/Div" Position and verify signal level on CRT (31) is -40 dBm. Adjust R559 (300 Hz LVL ADJ) on Analyzer IF PC Board, as necessary, to obtain desired level.

48. Disconnect test equipment, replace Analyzer Log Amp assembly and FM/AM-1200S cover.

4-2-11 OSCILLOSCOPE CALIBRATION (FM/AM-1200A ONLY)

PREREQUISITES:
Meter Zero Calibration Procedure (4-2-1)
Power Supply Calibration Procedure (4-2-2)
Frequency Standard Calibration Procedure (4-2-3)
Function Generator Calibration Procedure (4-2-4)
High Loop Calibration Procedure (4-2-5)
Digital Module Calibration Procedure (4-2-6)
Modulation Meter Calibration Procedure (4-2-8)

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)

1 Non-Conductive Tuning Tool
1 Digital Multimeter
1 RF Signal Generator
1 Function Generator
1 DC Power Supply
1 Coax Cable, BNC-to-BNC

INITIAL CONTROL SETTINGS:
See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector Control	"GEN"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"1V/DIV"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"TONE"
27	VERT POS Control	MIDRANGE
28	INT Control	MIDRANGE
29	FOCUS Control	MIDRANGE
30	HORIZ POS Control	MIDRANGE

CALIBRATION POINTS:
See Figure 4-10

STEP PROCEDURE

1. Verify trace on CRT is a SHARP ROUND DOT. Adjust, as required, Geometry Control, R317 and Astigmatism Control, R316 on Scope Power PC Board for a sharp round dot.

2. Using INT Control (28) and FOCUS Control (29), verify intensity and focus of trace can be properly adjusted. Alternately adjust R317 and R316, if necessary, for proper control of trace.

STEP	PROCEDURE

3. Set VERTICAL Vernier Control (23) to fully CCW Position.

4. Rotate the HORIZONTAL Sweep Selector Control (26) to "100 µs/DIV". Verify the trace is parallel to the horizontal lines on the CRT (31). Adjust R322 on Scope Power PC Board, as required, to correct any nonparallel condition. If this adjustment cannot correct the nonparallel condition, reverse P301 on the Scope Power PC Board and readjust R322.

5. Adjust VERT POS Control (27) to properly position trace over major horizontal axis.

6. Rotate the VERTICAL Vernier Control (23) fully cw and verify the trace does not move. Adjust R215 (BAL) on Scope Control PC Board, as necessary, for proper trace operation.

7. Repeat Steps 5 and 6, as required, if an adjustment was made.

8. Verify trace extends 1 minor division past the left edge of the CRT (31). Adjust R271 (HORIZ SIZE) on Scope Control PC Board, as required, for correct trace position.

9. Verify the trace extends 1 minor division past the right edge of the CRT (31). Adjust R293 on Scope Control PC Board, as required, for correct trace position.

10. Repeat Steps 8 and 9 as required for proper trace positioning on CRT (31).

11. Set the FM/AM-1200A controls as follows:

	CONTROL	SETTING
39	MODE Selector Control	"REC"
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"1V/DIV"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"10 µs/DIV"
21	AC/GND/DC Switch	"DC"

12. Verify trace is centered over major horizontal axis.

13. Connect Power Supply to SCOPE/DVM Connector (20) and apply +4 VDC. Verify trace moves up 4 divisions. Adjust R221 (GAIN CAL) on Scope Control PC Board, as required, for correct deflection.

14. Repeat Steps 12 and 13, as required, if adjustment was made.

15. Rotate VERTICAL Vernier Control (23) fully ccw and verify the trace shows approximately 0.4V.

16. Set Scope VERTICAL Attenuator Vernier Control (25) to "CAL" position.

17. Set AC/GND/DC Switch (21) to "AC" position and verify the trace returns to the center line.

18. Set AC/GND/DC Switch (21) to "GND" position and verify the trace does not move.

19. Disconnect the Power Supply and couple the TONE OUT Connector (17) to the SCOPE/DVM Connector (20) with a coax cable.

20. Set the FM/AM-1200A controls as follows:

CONTROL	SETTING
21 AC/GND/DC Switch	"DC"
26 HORIZONTAL Sweep Selector Control	"1 ms/DIV"

21. Connect Function Generator to SCOPE/DVM Connector (15). Set output to 1000 Hz. Adjust HORIZ POS Control to position first positive peak of signal on leftmost major vertical graticule. Verify each positive peak of the triangle waveform is positioned over each major vertical graticule. Adjust R247 (SWP CAL) on the Scope Control PC Board, if necessary.

22. Rotate the HORIZONTAL Sweep Selector Control (26) to each of the following positions and select the corresponding frequency on Function Generator. At each selection, verify the CRT (31) shows one cycle per division.

HORIZONTAL SELECTOR	FUNCTION GENERATOR FREQUENCY
a. 10 ms	100 Hz (±10%)
b. 1 ms	1,000 Hz (±10%)
c. 100 µs	10,000 Hz (±10%)
d. 10 ns	100,000 Hz (±10%)
e. 1 ns	1,000,000 Hz (±10%)

23. With the FM/AM-1200A set as in Step 22.c., rotate the HORIZONTAL Vernier Control (25) fully ccw and verify a miminum of 10 cycles per division on the CRT (31). Return the HORIZONTAL Vernier Control (25) to the "CAL" (fully cw) position.

STEP	PROCEDURE

24. Set the FM/AM-1200A Controls as follows:

	CONTROL	SETTING
39	MODE Selector Control	"GEN"
3	MODULATION Select Control	"FM NAR"
4	Modulation METER Control	"6 kHz/%X10"
5	VAR Tone Selector switch	"OFF"
7	1 kHz Tone Selector Switch	"INTL"
18	Keyboard	"RF 121.0000 MHz"
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"2 kHz/%X10"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"1 ms/DIV"

25. Adjust the 1 kHz Tone Level Control (8) for 4 kHz deviation on the MODULATION METER (1).

26. Verify the signal displayed on the CRT (31) is 2 divisions peak-to- peak. Adjust R201 (DEMOD CAL) on the Scope Control PC Board, as required, for correct display.

27. Disconnect test equipment.

4-2-12 DVM I/O BOARD CALIBRATION

PREREQUISITES:
- Meter Zero Calibration Procedure (4-2-1)
- Power Supply Calibration Procedure (4-2-2)
- Frequency Standard Calibration Procedure (4-2-3)
- Function Generator Calibration Procedure (4-2-4)
- High Loop Calibration Procedure (4-2-5)
- Digital Module Calibration Procedure (4-2-6)
- Modulation Meter Calibration (4-2-8, Steps 1 thru 11)
- Oscilloscope Calibration Procedure (4-2-10 or 4-2-11)

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)

- 1 Variable Power Supply (w/option 10 only)
- 1 Digital Voltmeter (w/option 10 only)
- 1 RF Signal Generator
- 1 BNC-to-BNC Coax Cable

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
22	PWR/OFF/BATT Switch	"PWR"
39	MODE Selector Control	"REC"
41	SQUELCH Control	Fully ccw
3	MODULATION SELECT Control	"FM MID"
4	Modulation METER Control	"6 kHz/%X10"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
18	Keyboard	"RF 121.0000 MHz" ENTER "2ND METER"
23	VERTICAL Vernier Control	"CAL"
24	VERTICAL Attenuator Selector Control	"2 kHz/%X10"
25	HORIZONTAL Vernier Control	"CAL"
26	HORIZONTAL Sweep Selector Control	"1 ms/Div"
35	FREQ ERROR METER Range Selector Control	"RF 10K"

CALIBRATION POINTS: See Figure 4-10

STEP	PROCEDURE

1. Set the following controls on the RF Signal Generator:

CONTROL	SETTING
MODULATION	10 kHz Deviation at 1 kHz Rate
AMPLITUDE	-50 dBm

STEP	PROCEDURE

2. Adjust R3033 (INPUT GAIN) until VFD (37) reading is 6.2 (±0.15). Record this level:

   _____.

3. Select "2ND METER" on Keyboard.

4. Adjust R3032 (VFD) until the MD Display on the VFD (37) is less than or equal to 0.05. Record this level (VFD OFFSET):

   _____.

5. Set the RF Signal Generator to 10 kHz deviation with a 1 kHz tone.

6. Reset the METER Range Selector (4) to 20 kHz/%X10.

7. Adjust R3039 (MOD METER CAL) until the VFD (37) reads "MD 10.00" (±0.60). Record this level:

   _____.

FE (Frequency Error) Meter Display

8. Connect a coax from the 10 MHz External Reference Connector (46) on the Rear Panel to the ANT Connector (34).

9. Set the following FM/AM-1200S/A controls:

CONTROL		SETTING
18	Keyboard	"RF 9.9900 MHz" "2ND METER"
39	MODE Selector Control	"REC"
35	FREQ ERROR Meter Range Selector Control	"10K"

10. Adjust R3035 (FREQ METER CAL) until FE display of VFD (37) reads 10.00 (±0.30). Record this level:

    _____.

STEP	PROCEDURE

DTMF Encode Test

11. Set the following controls on the FM/AM-1200S/A:

CONTROL		SETTING
3	MODULATION SELECT Control	"FM NAR"
4	Modulation Meter Control	"6 kHz/%X10"
18	Keyboard	"DTMF"
39	MODE Selector Control	"GEN"

12. While holding down the "5" key on the Keyboard, adjust R3260 (DTMF LEVEL ADJ) on the Generate Audio PC Board until the MODULATION METER (1) indicates 3.5 kHz deviation.

13. Set the controls of a second FM/AM-1200S/A, with Option 10 installed, for DTMF as follows:

CONTROL		SETTING
3	MODULATION SELECT Control	"FM NAR"
39	MODE Selector Control	"REC"
18	Keyboard	"RF 121.0000 MHz" "DTMF - ENTER"

14. Connect a coax from the T/R Connector (11) of the FM/AM-1200S/A under test to the ANT Connector (34) of the DTMF FM/AM-1200S/A.

15. Reset the controls of the FM/AM-1200S/A test set as follows:

CONTROL		SETTING
18	Keyboard	"RF 121.0000 MHz"
39	MODE Selector	"GEN"
3	MODULATION Select Control	"FM NAR"
5	VAR Tone Selector Switch	"OFF"
7	1 kHz Tone Selector Switch	"OFF"
18	Keyboard	PROG - DTMF - 1 - 1 - 2 - 3 - 4 - 5 - 6 - 7 - 8 - 9 - 0 - 2nd A - 2nd B - 2nd C - 2nd D - 2nd # - 2nd * - EXEC - ENTER

16. Verify the DTMF numbers entered from the test set appear in the VFD (37) of the DTMF Receiver. Record this Display:

— — — — — — — — — — — — — — — — —

STEP PROCEDURE

DTMF Decode Test (With Option 10 Only)

17. Reset the controls of the FM/AM-1200S/A test set as follows:

CONTROL		SETTING
39	MODE Selector	"REC"
18	Keyboard	"DTMF - ENTER"

18. Reset the controls of the FM/AM-1200S/A for DTMF as follows:

CONTROL		SETTING
39	MODE Selector	"GEN"
18	Keyboard	PROG - DTMF - 1 - 1 - 2 - 3 - 4 - 5 - 6 - 7 - 8 - 9 - 0 - 2nd A - 2nd B - 2nd C - 2nd D - 2nd # - 2nd * - EXEC - ENTER

19. Verify the DTMF numbers entered from the DTMF Receiver appear in the VFD (37) of the Test Set. Record this Display (if in error):

__ __ __ __ __ __ __ __ __ __ __ __ __ __ __ __ __

DCS Test

20. Set the controls of the second FM/AM-1200S/A for DCS as follows:

CONTROL		SETTING
3	MODULATION Select Control	"FM NAR"
39	MODE Selector	"REC"
5	VAR Tone Selector Switch	"VAR"
6	VAR Tone Level Control	"OFF"
18	Keyboard	2ND - DCS - ENTER

21. Reset the controls of the FM/AM-1200S/A test set as follows:

CONTROL		SETTING
39	MODE Selector	"GEN"
3	MODULATION Select Control	"FM NAR"
5	VAR Tone Selector Switch	"VAR"
6	VAR Tone Level Control	"1.5" (on MODULATION METER)
18	Keyboard Sequence	PROG - DCS - 0 - 2 - 3 - EXEC - DCS - ENTER

STEP	PROCEDURE

22. Verify the DCS numbers entered from the test set appear in the VFD (37) of the DCS Receiver. Record this Display:

    __ __ ___

23. Reset the following controls on the FM/AM-1200S/A test set:

CONTROL	SETTING
39 MODE Selector	"REC"
18 Keyboard	2ND - DCS - ENTER

24. Reset the following controls on the DCS FM/AM-1200S/A set:

CONTROL	SETTING
39 MODE Selector	"GEN"
18 Keyboard	PROG - DCS - 0 - 2 - 3 - EXEC - DCS - ENTER

25. Verify the DCS numbers entered from the DCS set appear in the VFD (37) of the Test Set. Record this Display:

    __ __ ___

DVM Test (Option 10 Only)

26. Press the following Keyboard sequence on the FM/AM-1200S/A:

    "2ND FUNCT" - "DVM" - "+/-" (i.e., DC)

27. Adjust trimpot R3016 (ZERO ADJ) to +12 VDC on the VFD (37). Alternate the "POS/NEG" Switch on TF-30 until the voltage reading is the same, positive and negative value, on the VFD (37). Record the voltage(s):

    VFD: +_____, -_____

28. Set Digital Voltmeter to VDC at 2V range.

29. Use Tee Connector to connect Variable Power Supply set to 0 µV and Digital Voltmeter to Scope/DVM Connector (20).

30. Adjust DC Power Supply to 1.20 VDC as displayed on Digital Voltmeter. Adjust R3020 (DC CAL) for reading on DVM I/O PC Board the same as displayed on external Power Supply. Record this level:

    VDC on DVM I/O: _____

31. Adjust the DC power supply voltage to 13.3 VDC, to 1.33 VDC and below 0.99 VDC several times. Verify the transition above and below the autorange switching points are smooth. Record these levels:

    Autorange (13.3 VDC): _____
    Autorange (1.33 VDC): _____
    Autorange (low): _____

32. Set variable power supply to 5 VDC as displayed on Digital Voltmeter. Verify DVM reading on FM/AM-1200S/A is the same as that of the external Digital Voltmeter (±10%).

33. Reset the external Digital Voltmeter to 20 VDC and repeat Step 32.

34. Reset the Digital Voltmeter to VAC at 2V Range.

35. Reset the controls on the FM/AM-1200S/A as follows:

	CONTROL	SETTING
7	1 kHz Tone Selector Switch	"INTL"
5	VAR Tone Selector Switch	"OFF"
18	Keyboard	"+/-"

36. Adjust 1 kHz tone level on FM/AM-1200S/A until Digital Voltmeter reads 2.0 VAC. Adjust R3008 (AC CAL) on DVM I/O PC Board until DVM display on FM/AM-1200S/A is the same as the reading on the external Digital Voltmeter. Record this level:

    R3008 (VAC): _____

Check Variable Tone

37. Set the following controls on the FM/AM-1200S/A:

	CONTROL	SETTING
5	VAR Tone Selector Switch	"INTL"
7	1 kHz Tone Selector Switch	"OFF"
18	Keyboard	"2nd METER"
		"45 Hz SINE"

38. Connect external Digital Voltmeter to TONE OUT Connector (17).

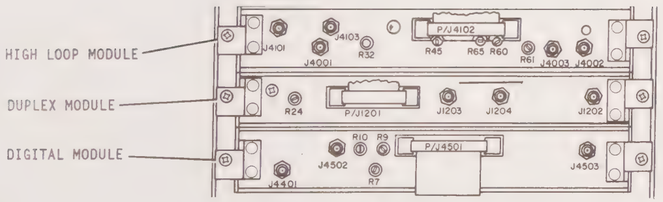
39. Adjust VAR TONE LVL to 1.94 VRMS (±10%) on external Digital Voltmeter.

40. Connect TONE OUT Connector (17) to SCOPE/DVM Connector (20).

STEP	PROCEDURE
41.	Verify VFD reading is the same as that of Digital Voltmeter (±10%).
42.	Disconnect all equipment.

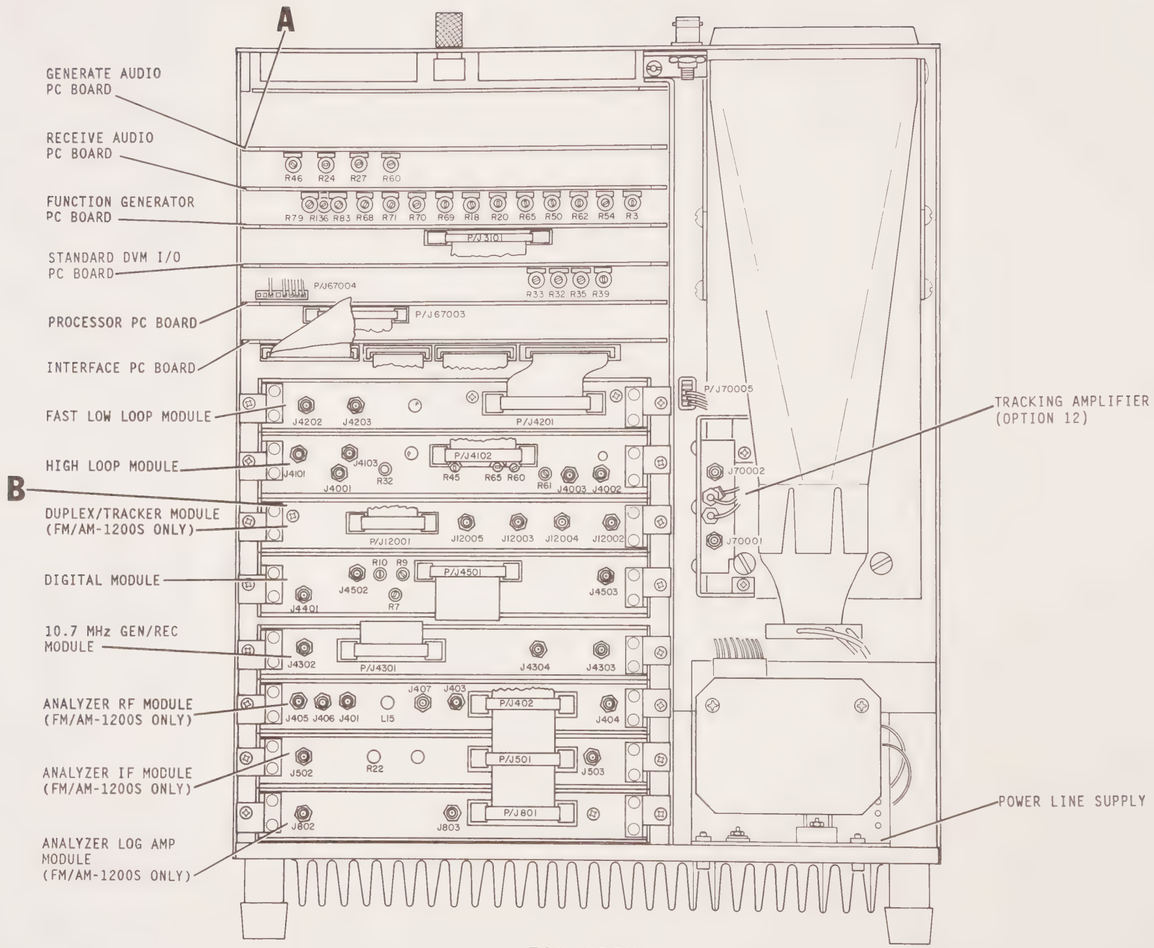
DETAIL **A**

GENERATE AUDIO PC BOARD
W/OPTION 10

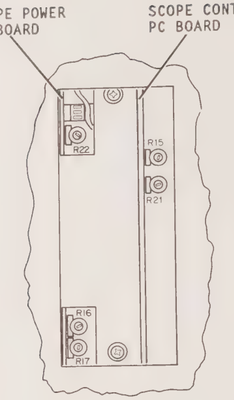


DETAIL **B**

FM/AM-1200A W/DUPLEX MODULE

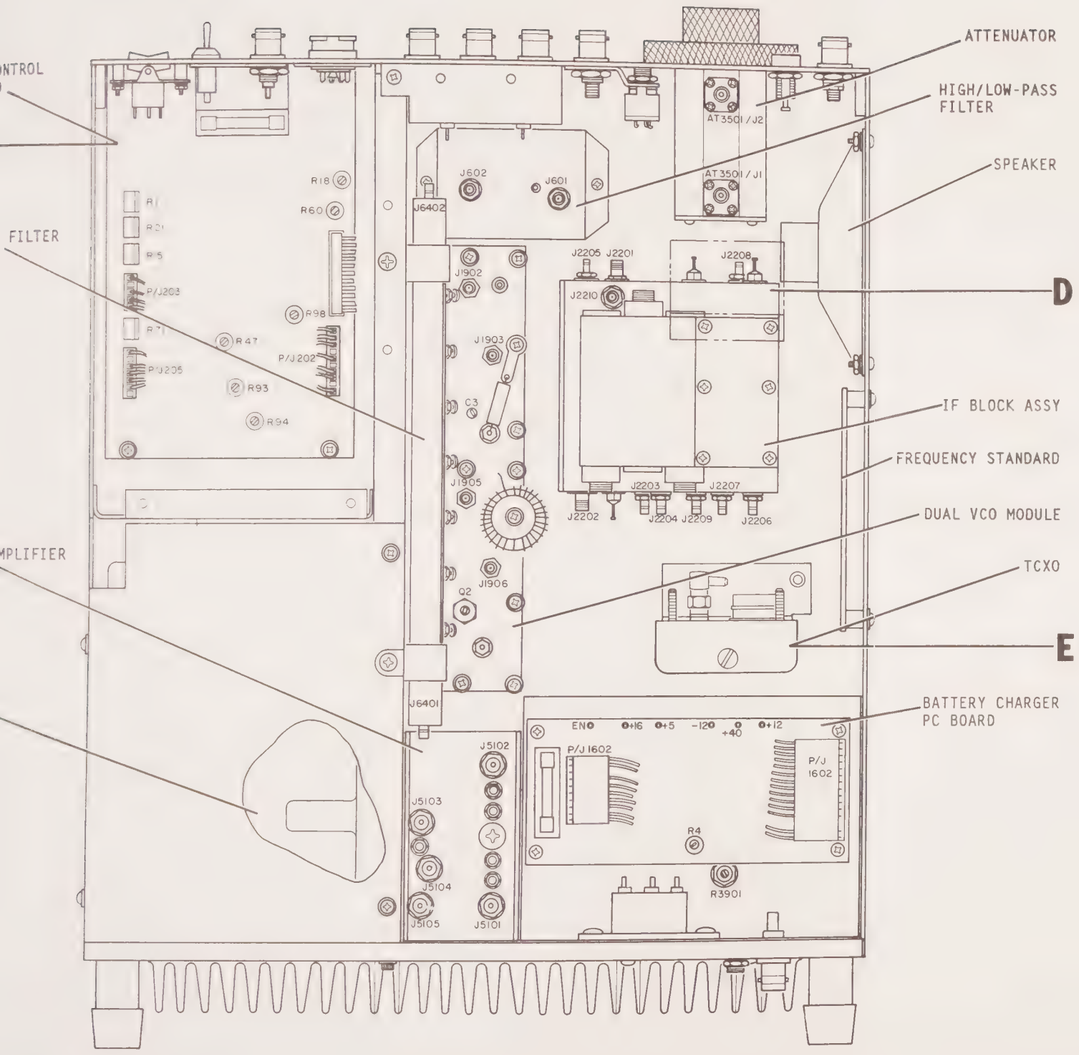


TOP VIEW

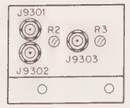


DETAIL **C**

SIDE VIEW: SCOPE POWER
AND CONTROL PC BOARDS
(FM/AM-1200A)

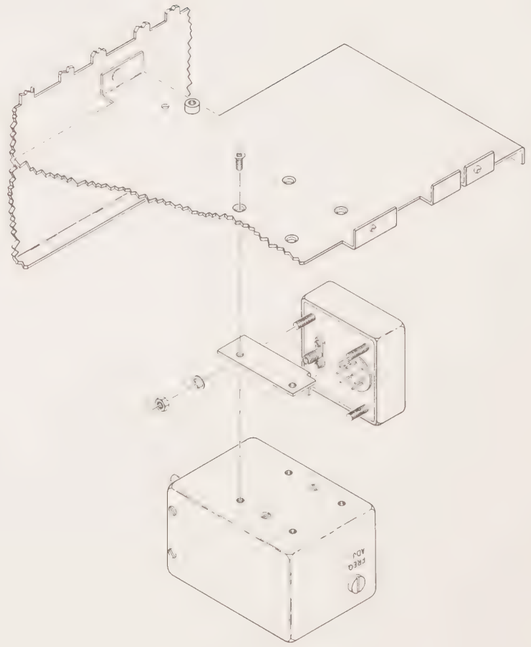


BOTTOM VIEW



DETAIL **D**

MIXER NULL ASSY



DETAIL **E**

OPTION 03:OVEN OSCILLATOR

Figure 4-10 Location of Calibration Adjustments and Test Points

SECTION 5 - PREVENTIVE MAINTENANCE

5-1 GENERAL

Preventive maintenance on FM/AM-1200S/A test sets consists primarily of cleaning and visual inspection of internal/external components. External cleaning of the test set is recommended as often as necessary, depending on the environmental conditions to which the set is exposed. Internal cleaning should be performed on a more limited basis, prefreably when the set is in a disassembled state for routine calibration, troubleshooting and/or repair. Test set disassembly for the sole purpose of internal cleaning is not recommended.

5-1-1 EXTERNAL CLEANING

A. Clean front panel and case with a soft lint-free cloth moistened with rubbing alcohol.

B. To remove tar or oil from outside case, safety solvent may be used.

CAUTION: DO NOT ALLOW SAFETY SOLVENT TO CONTACT FRONT PANEL CONTROL AREA. SOLVENT CAN CAUSE DAMAGE TO FRONT PANEL CONTROLS, MARKINGS ETC.

5-1-2 INTERNAL CLEANING AND INSPECTION

NOTE: The following procedures require external case to be removed from test set.

CAUTION: DELIBERATE MOVING (HOWEVER SLIGHT) OF DISCRETE COMPONENTS ON CIRCUIT BOARDS, ETC. SHOULD BE AVOIDED.

DO NOT CLEAN INTERNAL MODULES FOR SOLE PURPOSE OF CLEANING.

A. Remove dust with hand-controlled dry air jet of 15 psi (1.054 kg/cm^2) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.

A. (Continued)

WARNING: DO NOT USE COMPRESSED AIR IN EXCESS OF 15 PSI. USE EXTREME CARE WHEN USING COMPRESSED AIR IN THE VICINITY OF CRT, IN ORDER TO MINIMIZE POSSIBILITY OF CRT IMPLOSION. OBSERVE FOLLOWING PRECAUTIONS:

1. REMOVE ANY LARGE DIRT/DUST PARTICLES FROM CRT MANUALLY, AS OPPOSED TO USING COMPRESSED AIR.

2. DO NOT USE COMPRESSED AIR IN A DIRTY CLUTTERED ENVIRONMENT. REMOVE ANY DEBRIS OR SMALL OBJECTS IN THE IMMEDIATE WORK AREA THAT MAY BECOME AIRBORNE DUE TO PRESSURIZED AIRFLOW.

3. IF POSSIBLE, USE AN AIR HOSE NOZZLE EQUIPPED WITH A SPRING LOADED ON/OFF VALVE, AS OPPOSED TO ONE THAT REMAINS OPEN OR CLOSED CONTINUOUSLY.

4. MAKE SURE COMPRESSED AIR HOSE IS FILTERED, TO PREVENT POSSIBLE OIL OR WATER DROPLETS FROM STRIKING CRT AT HIGH SPEEDS.

B. Inspect CHASSIS for:

1. Tightness of subassemblies and chassis mounted connectors.

2. Corrosion or damage to metal surfaces.

C. Inspect CAPACITORS for:

1. Loose mounting, deformities or obvious physical damage.

2. Leakage or corrosion around leads.

D. Inspect CONNECTORS for:

1. Loose or broken parts, cracked insulation and bad contacts.
DO NOT disassemble connectors needlessly within test set.

E. Inspect POTENTIOMETER CONTROLS for:

1. Free rotation. If rotation feels rough, check control with
an ohmmeter.

F. Inspect readily accessible PRINTED CIRCUIT BOARDS for:

1. Corrosion or damage to connectors.

G. Inspect RESISTORS for:

1. Cracked, broken, charred or blistered bodies.

2. Loose or corroded solder connections.

H. Inspect SEMICONDUCTORS for:

1. Cracked, broken, charred or discolored bodies.

2. Seals around leads being in place and in good condition.

I. Inspect TOGGLE SWITCHES for:

1. Loose levers or terminals and switch body contact to frame.

2. Bent or loose line switch contacts.

J. Inspect TRANSFORMER for:

1. Signs of excessive heating.

2. Broken or charred insulation and loose mounting hardware.

K. Inspect WIRING for:

1. Broken or loose ends and connections.

2. Proper dress relative to other chassis parts.

NOTE: All laced wiring should be tight with ends securely tied.

SECTION 6 - MECHANICAL ASSEMBLIES, PC BOARDS & SCHEMATICS

6-1 GENERAL

This section contains component layout drawings for all PC Board assemblies, interconnect diagrams, circuit schematics, waveforms and charts reflecting voltage levels keyed to test points. These drawings are sequenced in the general order they are discussed in Section 2 (Theory of Operation). An alphabetical index of all drawings for each module is contained in Paragraph 6-3.

6-2 HOW TO USE SCHEMATICS

To trace coaxial cable conductors from one schematic to another, follow the procedures outlined in Paragraph 6-2-1. To trace conductors for multiple pin connectors, refer to Paragraph 6-2-2.

6-2-1 COAXIAL CABLES

A. Locate desired module on Coaxial Cable Interconnect Drawing.

B. Locate desired coaxial cable on Interconnect Drawing. (Connectors are identified by reference designators.)

C. Follow coaxial cable on Interconnect Drawing to locate opposite end of conductor. Note cable reference designator and module of cable's destination.

D. Locate schematic of desired module on Index of Circuit Schematics in Paragraph 6-3.

E. Locate reference designator of coaxial connector and continue tracing circuit.

6-2-2 MULTIPLE PIN CONNECTORS

A. Locate desired module on Interconnect drawing.

B. Locate desired multiple pin connector on Interconnect Drawing. Note reference designator of the mating connector.

C. Note module or wire harness on which the connector is mounted or grouped.

D. Locate schematic of desired module on Index of Circuit Schematics in Paragraph 6-3.

E. Using module schematic, locate reference designator of multiple pin connector and continue tracing circuit.

6-3 ALPHABETICAL INDEX OF FM/AM-1200S/A DRAWINGS

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10.7 MHz GEN REC PC Board Assembly (FM/AM-1200A)	6-28
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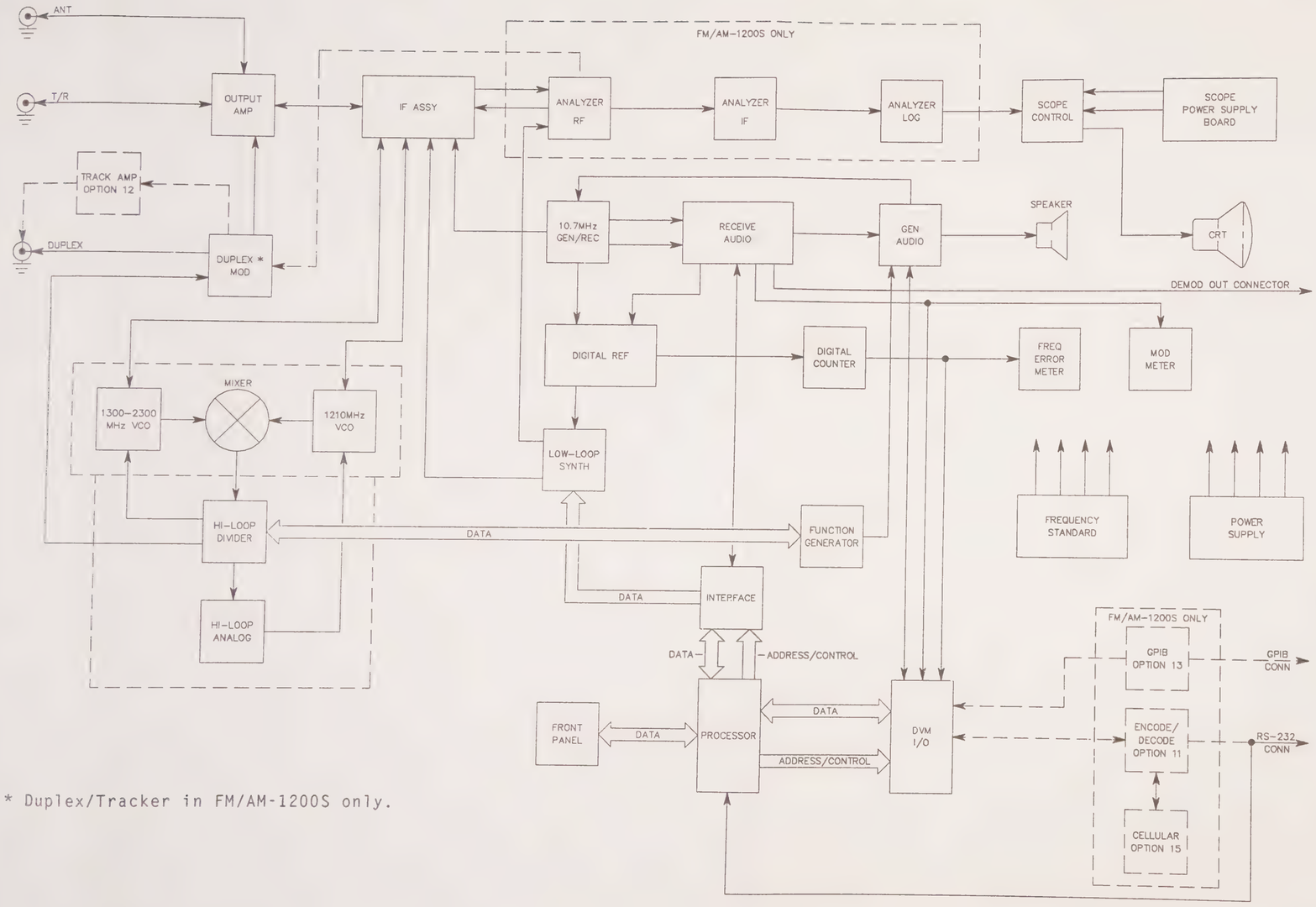


* Duplex/Tracker in FM/AM-1200S only.

	SIGNAL SOURCE			SIGNAL DESTINATION		
	COAX NO.	CONNECTOR NO.	MODULE	CONNECTOR NO.	MODULE	
2	1	J4202	LOW LOOP	J2203	IF BLOCK	+5
1	2	J4203	LOW LOOP	J403	ANALYZER RF	-20
	3	J602	HI/LOW FILTER	J4101	HIGH LOOP	-28
	4	E2807	FREQ STANDARD	J4001	HIGH LOOP	4
	5	J4103	HIGH LOOP	J1202	DUPLEX	-20
1	5	J4103	HIGH LOOP	J12002	DUPLEX/TRACKER	0 T
	6	J4003	HIGH LOOP	J1906	DUAL VCO (1ST LO)	D.C
	7	J4002	HIGH LOOP	J1903	DUAL VCO (2ND LO)	D.C
6	8	J1203	DUPLEX	J3513	DUPLEX CONNECTOR	
1	9	J1204	DUPLEX	J5105	OUTPUT AMPLIFIER	
	8	J70002	TRACKER AMP	J3512	DUPLEX CONNECTOR	
	9	J12004	DUPLEX/TRACKER	J5105	OUTPUT AMPLIFIER	
	10	J4303	10.7 MHz GEN/REC	J4401	DIGITAL	120
	11	J4304	10.7 MHz GEN/REC	J4502	DIGITAL	2.2
	12	E2806	FREQ STANDARD	J58002	FAST LOW LOOP	4.0
	13	J2202	IF BLOCK	J4302	10.7 MHz GEN/REC	INP
3 1	14	J405	ANALYZER RF	J2208	IF BLOCK	INP
1	15	E2809	FREQ STANDARD	J404	ANALYZER RF	1.5
1	16	J401	ANALYZER RF	J502	ANALYZER IF	0 T
1	17	J503	ANALYZER IF	J802	ANALYZER LOG AMP	30
	18	J3512	ANT CONNECTOR	J2201	IF BLOCK	INP
	19	J2202	IF BLOCK	J1501	OUTPUT AMPLIFIER	INP
	20	J5103	OUTPUT AMPLIFIER	AT3501-J1	ATTENUATOR	
	21	AT3501-J2	ATTENUATOR	J5102	OUTPUT AMPLIFIER	
7	22	J3514	T/R CONNECTOR	J5104	OUTPUT AMPLIFIER	
1	23	J2209	IF BLOCK	J406	ANALYZER RF	INP
	24	J6402	LOW PASS FILTER	J601	HI/LOW FILTER	-25
	25	J1907	DUAL VCO	J6401	LOW PASS FILTER	-22
	26	J1905	DUAL VCO	J9301	MIXER NULL	+5
	27	J1902	DUAL VCO	J2207	IF BLOCK	+5
	28	E2805	FREQ STANDARD	J4603	EXT REF CONNECTOR	13
	29	J3602	OPT OVEN OSC	E2808	FREQ STANDARD	1.5
	30	J9302	MIXER NULL	J2205	IF BLOCK	+5
	31	J9303	MIXER NULL	J2210	IF BLOCK	
1	32	J407	ANALYZER RF	J12005	DUPLEX/TRACKER	
8	32	J2208	IF BLOCK	J2209	IF BLOCK	INP
6	33	J12003	DUPLEX/TRACKER	J70001	TRACKER AMP	
	34	J58005	FAST LOW LOOP	J4503	DIGITAL	4.0

RECEIVE MODE		GENERATE MODE		DUPLEX MODE	
EVEL	FREQ/SIGNAL	LEVEL	FREQ/SIGNAL	LEVEL	FREQ/SIGNAL
+12 dBm	77.3-79.3 MHz	+5 TO +12 dBm	77.3-79.3 MHz	+5 TO +12 dBm	77.3-79.3 MHz
) -40 dBm	77-3.79.3 MHz	-20 TO -40 dBm	77.3-79.3 MHz	-20 TO -40 dBm	77.3-79.3 MHz
) -34 dBm	90-1088 MHz	-28 TO -34 dBm	90-1088 MHz	-28 TO -34 dBm	90-1088 MHz
) (±0.5V)	90-1088 MHz	4 Vp-p (±0.5V)	500 kHz	4 Vp-p (± 0.5V)	500 kHz
) -30 dBm	500 kHz	-20 TO -30 dBm	90-1088 MHz	-20 TO -30 dBm	90-1088 MHz
-5 dBm	90-1088 MHz	0 TO +5 dBm	90-1088 MHz	0 TO +15 dBm	90-1088 MHz
	90-1088 MHz	DC	0-35 VDC	0-35 VDC	DC
	0-35 VDC	DC	0 VDC	0 VDC	DC
	0 VDC			-60 dBm	OFFSET GEN FREQ
				-30 dBm	OFFSET GEN FREQ
				-6 TO -50 dBm	OFFSET GEN FREQ
				-35 dBm	OFFSET GEN FREQ
Vp-p (±10 mV)	10.7 MHz	120 mVp-p (±10 mV)	10.7 MHz	120 mVp-p (±10 mV)	10.7 MHz
p-p (±0.2 mV)	21.4 MHz	2.2 Vp-p (±0.2V)	21.4 MHz	2.2 Vp-p (±0.2V)	21.4 MHz
p-p (±0.5V)	1 MHz	4.0 Vp-p (±0.5V)	1 MHz	4.0 Vp-p (±0.5V)	1 MHz
±2 dBm	10.7 MHz	-15 TO -20 dBm	10.7 MHz	INPUT ±2 dBm	10.7 MHz
	83-95 MHz	-28 TO -32 dBm	88-90 MHz	INPUT	83-95 MHz
p-p (±0.2V)	1 MHz	1.5 Vp-p (±0.2V)	1 MHz	1.5 Vp-p (±0.2V)	1 MHz
5 dBc	22.3 MHz	-45 TO -60 dBc	22.3 MHz	0 TO 5 dBc	22.3 MHz
C	1.2 MHz	30 dBc	1.2 MHz	30 dBc	1.2 MHz
	RF			INPUT	RF
-80 dB	RF	-20 dBm (±5 dB)	RF		
		W/FINE ATTN CCW 0 dBm (±1 dB)	RF		
		20 dB ABOVE SELECTED LEVEL	RF		
		-20 TO -127 dBm	RF	-85 dBm/-80 dBm	RF
	83-95 MHz	-28 TO -32 dBm	83-95 MHz	INPUT	83-95 MHz
) -30 dBm	90-1088 MHz	-25 TO -30 dBm	90-1088 MHz	-25 TO -3 dBm	90-1088 MHz
) -28 dBm	90-1088 MHz	-22 TO -28 dBm	90-1088 MHz	-22 TO -28 dBm	90-1088 MHz
+12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz
+12 dBm	1210 MHz	+5 TO +12 dBm	1210 MHz	+5 TO +12 dBm	1210 MHz
Vp-p (±10 mV)	10 MHz	130 mVp-p (±10 mV)	10 MHz	130 mVp-p (±10 mV)	10 MHz
p-p (±0.2V)	10 MHz	1.5 Vp-p (±0.2V)	10 MHz	1.5 Vp-p (±0.2V)	10 MHz
+12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz
	1300-2298 MHz		1300-2298 MHz		
				-10 dBm	OFFSET GEN FREQ
	83-95 MHz	-28 TO -32 dBm	88-90 MHz	INPUT	83-95 MHz
				-15 TO -50 dBm	OFFSET GEN FREQ
p-p (±0.5V)	1 MHz	4.0 Vp-p (±0.5V)	1 MHz	4.0 Vp-p (±0.5V)	1 MHz

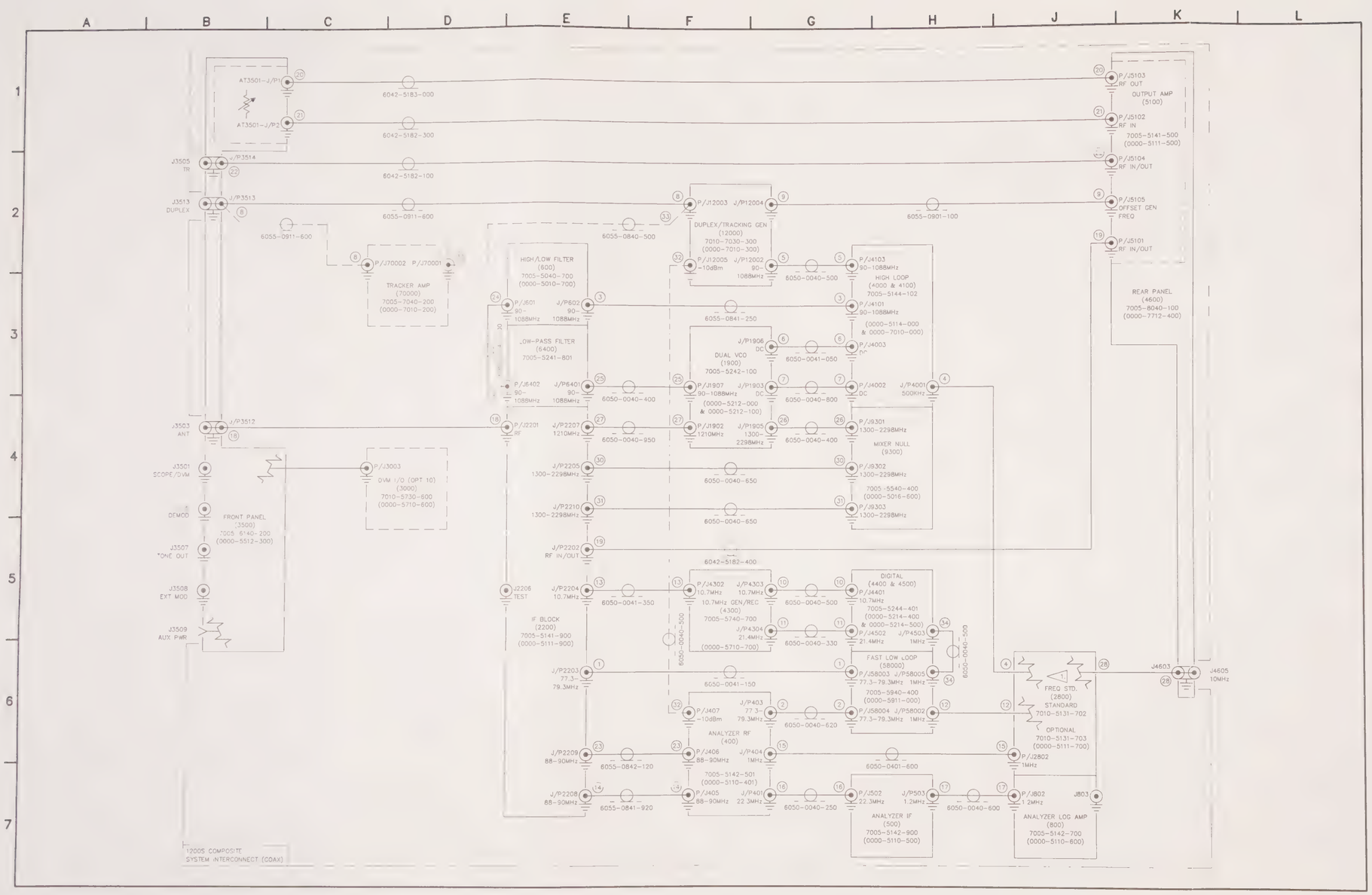
NOTES:

1. FM/AM-1200S ONLY.
2. REFER TO FIGURES 6-2 AND 6-4 TO LOCATE COAX NUMBERS.
3. FM/AM-1200S: SIGNAL SOURCE IS J2209 ON IF BLOCK ASSY.

4. AND 5. N/A.

6. FM/AM-1200S ONLY W/OPTION 12 (TRACKING GENERATOR) INSTALLED.
7. FM/AM-1200S: DUPLEX MODE OUTPUT IS -85 dBm (±10 dB).
8. FM/AM-1200A ONLY.

Figure 6-1 FM/AM-1200S/A System Block Diagram with System Flow Data



NOTES:

1. FREQUENCY STANDARD:
   OPTION 1: .2 PPM TCXO (P/N: 7010-5131-702)
   OPTION 2: .05 PPM OVEN OSCILLATOR (P/N: 7010-5131-703).

2. WHEN GPIB/RS-232C INTERFACE (OPTION 13) IS INSTALLED, USE THE FOLLOWING CABLES: 1) FROM/TO FRONT PANEL: 6045-5780-000; 2) FROM/TO PROCESSOR: 7007-5780-100.

3. WHEN ENCODE/DECODE (OPTION 11) OR CELLULAR (OPTION 15) IS INSTALLED, USE CABLE: 7007-7780-000.

4. ENCODE/DECODE (OPTION 11) USES ONLY 7010-7730-000; CELLULAR ASS'Y (OPTION 15) USES 7005-7740-100, WHICH CONTAINS: ENCODE/DECODE: (7010-7730-000) AND CELLULAR OPTIONS (7010-7730-100).

5. THRU SER NO 8300, PROCESSOR (7010-5730-900) WAS 7010-5730-200.

Figure 6-2 Coaxial Cable Interconnect Diagram (FM/AM-1200S) (0000-6111-800-H)

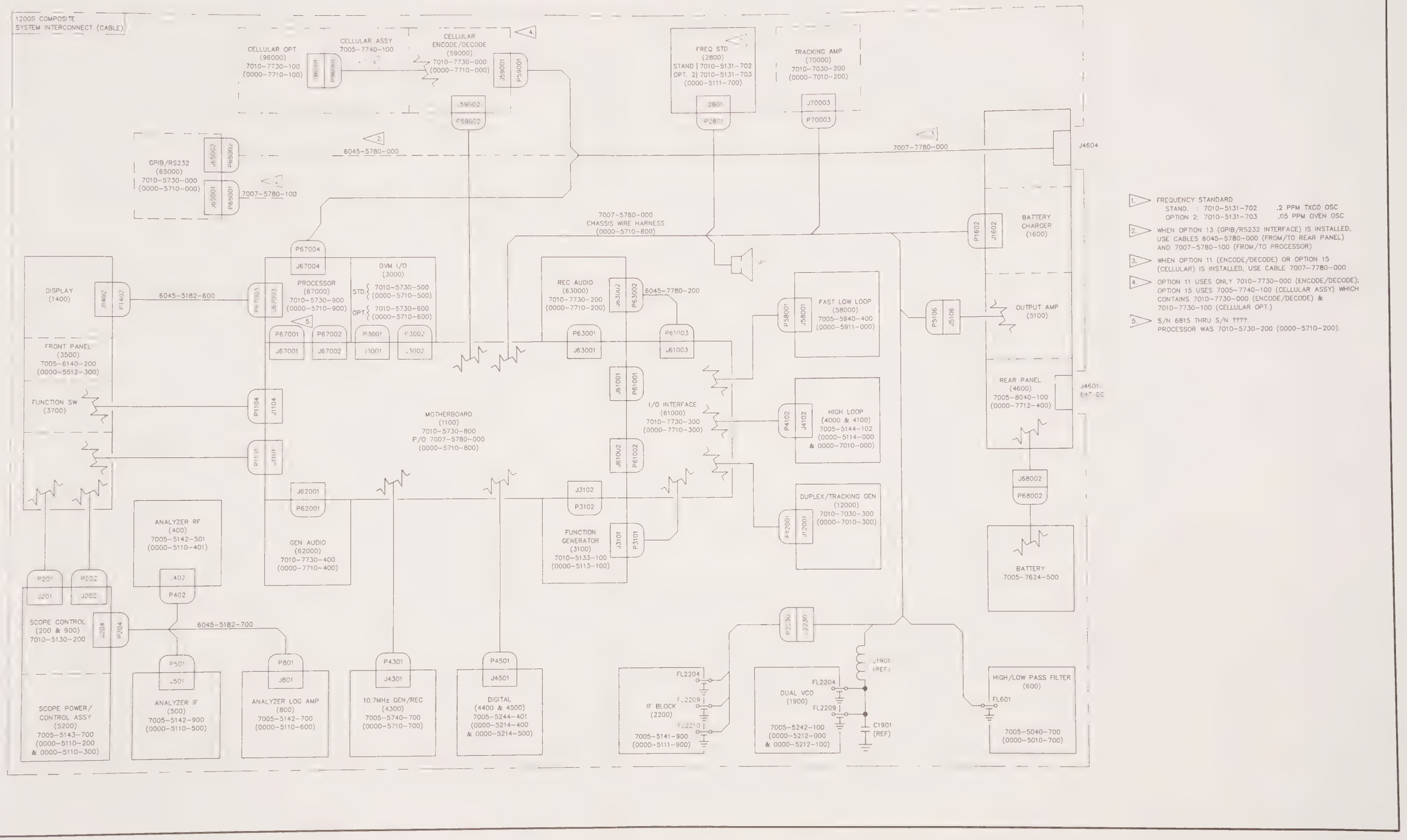
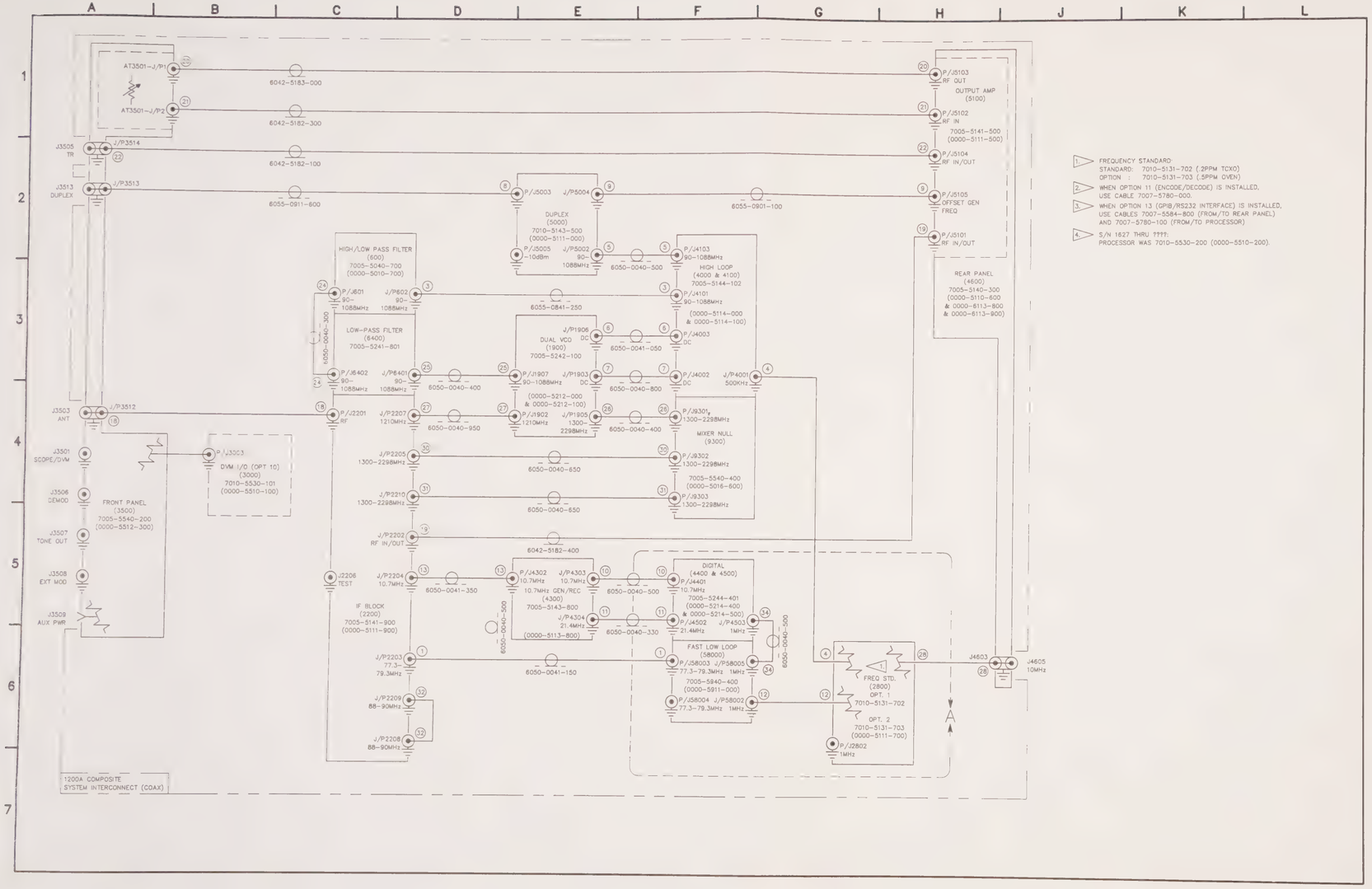


Figure 6-3 Ribbon Cable Interconnect Diagram (FM/AM-1200S) (0000-6111-800-H)



NOTES:

1. FREQUENCY STANDARD:
   STANDARD: .2 PPM TCXO (P/N: 7010-5131-702)
   OPTION: .05 PPM OVEN OSCILLATOR (P/N: 7010-5131-0703).
2. WHEN ENCODE/DECODE (OPTION 11) IS INSTALLED, USE CABLE NO.: 7007-5730-000.
3. WHEN GPIB/RS-232C INTERFACE (OPTION 13) IS INSTALLED, USE THE FOLLOWING CABLES: 1) FROM/TO REAR PANEL: 7007-5584-800; 2) FROM/TO PROCESSOR: 7007-5780-000.
4. THRU SER NO. 1706: PROCESSOR (7010-5730-900) WAS 7010-5530-200.

Figure 6-4 Coaxial Cable Interconnect Diagram (FM/AM-1200A)
(0000-5511-800-E1)

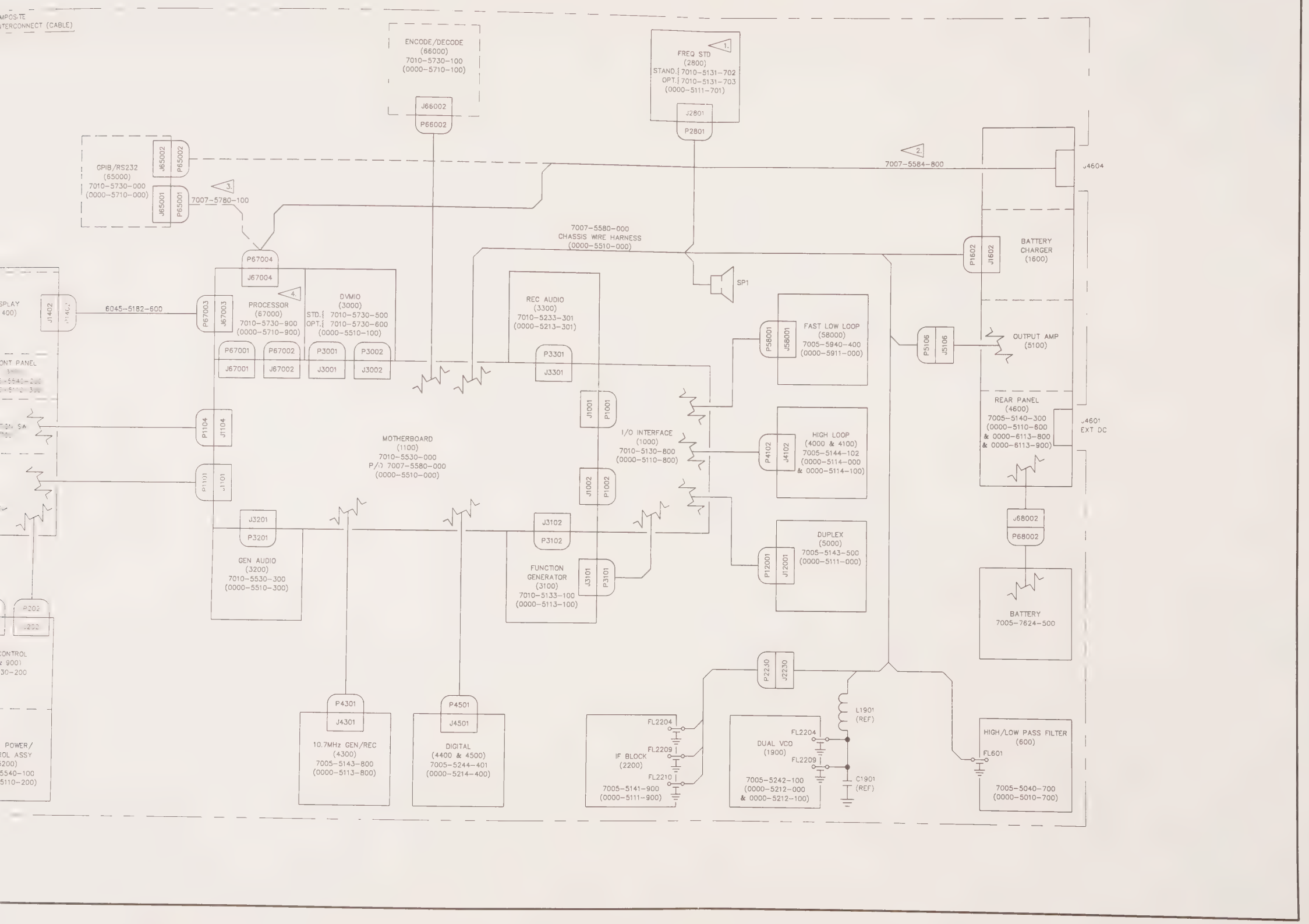
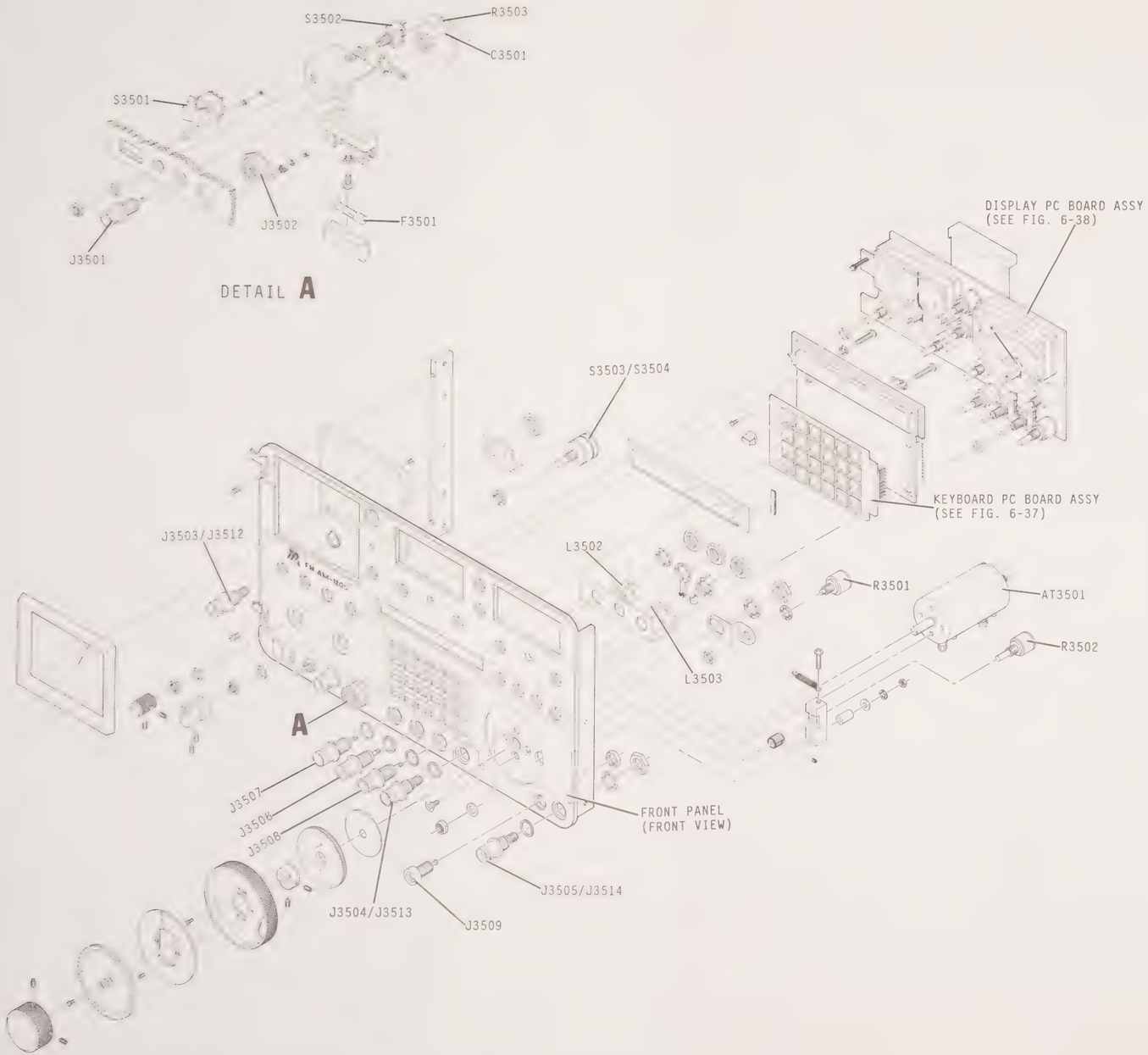
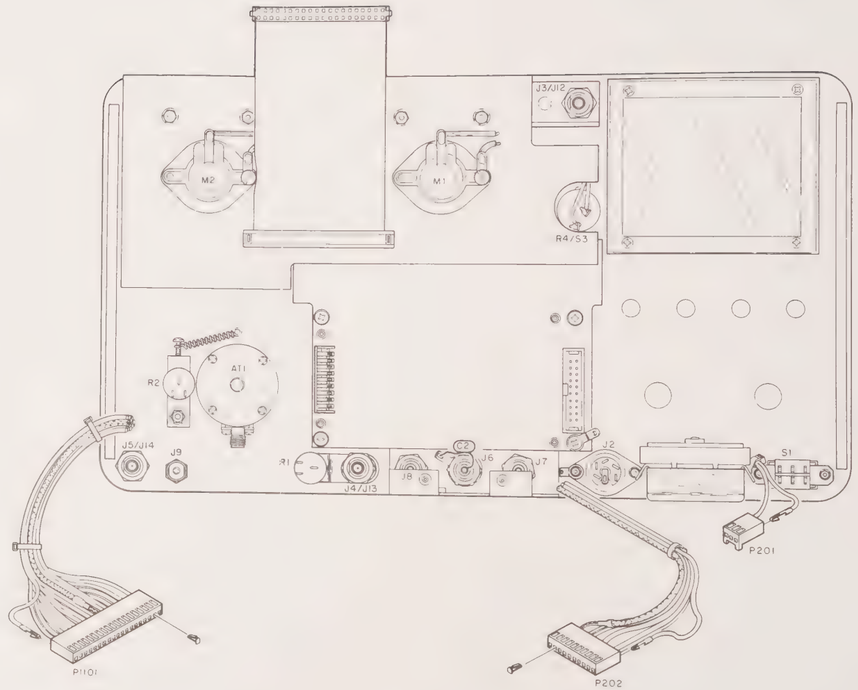


Figure 6-5 Ribbon Cable Interconnect Diagram (FM/AM-1200A) (0000-5511-800-E1)



FRONT PANEL ASSY (7005-5540-200-C)



FRONT PANEL (REAR VIEW)

A

1

2

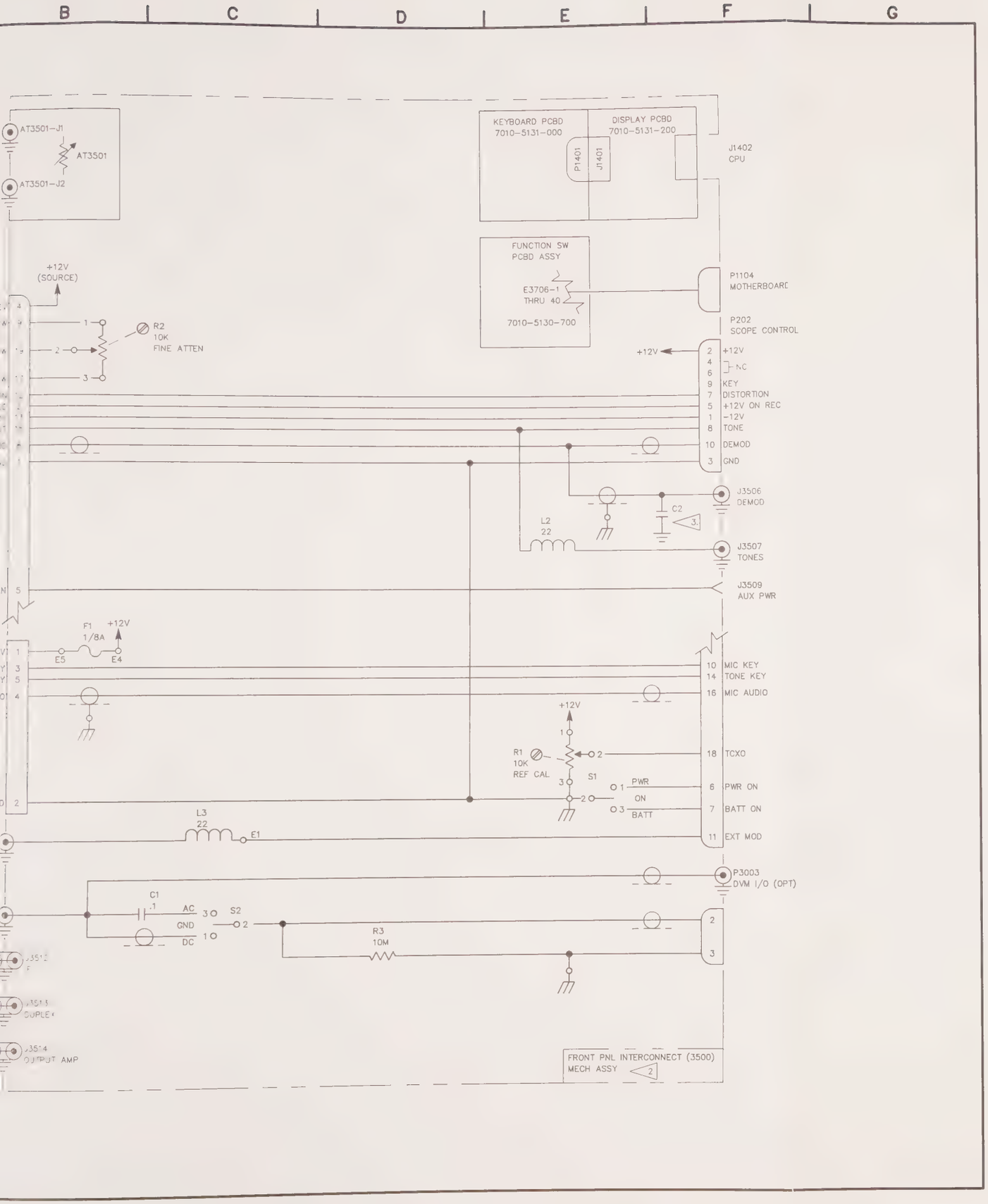
3

4

5

6

7



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3500 (I.E., R1 IS R3501).

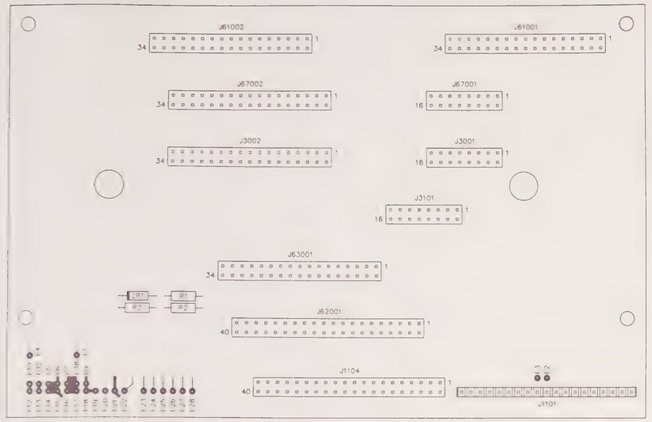
2. FM/AM-1200S: MECH ASS'Y IS 7005-6140-200.
   FM/AM-1200A: MECH ASS'Y IS 7005-5540-200.

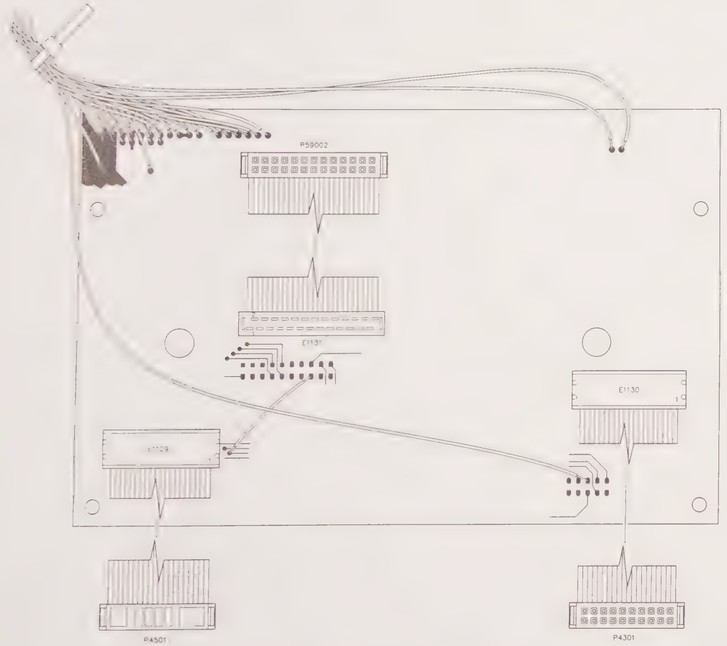
3. FM/AM-1200S: C3502 IS 5600 pF, 100V.
   FM/AM-1200A: C3502 IS 100 pF, 100V.

4. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

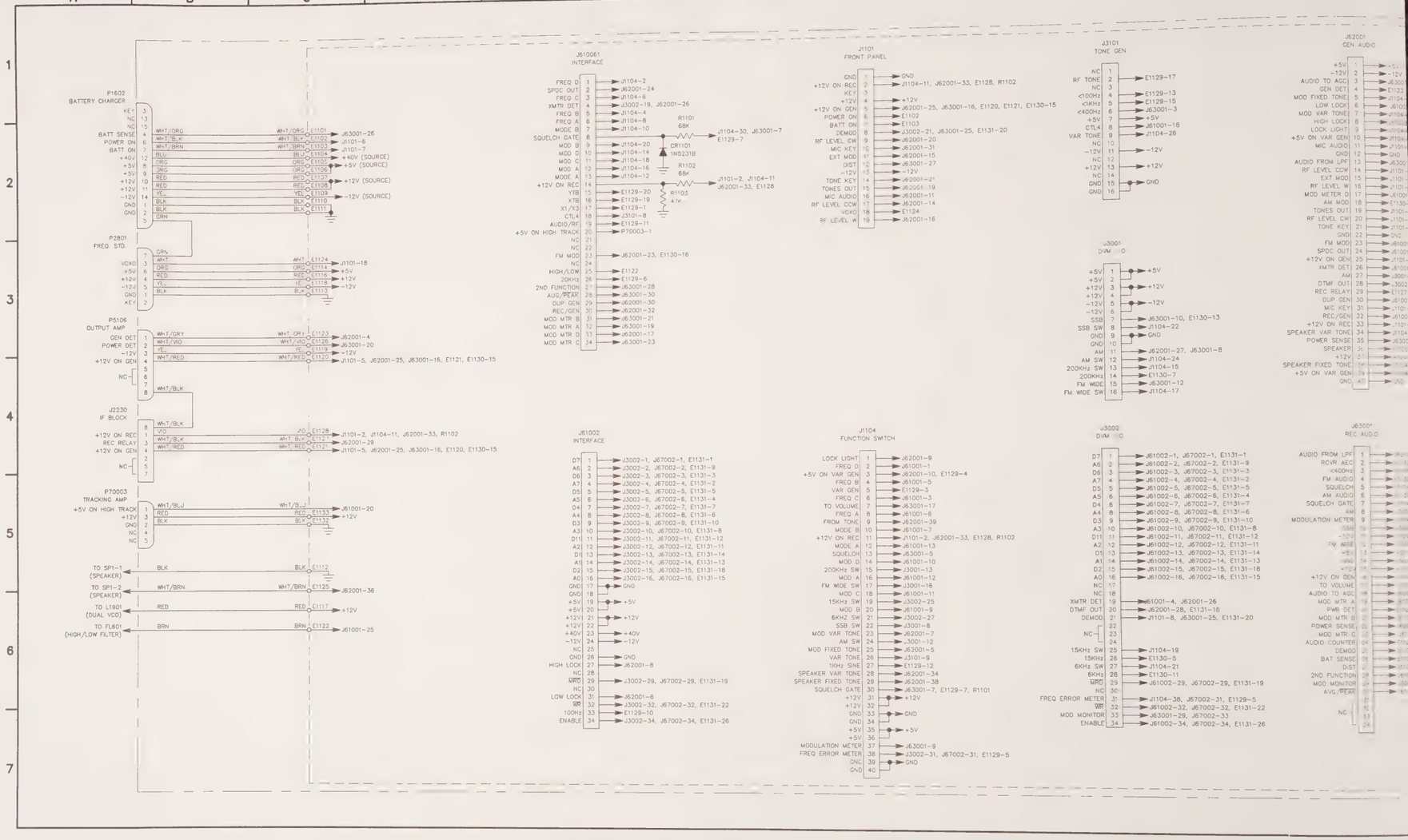
5. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

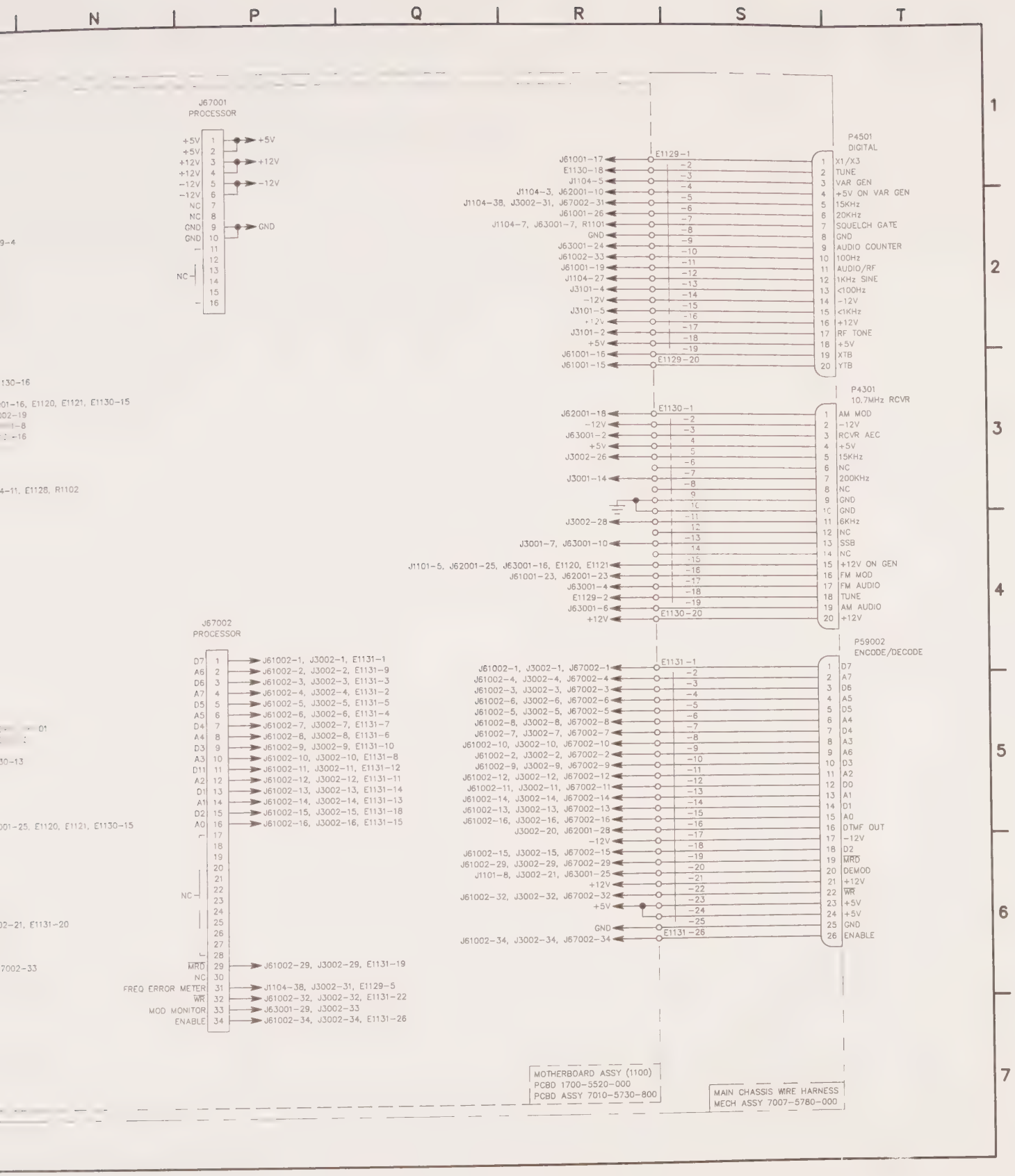
Figure 6-6 Front Panel Assembly/Interconnect Diagram (0000-5512-300-E1)





MOTHERBOARD/WIRE HARNESS ASSY (FM/AM-1200S)
(7007-5780-000)





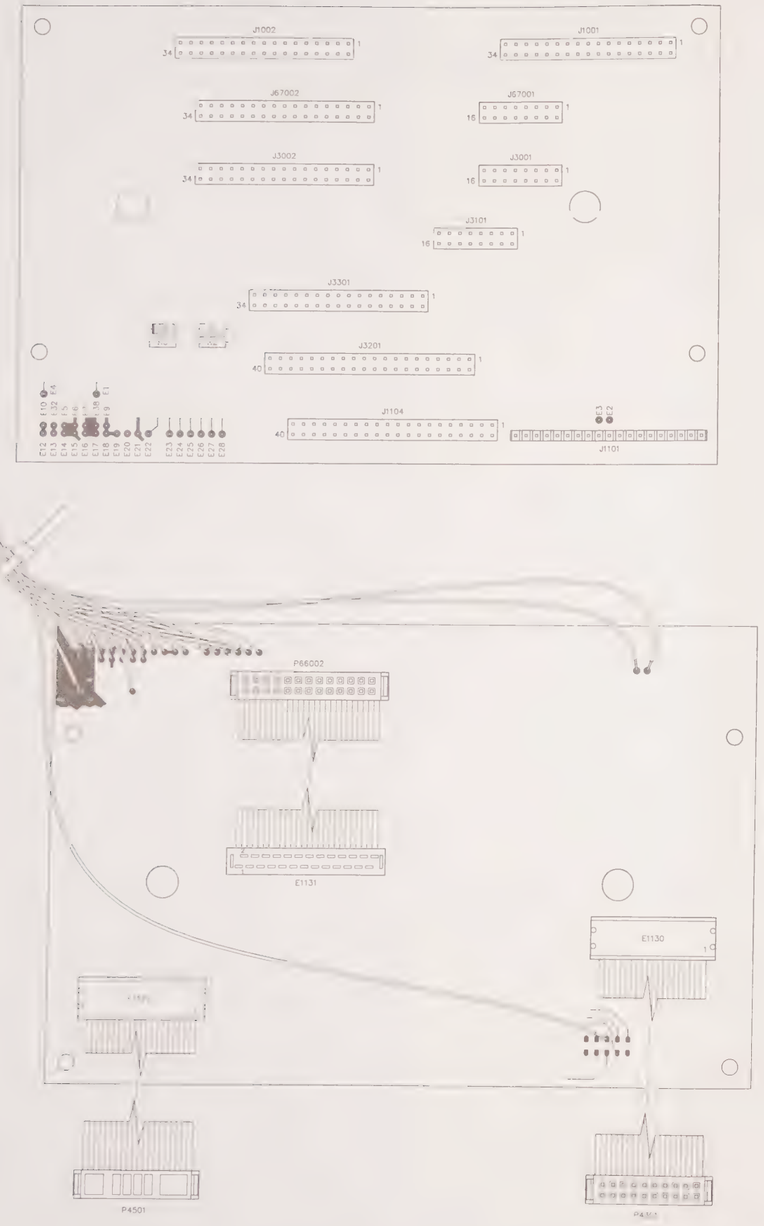
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 1100 (I.E., R1 IS R1101).

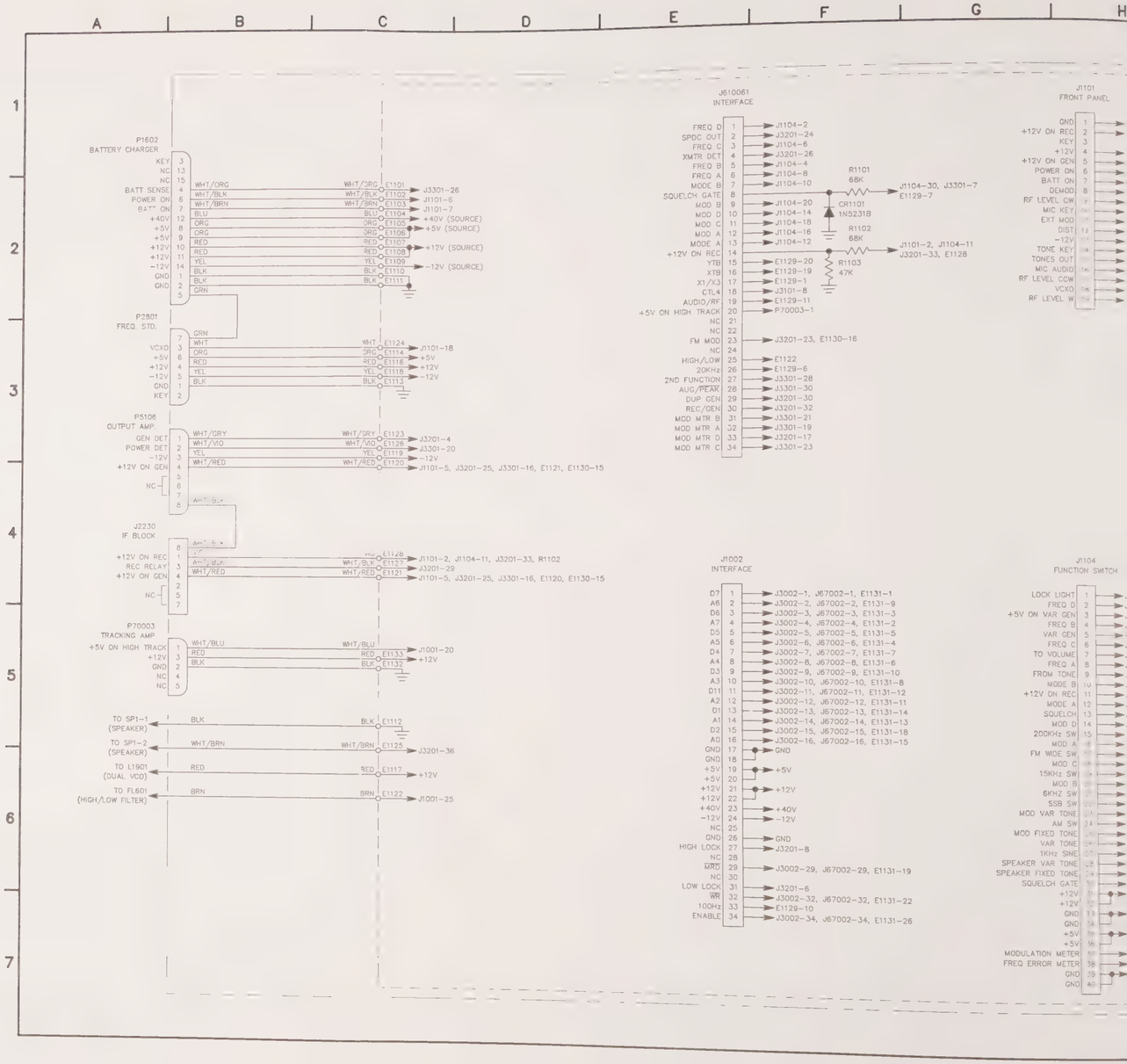
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

Figure 6-7 Motherboard/Wire Harness Assembly (FM/AM-1200S) (0000-5710-800-A1)



MOTHERBOARD/WIRE HARNESS ASSY (FM/AM-1200A)
(7007-5580-000)



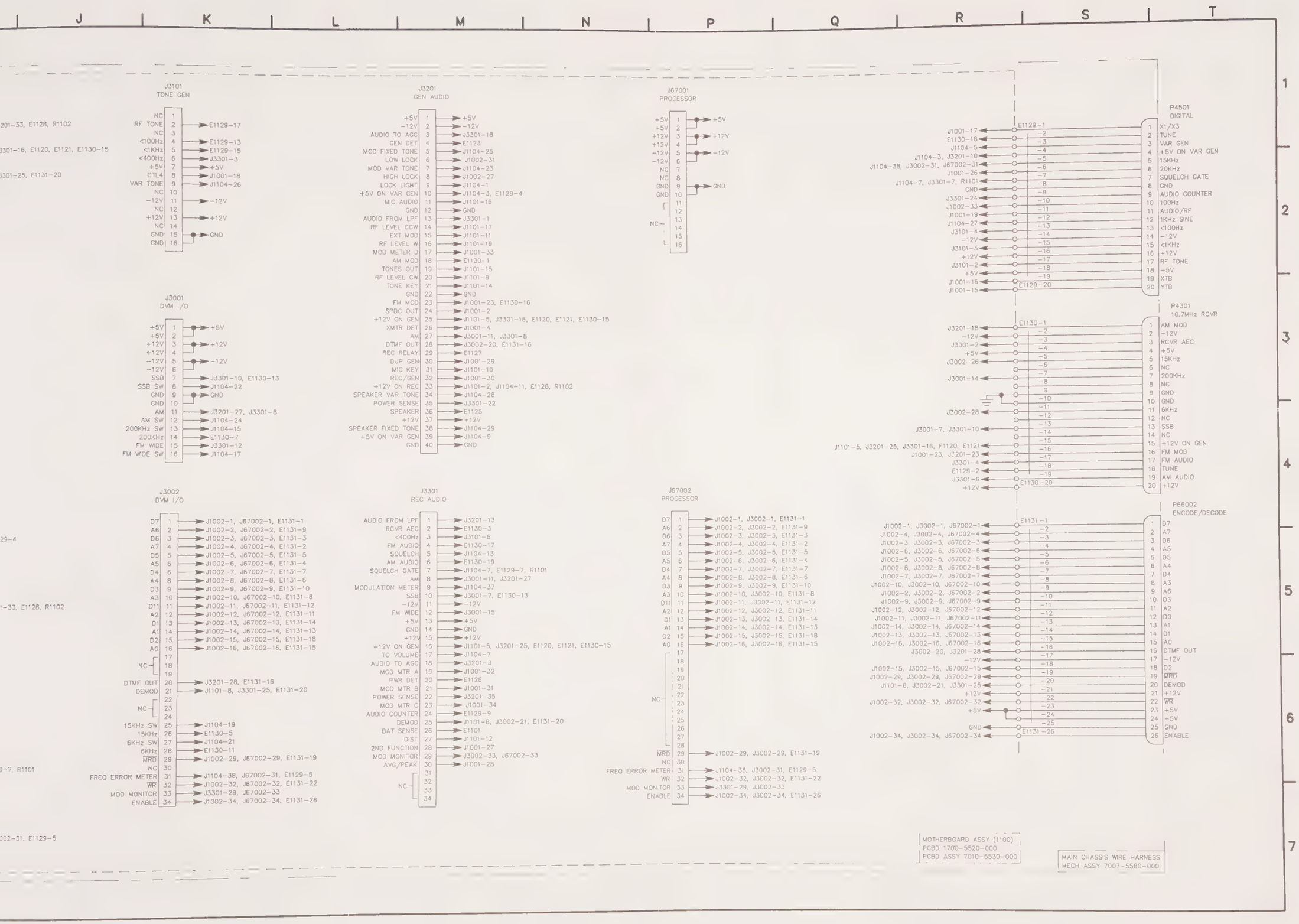
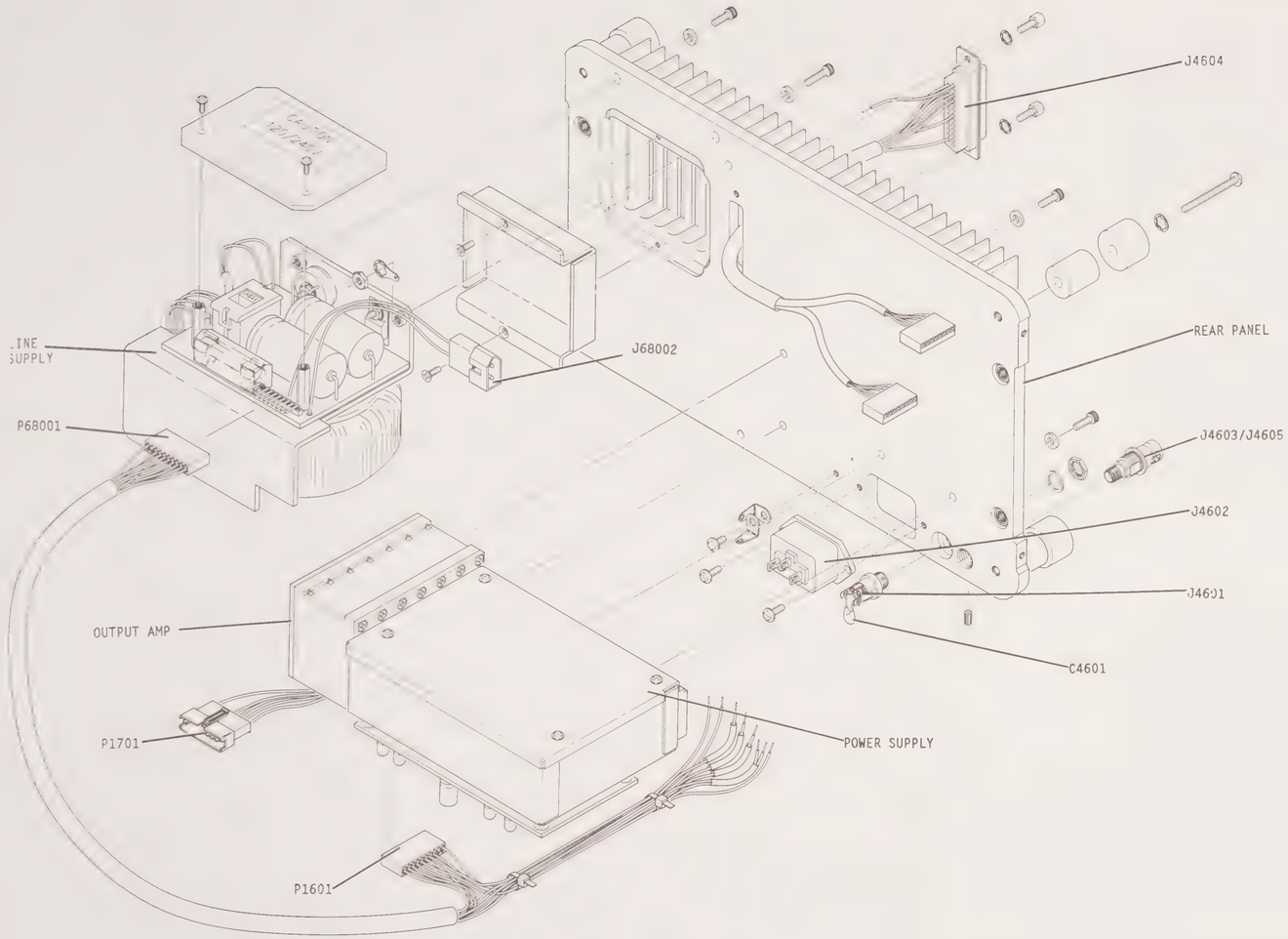
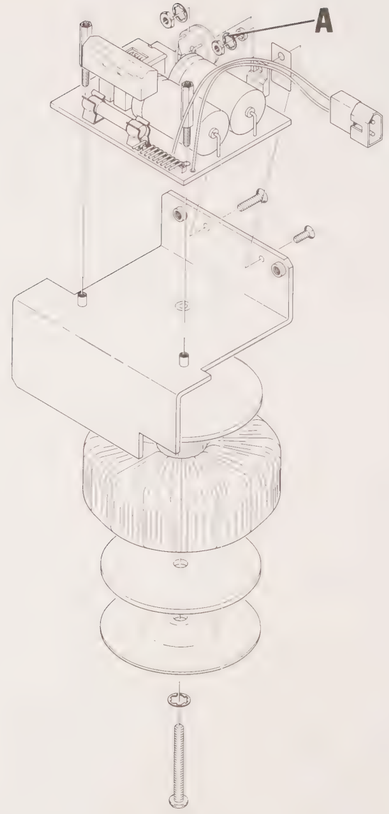


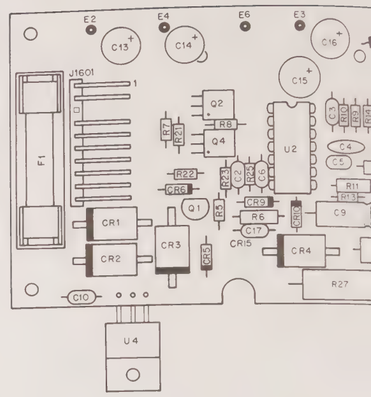
Figure 6-8 Motherboard/Wire Harness Assembly (FM/AM-1200A) (0000-5510-000-E1)



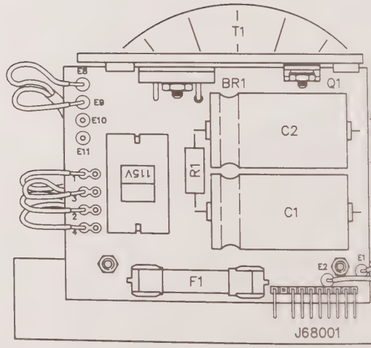
REAR PANEL ASSY (FM/AM-1200S)
(7005-8040-100-A3)



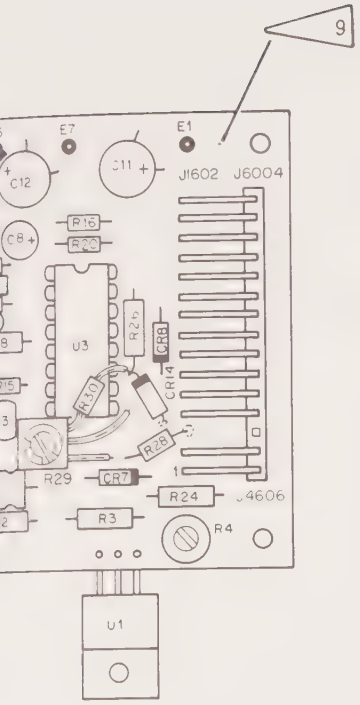
LINE SUPPLY PC BOARD ASSY (FM/AM-1200S)
(7010-8030-000-A3)



BATTERY CHARGER PC BOA
(FM/AM-1200S/A) (7010-

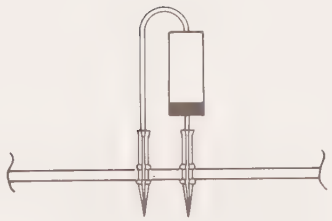


DETAIL A



ASSY
83-800-D2)

DETAIL **B**

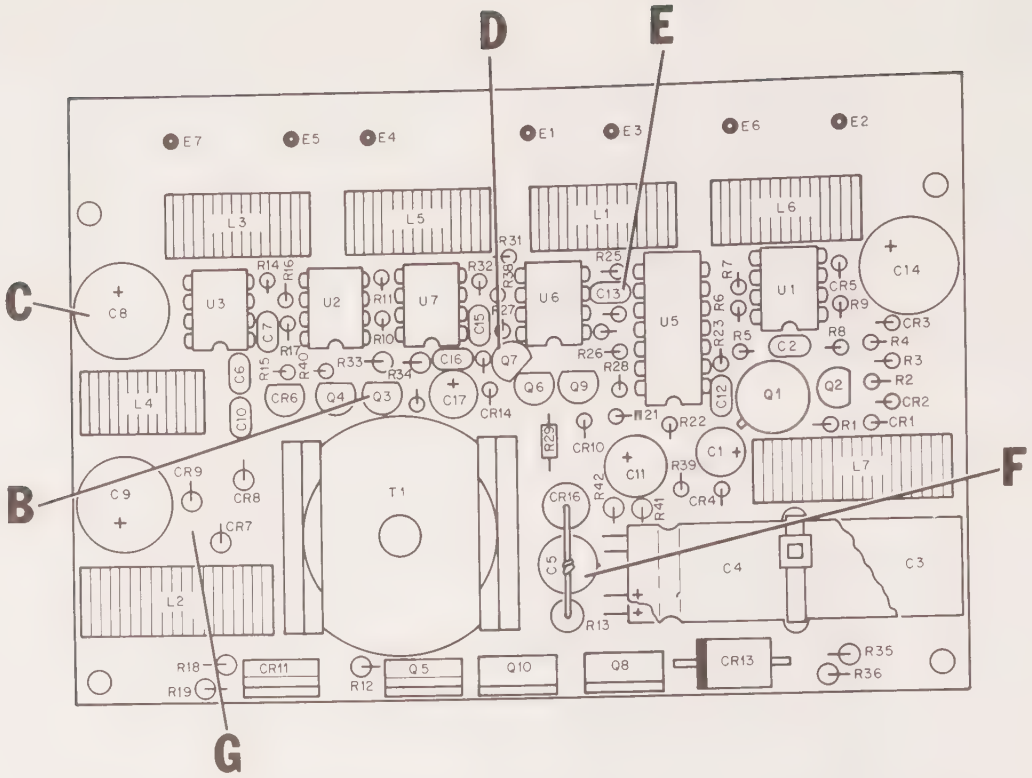


APPLIES TO CR7, CR8, CR9, CR10

DETAIL **C**

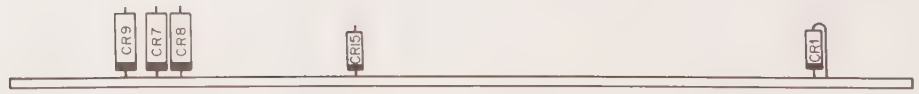
DETAIL **D**

DETAIL **E**



INVERTER SUPPLY PC BOARD ASSY
(FM/AM-1200S/A) (7010-6133-900-D2)

DETAIL **F**



DETAIL **G**

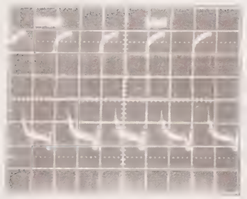
Figure 6-9 Rear Panel/Power Supply Assembly (Sheet 1 of 3)
(0000-7712-400-B2)

1

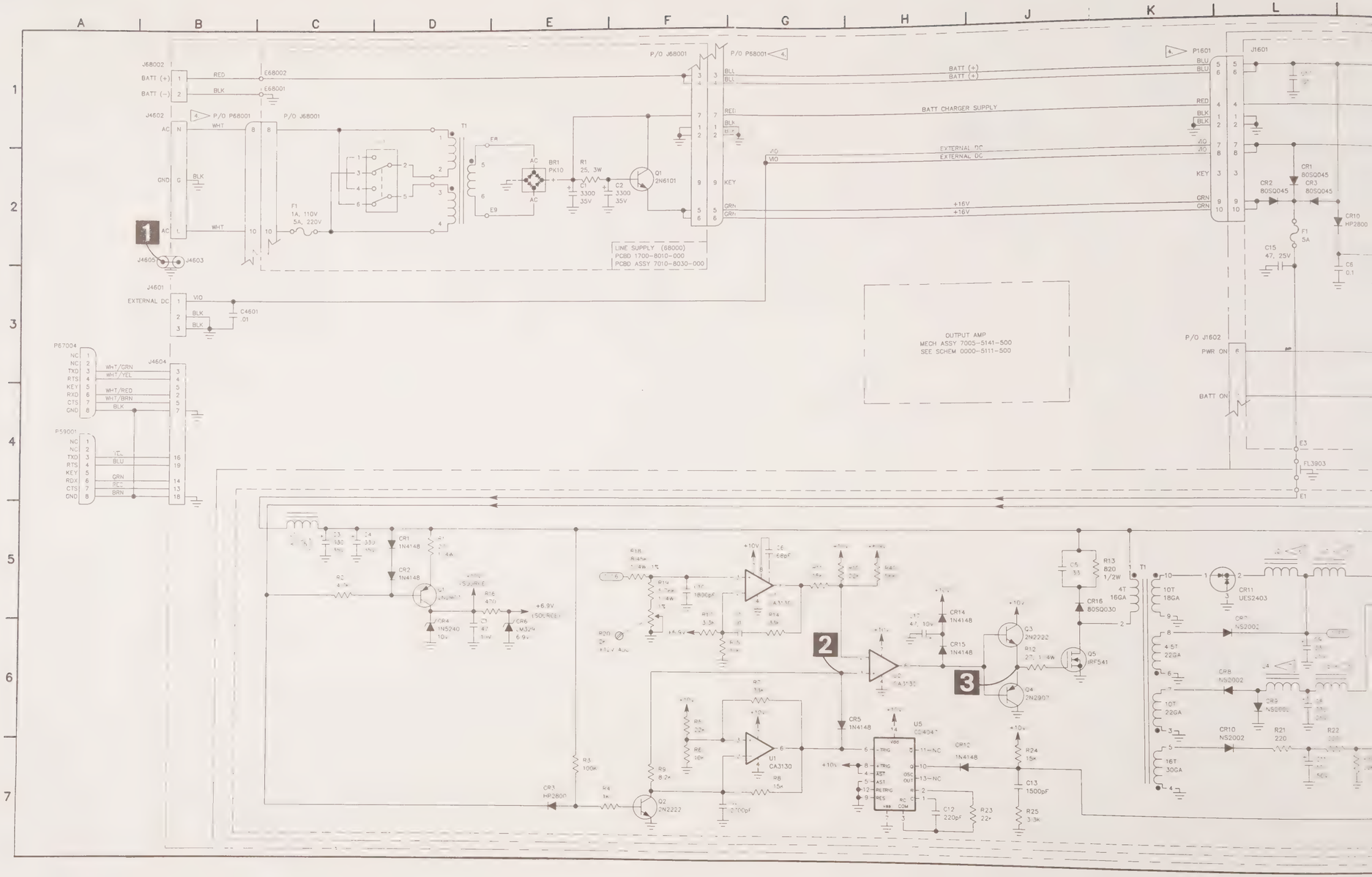
X1 PROBE

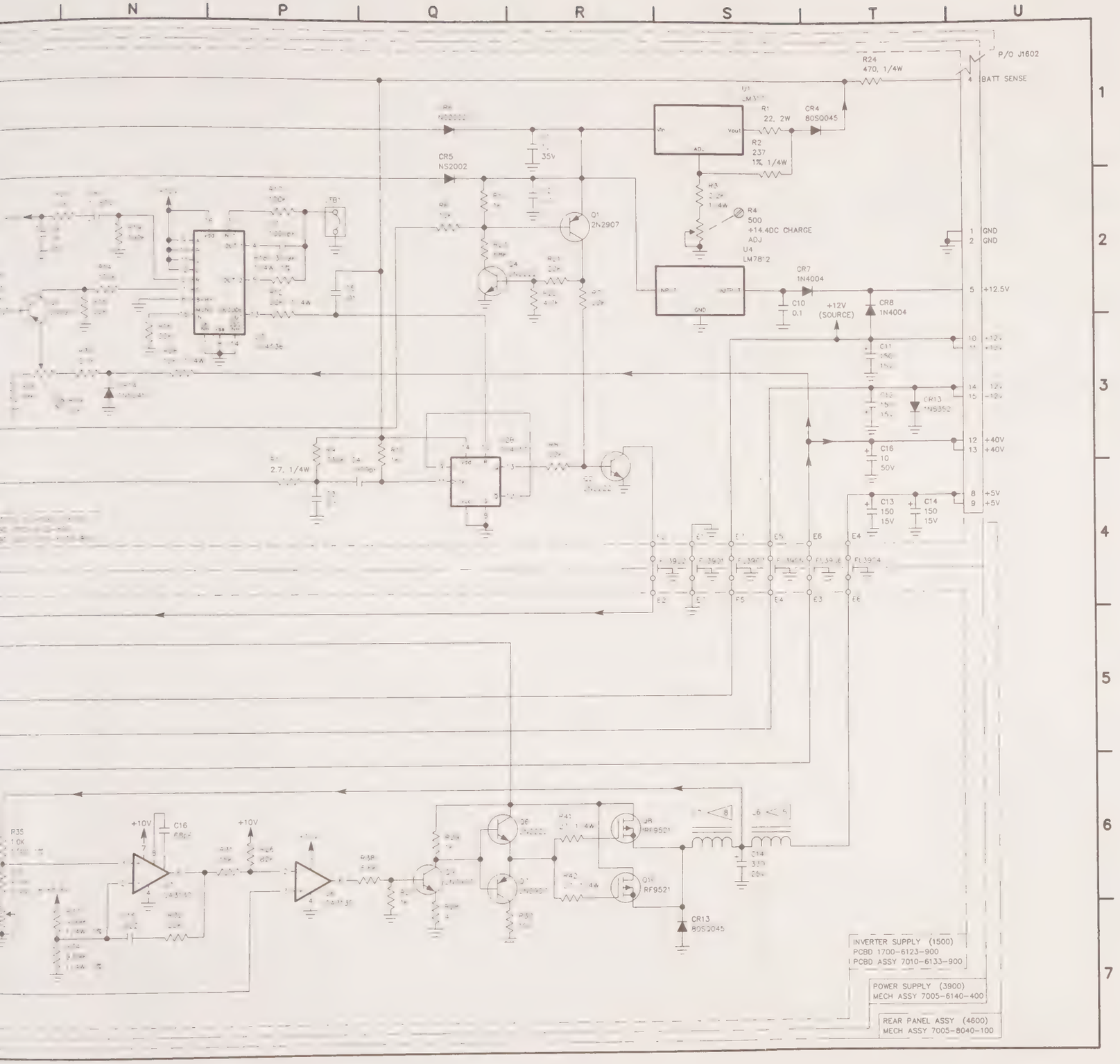
2

3



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz, WITH NO INPUT SIGNAL IN RECEIVE MODE USING AN X10 PROBE, UNLESS OTHERWISE NOTED.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 7005-8040-100 - 4600 (I.E., R1 IS R4601).
   B. 7005-6140-400 - 3900 (I.E., C1 IS C3901).
   C. 7010-6133-800 - 1600 (I.E., U1 IS U1601).
   D. 7010-6133-900 - 1500 (I.E., R1 IS R1501)
   E. 7010-8030-000 - 68000 (I.E., C1 IS C68001).

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4. P1601 AND P68001 ARE PART OF THE REAR PANEL WIRE HARNESS (7005-5140-301).

5. L1501, L1503, L1505 AND L1506 ARE 30 TURNS, 20 AWG TORROID INDUCTORS.

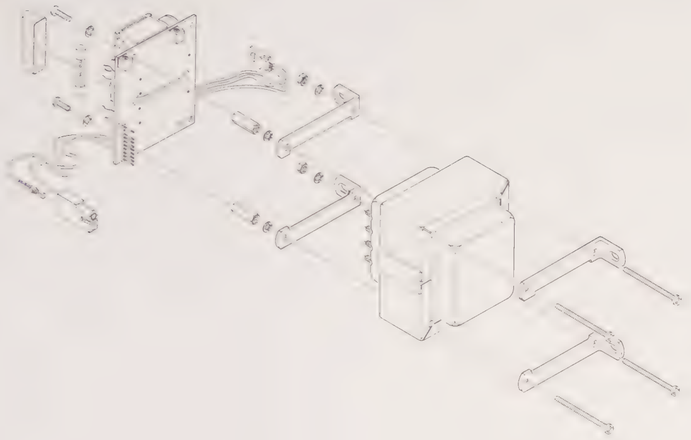
6. L1502 IS A 40 TURN, 18 AWG TORROID INDUCTOR.

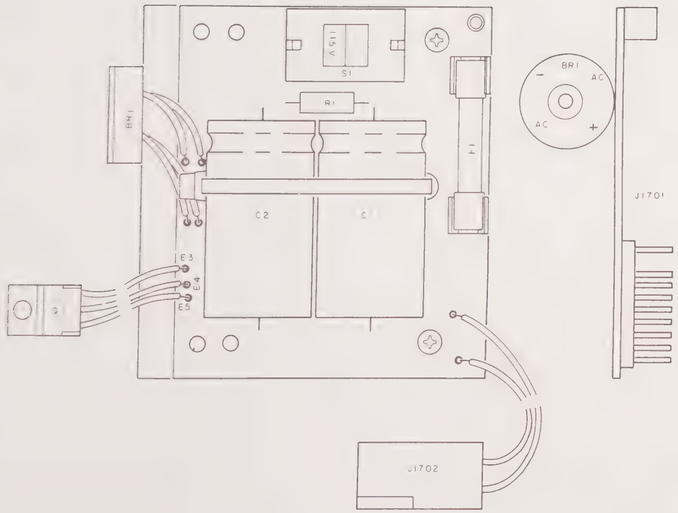
7. L1504 IS A 100 TURN, 24 AWG TORROID INDUCTOR.

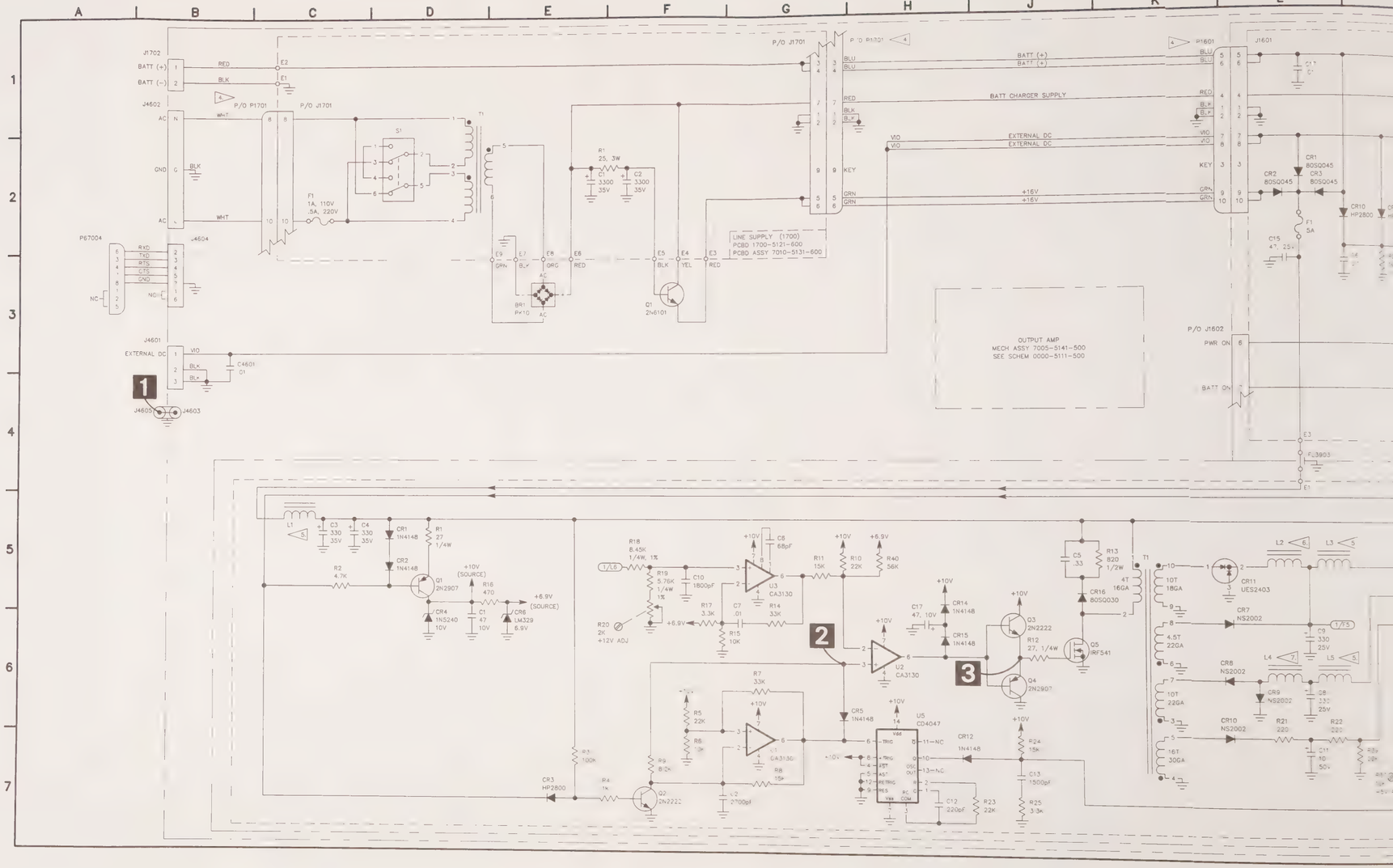
8. L1507 IS A 30 TURN, 18 AWG TORROID INDUCTOR.

9. J6004 USED FOR CELLULAR-READY UNITS LINE SUPPLY. J1602 IS STANDARD.

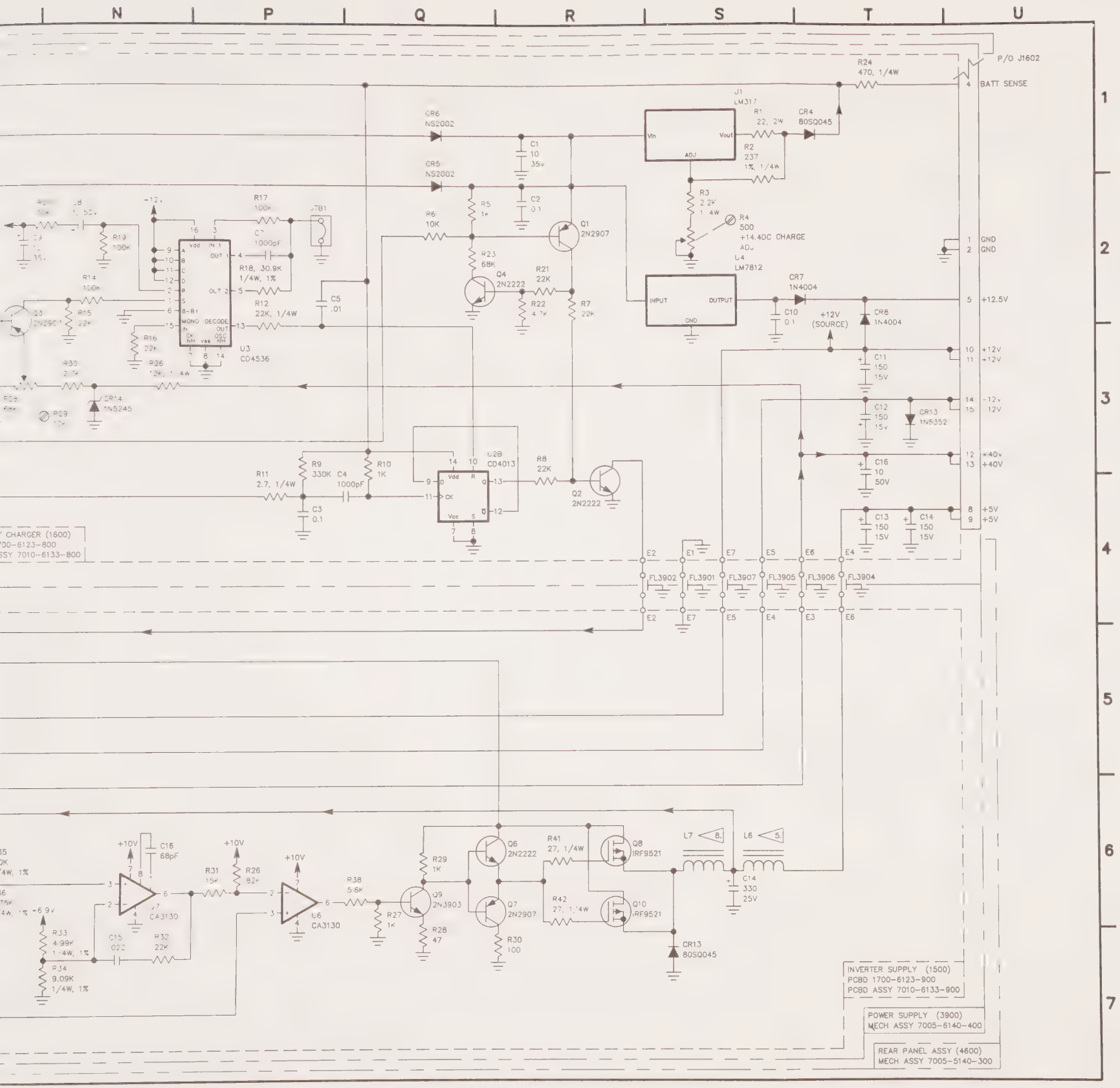
Figure 6-9 Rear Panel/Power Supply Assembly (Sheet 2 of 3) (0000-7712-400-B2)







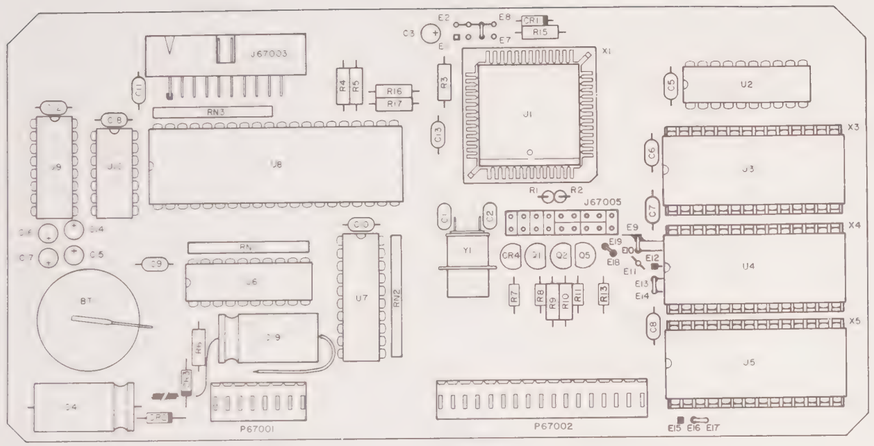
LINE SUPPLY PC BOARD ASSY (FM/AM-1200A)
(7010-5131-600-D8)

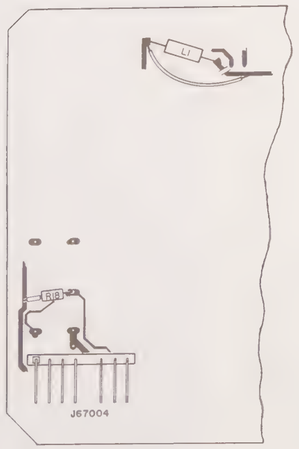


NOTES:

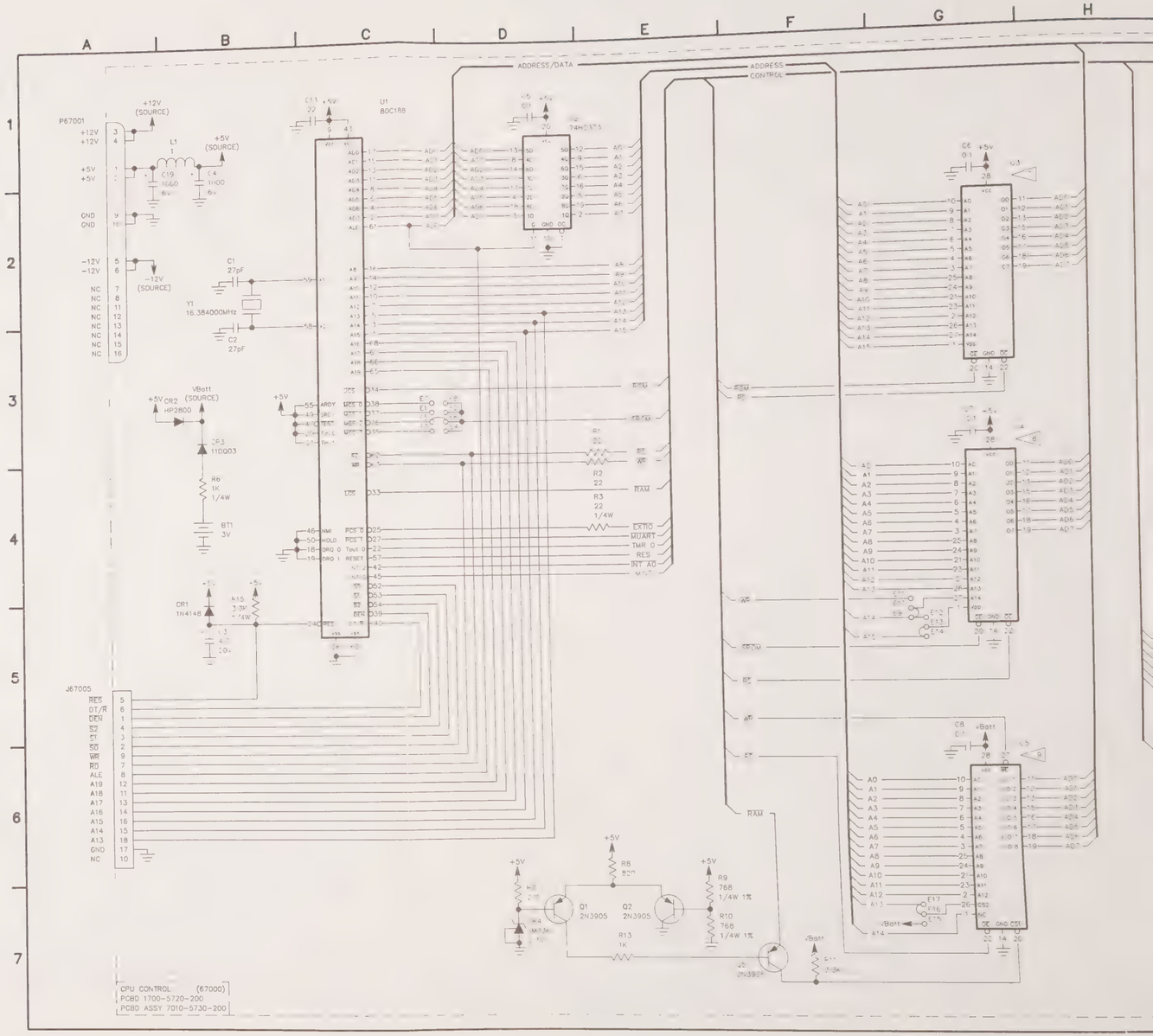
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   - A. 7005-8040-100 - 4600 (I.E., R1 IS R4601).
   - B. 7005-6140-400 - 3900 (I.E., C1 IS C3901).
   - C. 7010-6133-800 - 1600 (I.E., U1 IS U1601).
   - D. 7010-6133-900 - 1500 (I.E., R1 IS R1501)
   - E. 7010-8030-000 - 68000 (I.E., C1 IS C68001).
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.
4. P1601 AND P68001 ARE PART OF THE REAR PANEL WIRE HARNESS (7005-5140-301).
5. L1501, L1503, L1505 AND L1506 ARE 30 TURNS, 20 AWG TORROID INDUCTORS.
6. L1502 IS A 40 TURN, 18 AWG TORROID INDUCTOR.
7. L1504 IS A 100 TURN, 24 AWG TORROID INDUCTOR.
8. L1507 IS A 30 TURN, 18 AWG TORROID INDUCTOR.

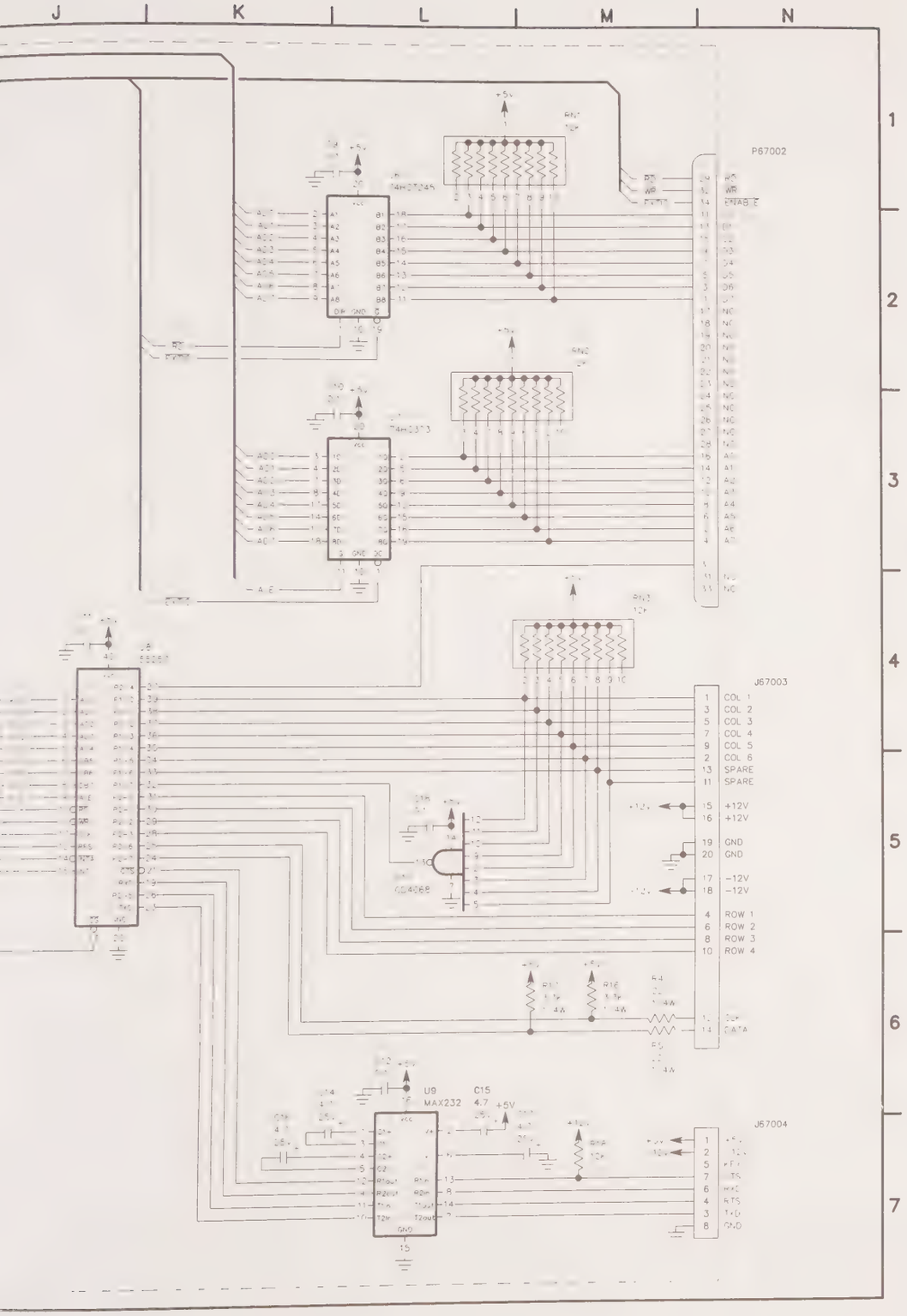
Figure 6-9 Rear Panel/Power Supply Assembly (Sheet 3 of 3) (0000-7712-400-B2)





PROCESSOR PC BOARD ASSY
(7010-5730-200-D5)





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 67000 (I.E., R1 IS R67001).

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4 THRU 6. NOT USED.

7. U67003 IC TYPE BY UNIT MODEL:

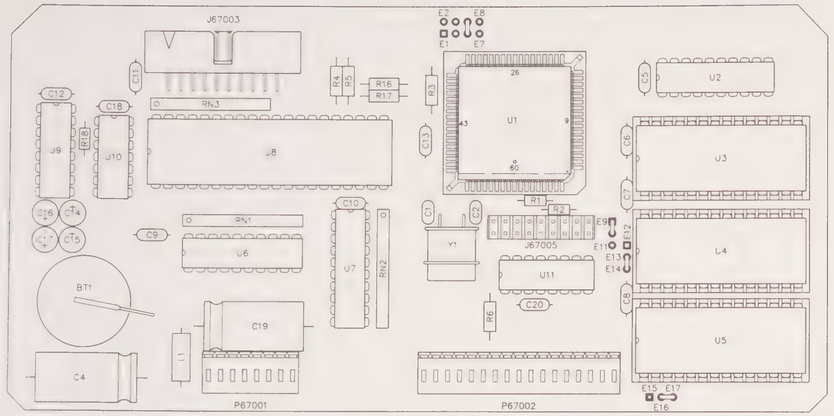
MODEL	IC TYPE
FM/AM-1200S	27C512
FM/AM-1200A	27256

8. U67004 IC TYPE BY MODEL:

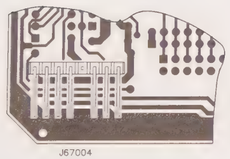
MODEL	IC TYPE
FM/AM-1200S (STD)	NO SOCKET
W/TRACKING (OPT 12)	27C512
FM/AM-1200A (ALL)	NO SOCKET

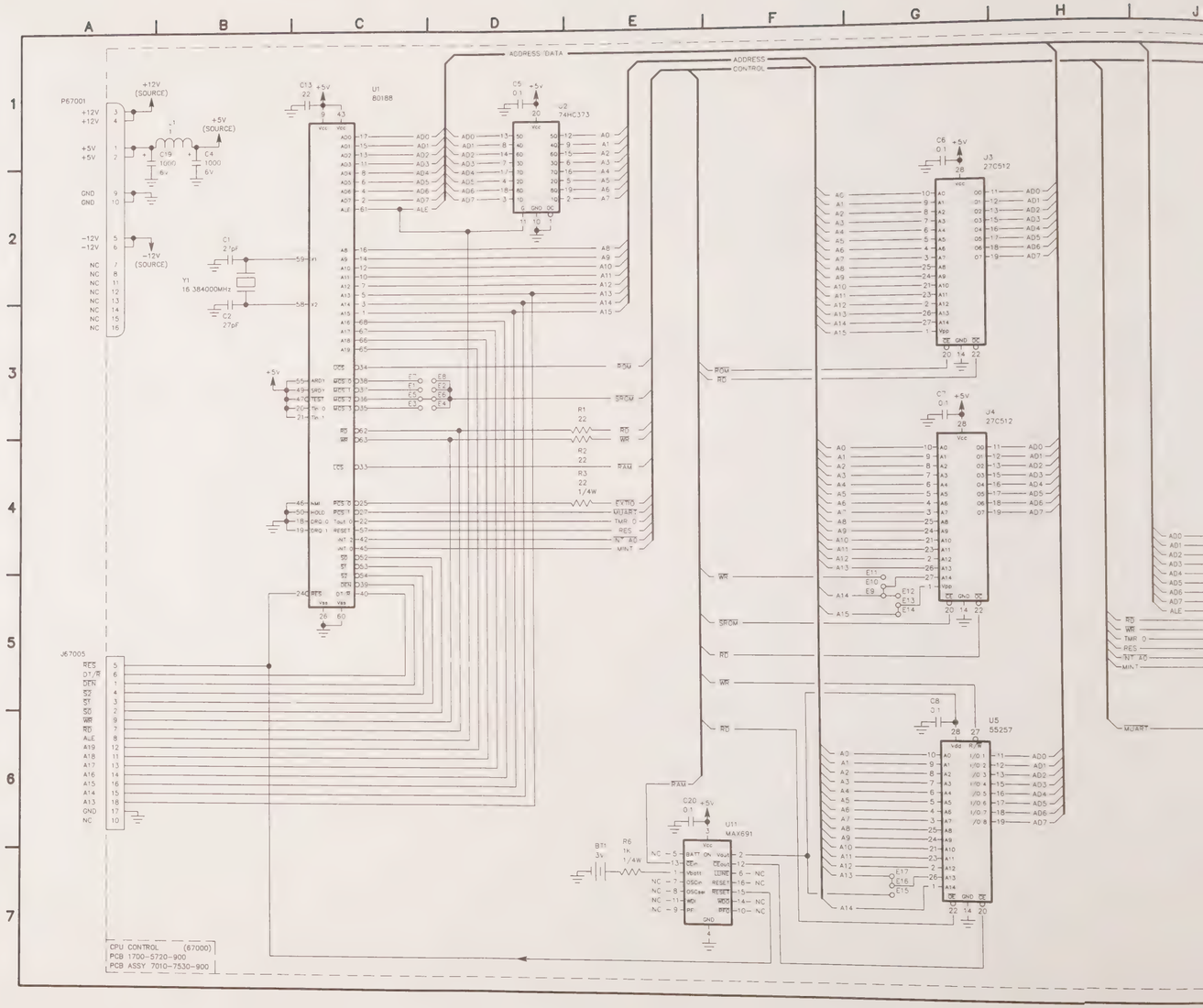
9. U67005 USES IC TYPE 55257.

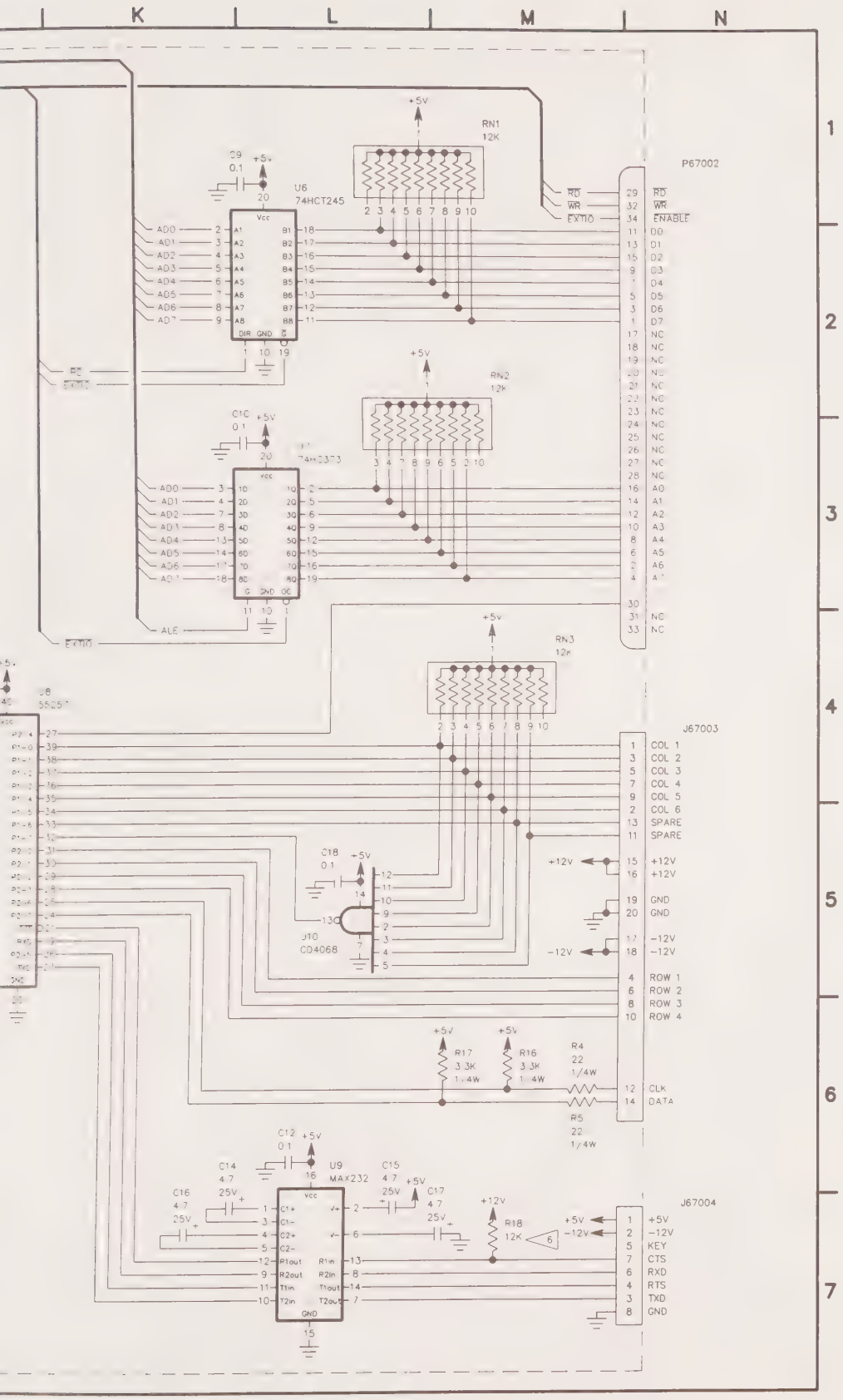
Figure 6-10 Processor PC Board Assembly (FM/AM-1200S thru S/N 8300; FM/AM-1200A thru S/N 1706) (0000-5710-200-D2)



PROCESSOR PC BOARD ASSY
(7010-5730-900-B)







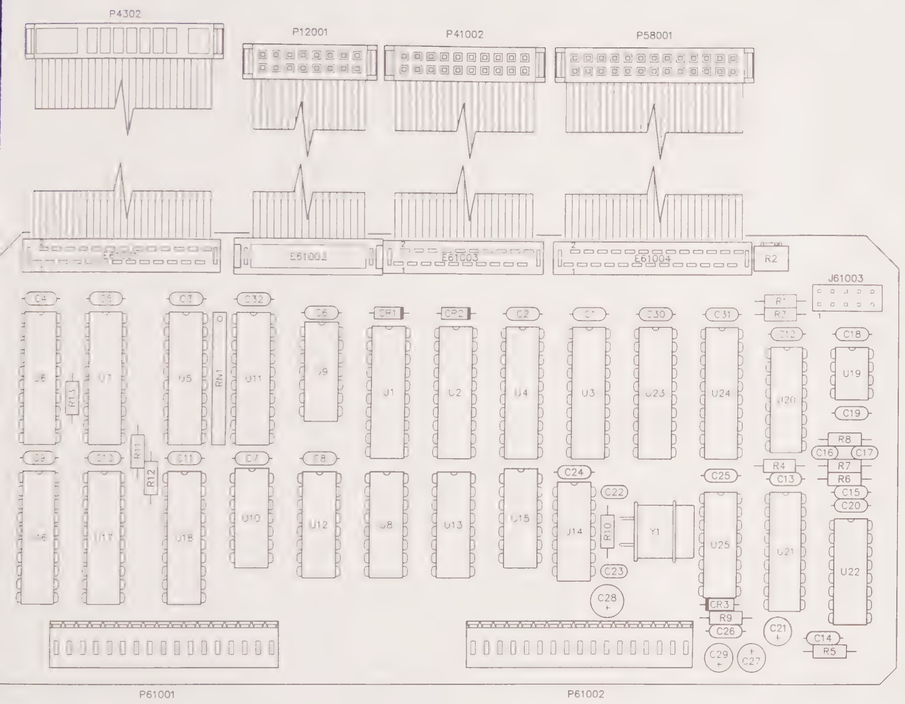
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 67000 (I.E., R1 IS R67001).

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

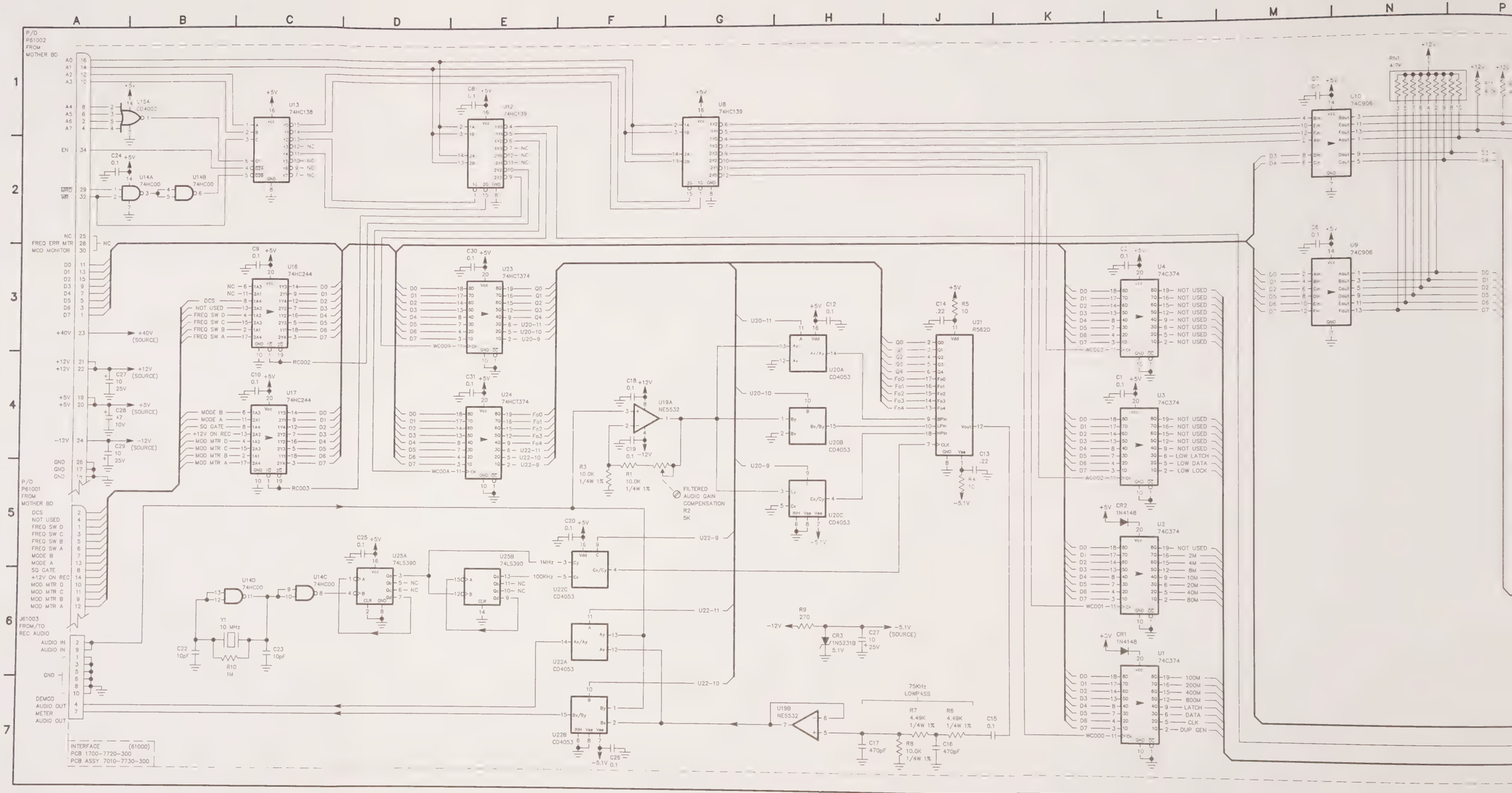
Figure 6-11 Processor PC Board Assembly (FM/AM-1200S from S/N 8301 & On; FM/AM-1200A from S/N 1707 & On) (0000-7510-400-B)



INTERFACE PC BOARD ASSY
(FM/AM-1200S) (7010-7730-300-C)

ADDRESS	STATUS	DATA BITS 7	6	5	4	3	2	1	0
C000	W	DUPLEX GENERATOR	DUPLEX CLOCK	DUPLEX DATA	DUPLEX LATCH	RF: 800 M	RF: 400 M	RF: 200 M	RF: 100 M
C001	W	RF: 80 M	RF: 40 M	RF: 20 M	RF: 10 M	RF: 8 M	RF: 4 M	RF: 2 M	RF: 1 M
C002	W	RF: 800 K	RF: 400 K	RF: 200 K	RF: 100 K	RF: 80 K	RF: 40 K	RF: 20 K	RF: 10 K
	R	FREQ METER SWITCH A	FREQ METER SWITCH B	FREQ METER SWITCH C	FREQ METER SWITCH D	DCS NEG DEV	DCS POS DEV	SPARE	SPARE
C003	W	RF: 8 K	RF: 4 K	RF: 2 K	RF: 1 K	RF: 800 Hz	RF: 400 Hz	RF: 200 Hz	RF: 100 Hz
	R	MOD METER SWITCH A	MOD METER SWITCH B	MOD METER SWITCH C	MOD METER SWITCH D	+12V ON RCV	SQUELCH GATE	MODE SWITCH A	MODE SWITCH B
C004	W	TONE GEN 52424.8 Hz	TONE GEN 26212.4 Hz	TONE GEN 13106.2 Hz	TONE GEN 6553.6 Hz	TONE GEN 3276.8 Hz	TONE GEN 1638.4 Hz	TONE GEN 819.2 Hz	TONE GEN 409.6 Hz
C005	W	TONE GEN 204.8 Hz	TONE GEN 102.4 Hz	TONE GEN 51.2 Hz	TONE GEN 25.6 Hz	TONE GEN 12.8 Hz	TONE GEN 6.4 Hz	TONE GEN 3.2 Hz	TONE GEN 1.6 Hz
C006	W	TONE GEN 0.8 Hz	TONE GEN 0.4 Hz	TONE GEN 0.2 Hz	TONE GEN 0.1 Hz	TONE GEN CTL 3	TONE GEN CTL 2	TONE GEN CTL 1	TONE GEN CTL 0
C007	W	MOD METER A	MOD METER B	MOD METER C	MOD METER D	MOD METER AVG/PEAK	MOD METER 2ND FREQ	REC (1) GEN (0)	DUP ENABLE (0)
C008	W	SPARE	SPARE	FREQ ERROR XTB	FREQ ERROR X1/X3	FREQ ERROR YTB	FREQ ERROR AUDIO/RF	TONE CTL 4	SPARE
C010	W	MODULATION 6 K	MODULATION 15 K	MODULATION 200 K	MODULATION FM WIDE	MODULATION SSB	MODULATION AM		METER SELECT
	R		METERS STATUS	METERS POLARITY	METERS OVERRANGE	METERS B12	METERS B11	METERS B10	METERS B9
C011	R	METERS B8	METERS B7	METERS B6	METERS B5	METERS B4	METERS B3	METERS B2	METERS B1
C012	R			MODULATION 6 K	MODULATION 15 K	MODULATION 200 K	MODULATION FM WIDE	MODULATION SSB	MODULATION AM
C013	W	DTMF RESET				WRITE - DTMF LATCH			
	R	DTMF READY	DTMF INSTALLED						

Figure 6-12 Interface PC Board Assembly (FM/AM-1200S)
(Sheet 1 of 2) (0000-7710-300-D1)



P/O P61002 FROM MOTHER BD
P/O P61001 FROM MOTHER BD
J61003 FROM/TO REC AUDIO
INTERFACE (61000)
PCB 1700-7720-300
PCB ASSY 7010-7730-300
FILTERED AUDIO GAIN COMPENSATION R2 5K
75KHz LOWPASS

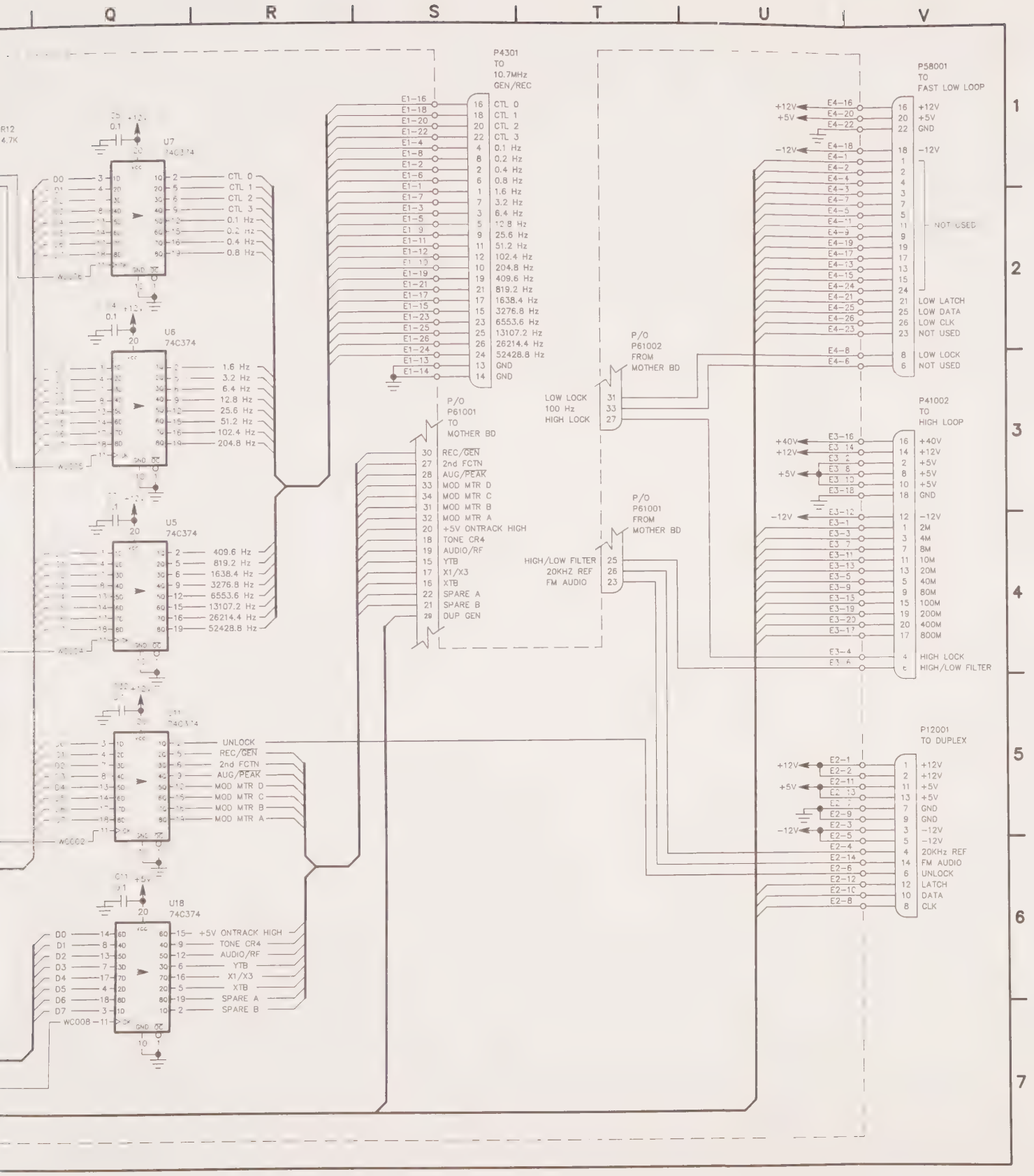
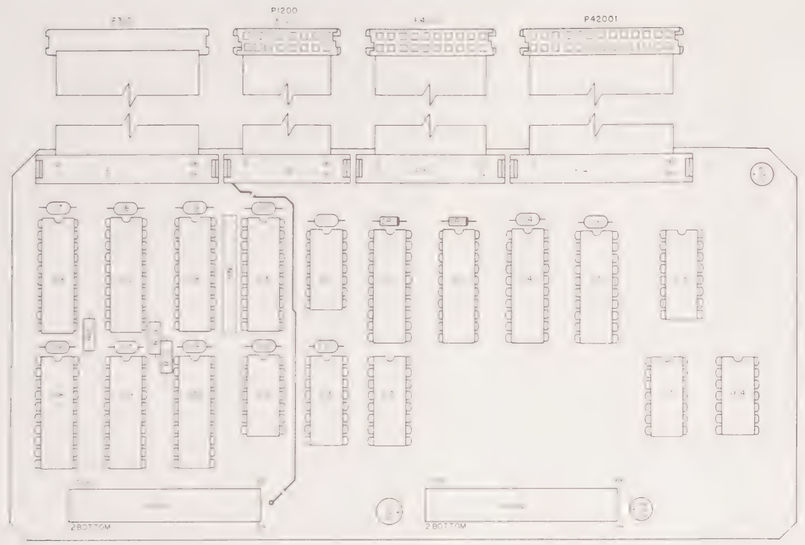


Figure 6-12 Interface PC Board Assembly (FM/AM-1200S) (Sheet 2 of 2) (0000-7710-300-D1)

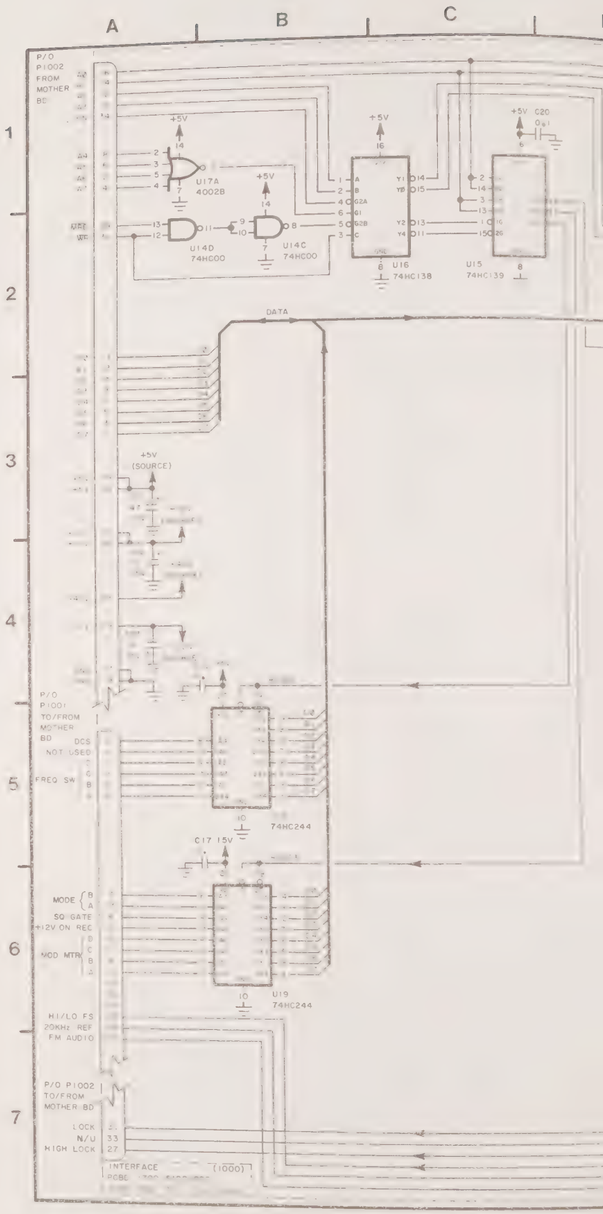


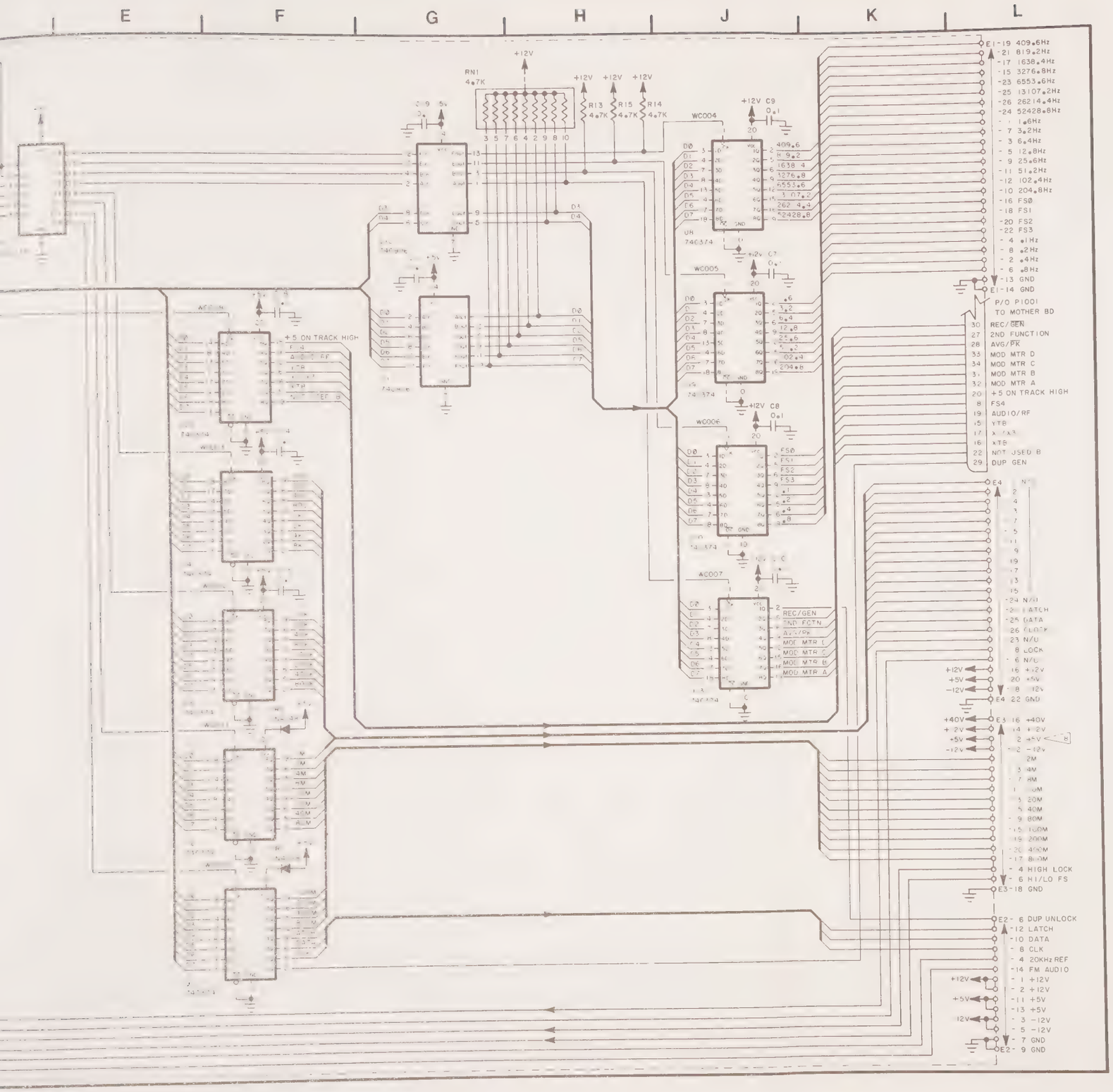
INTERFACE PC BOARD ASSY
(FM/AM-1200A) (7010-5130-800-J8)

MODULATION METER CONTROL (P1001)											
		INPUT				OUTPUT					
MOD METER CONTROL POSITION		MOD MTR A PIN 12	MOD MTR B PIN 9	MOD MTR C PIN 11	MOD MTR D PIN 10	MOD MTR A PIN 32	MOD MTR B PIN 31	MOD MTR C PIN 34	MOD MTR D PIN 33	AVG/PK PIN 28	2ND FUNC PIN 27
WF	150										
	15										
WA	150										
	15										
kHz/ $X10	2										
	6										
	20										
BATT											
SIG											
DIST											
SINAD											
1 = +5 VDC 0 = 0 VDC						1 = + 12 VDC 0 = 0 VDC					

FREQ ERROR METER CONTROL (P1001)									
		INPUT				OUTPUT			
FREQ ERROR METER POSITION		FREQ SW A PIN 6	FREQ SW B PIN 5	FREQ SW C PIN 3	FREQ SW D PIN 1	XTB PIN 16	YTB PIN 15	X1/X3 PIN 17	AUDIO/RF PIN 19
1 = +5 VDC 0 = 0 VDC						1 = +5 VDC 0 =			

MODE CONTROL SWITCH					
	P1001 INPUT		P1001 OUTPUT		E1002-6
MODE CONTROL POSITION	MODE A PIN 13	MODE B PIN 7	REC/GEN PIN 30	DUP GEN PIN 29	DUP UNLOCK
SEN	0	0	0	0	*
REC	1	0	1	0	*
DUP	0	1	1	0	**
DUP/GEN	1	1	0	*	*
0 = Ø VDC 1=+5 VDC			0 = 0 VDC 1 = 12 VDC	* = +5 VDC	
			** NORMALLY ZERO, ACTIVE DURING DIGITAL TRANSMISSION ONLY		





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE SCHEMATICS CARRY SERIES:

   A. FM/AM-1200S - 61000 (I.E., R1 IS R61001).
   B. FM/AM/1200A - 1000 (I.E., R1 IS R1001).

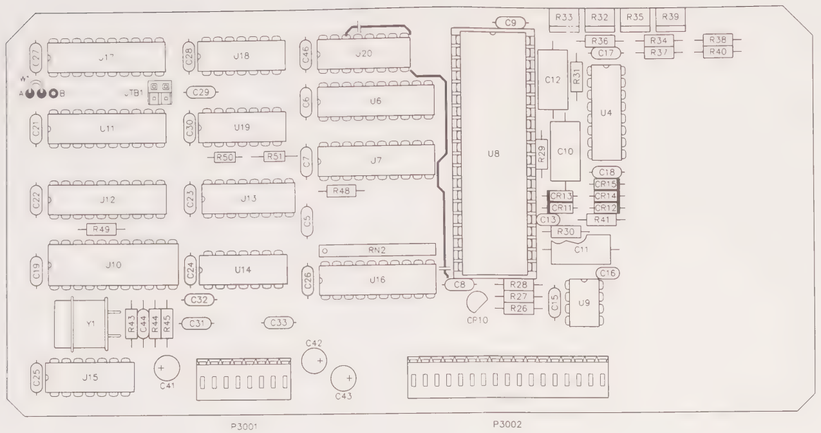
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

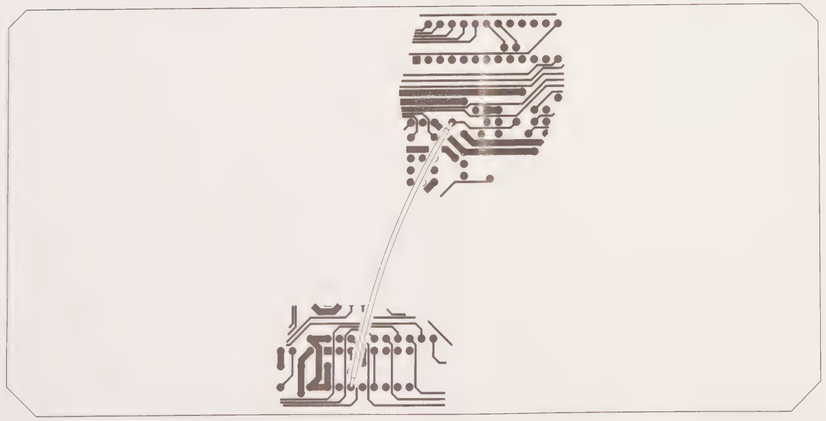
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

4. THRU 7. NOT USED.

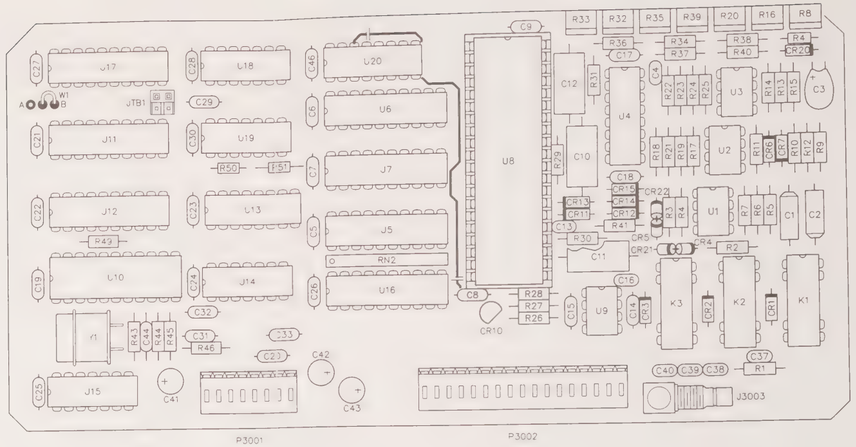
8. WITH TRACKING GENERATOR OPTION, PINS 2, 8 AND 10 ARE TIED BY 26 GA. SHIELDED BUS WIRE.

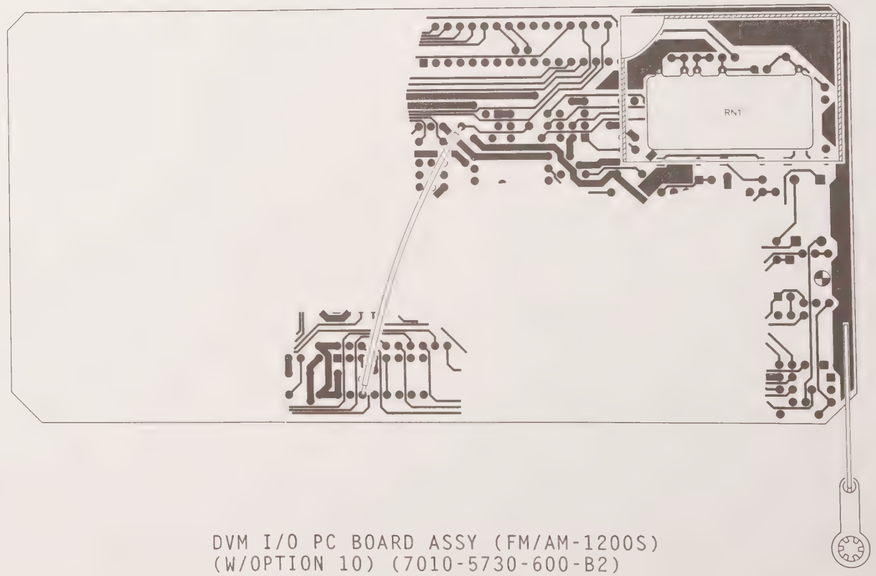
Figure 6-13 Interface PC Board Assembly (FM/AM-1200A) (0000-5110-800-J6)



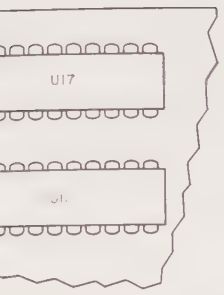


DVM I/O PC BOARD ASSY (FM/AM-1200S)
(W/O OPTION 10) (7010-5730-500-B1)

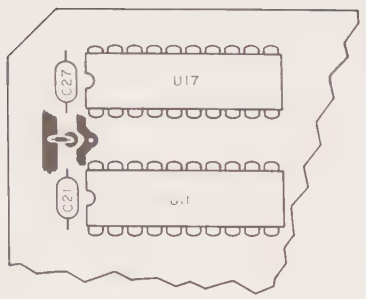




DVM I/O PC BOARD ASSY (FM/AM-1200S)
(W/OPTION 10) (7010-5730-600-B2)



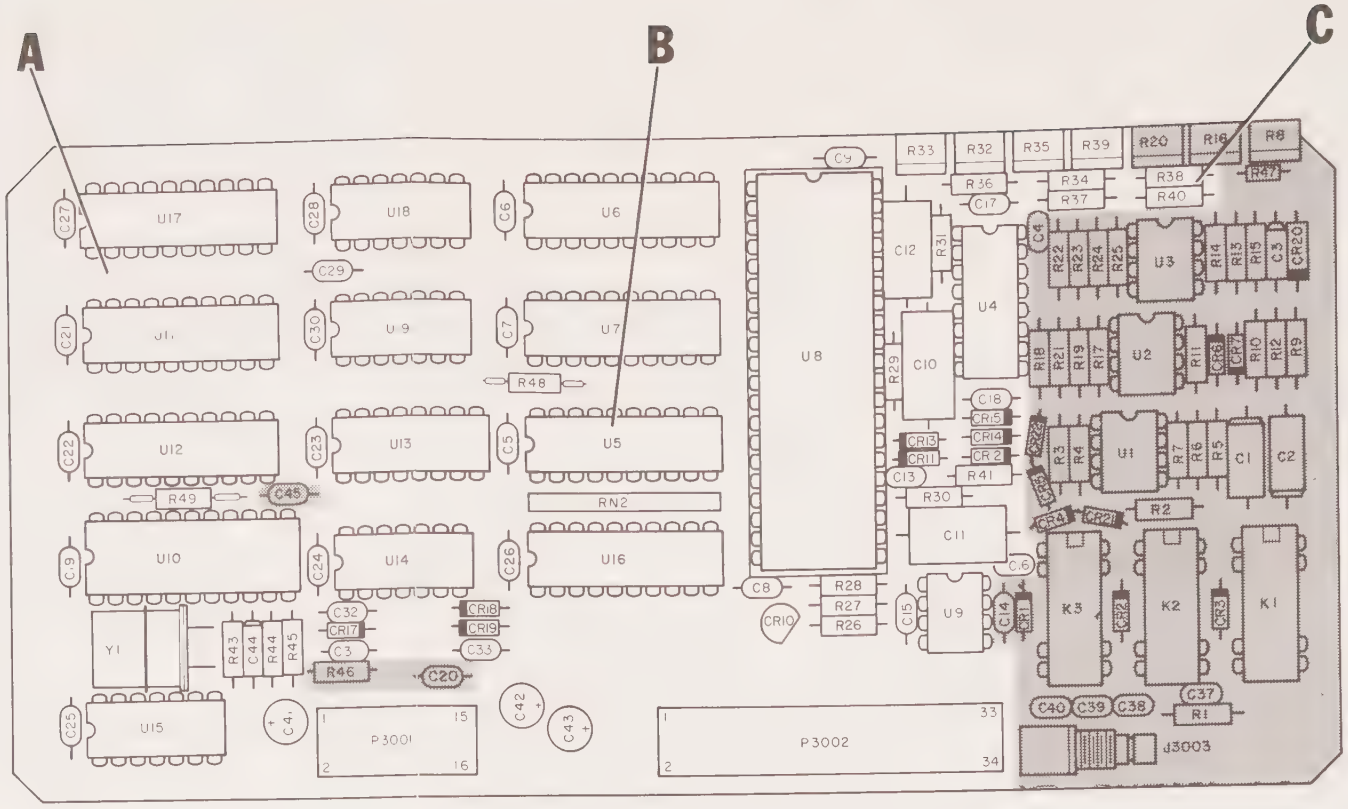
OCATION FOR OPTION
/O PC BOARD



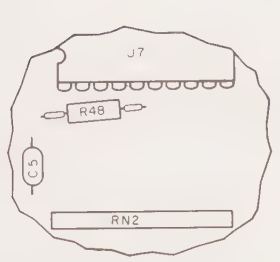
JUMPER LOCATION FOR
STANDARD DVM 1/O PC BOARD

DETAIL **A**

NOTE: SHADED AREAS FOR OPTION 10
DVM 1/O ONLY

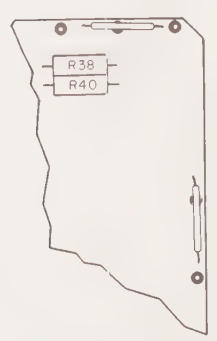


DVM I/O PC BOARD ASSY (FM/AM-1200A)
(W/OPTION 10-SHADED) (7010-5530-100-E7)



(STANDARD OPTION)

DETAIL **B**



BOTTOM VIEW
(STANDARD OPTION)

DETAIL **C**

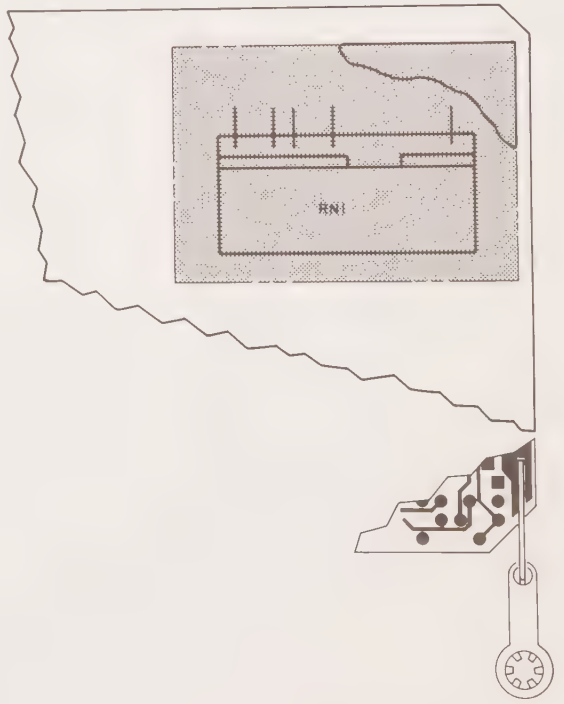
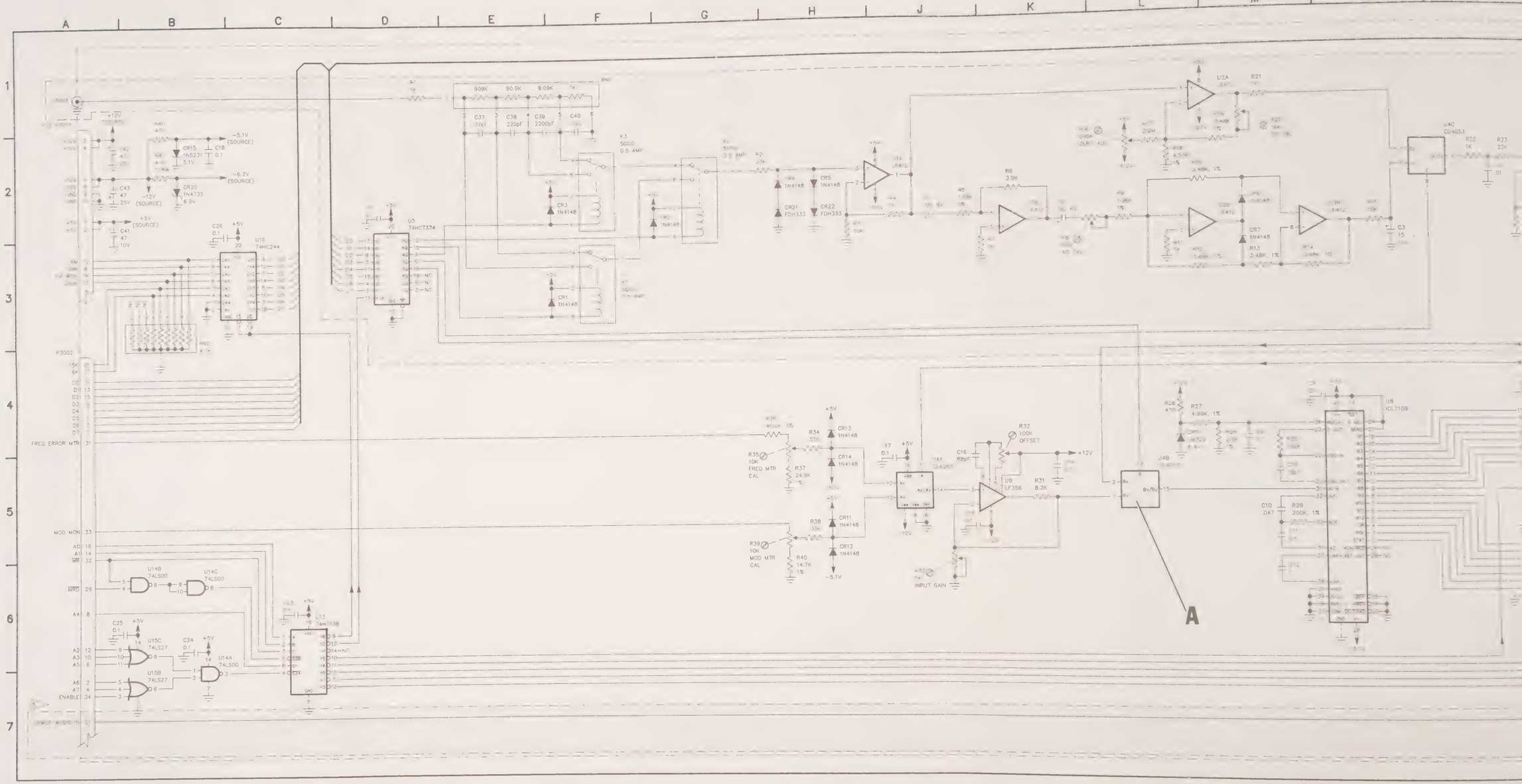
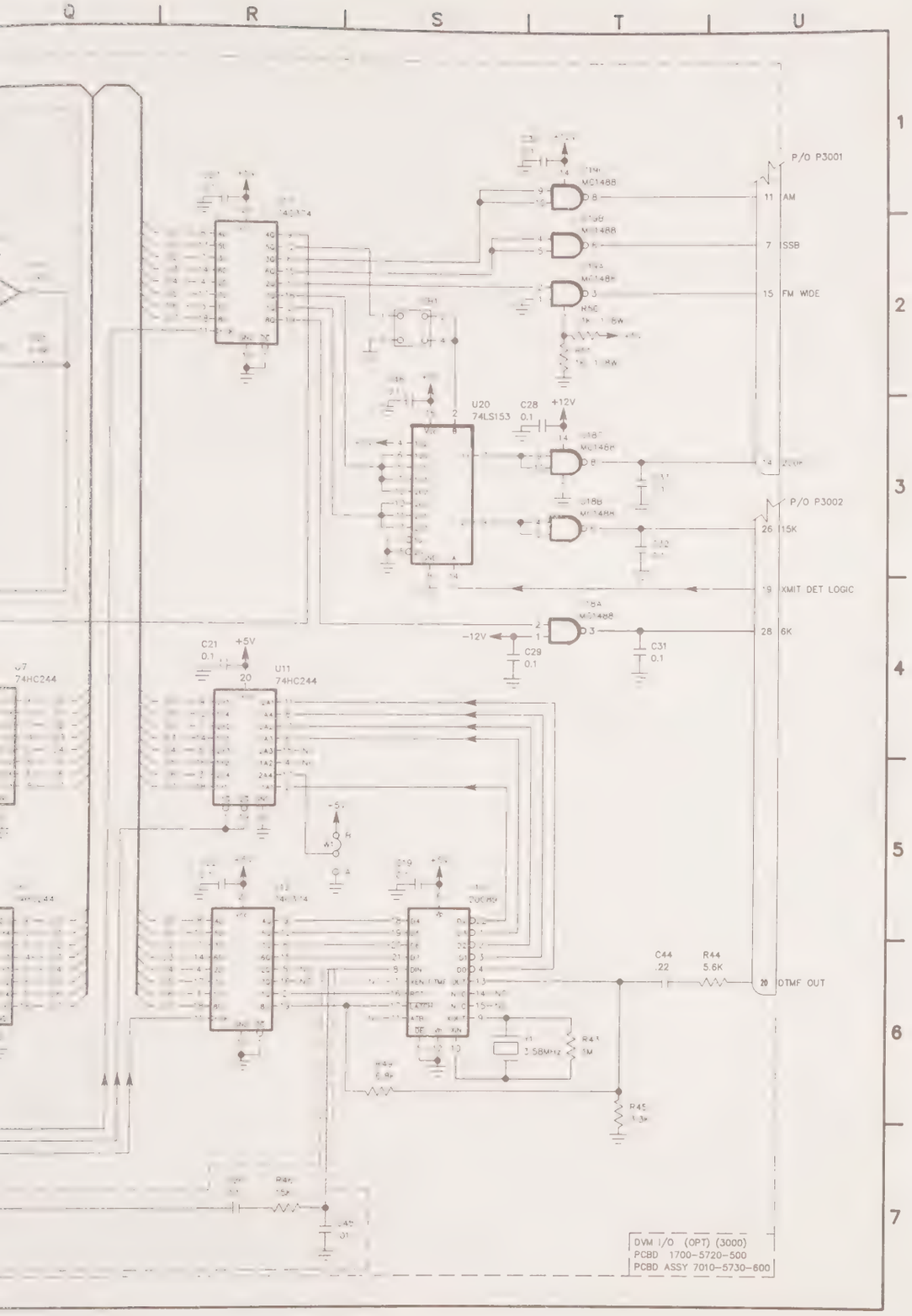


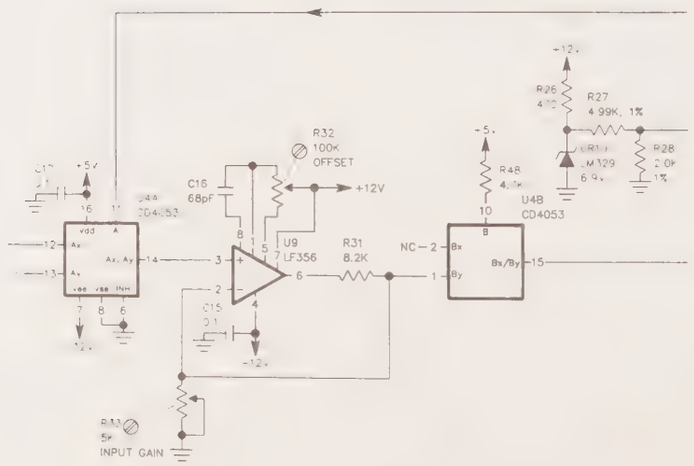
Figure 6-14 DVM I/O PC Board Assembly
(& DVM I/O W/OPTION 10)
(Sheet 1 of 3) (0000-5710-500-B)


A
B
C
D
E
F
G
H
J
K
L
M
N
P
1
2
3
4
5
6
7
+12V
−5.1V (SOURCE)
−6.2V (SOURCE)
−12V (SOURCE)
+5V (SOURCE)
CR15 1N5231 5.1V
CR20 1N4735 6.2V
C18 0.1
C43 47 25V
C41 47 10V
C26 0.1
C25 0.1
C24 0.1
U16 74HC244
U5 74HCT374
U15C 74LS27
U15B 74LS27
U14B 74LS00
U14C 74LS00
U14A 74LS00
U13 74HC138
P3002
FREQ ERROR MTR
MOD MON
WR
RD
ENABLE
909K
90.9K
9.09K
RN1
C37 22pF
C38 220pF
C39 2200pF
C40
K3 500Ω 0.5 AMP
K1 500Ω 0.5 AMP
CR3 1N4148
CR1 1N4148
CR5 1N4148
CR21 FDH333
CR22 FDH333
R6 3.9K
U2A
R21
R18 4.53K 1%
3.48K, 1%
CR7 1N4148
R13 3.48K, 1%
U4C CD4053
R22 1K
R23 22K
C3 15
.01
R34
R35 10K FREQ MTR CAL
R37 24.9K
R38
R39 10K MOD MTR CAL
R40 14.7K 1%
CR13 1N4148
CR14 1N4148
CR11 1N4148
CR12 1N4148
−5.1V
.17 0.1
C16 68pF
R32 100K OFFSET
+12V
U9 LF356
R31 8.2K
INPUT GAIN
U4B
R26 470
R27 4.99K, 1%
U8 ICL7109
C10 .047
R29 200K, 1%



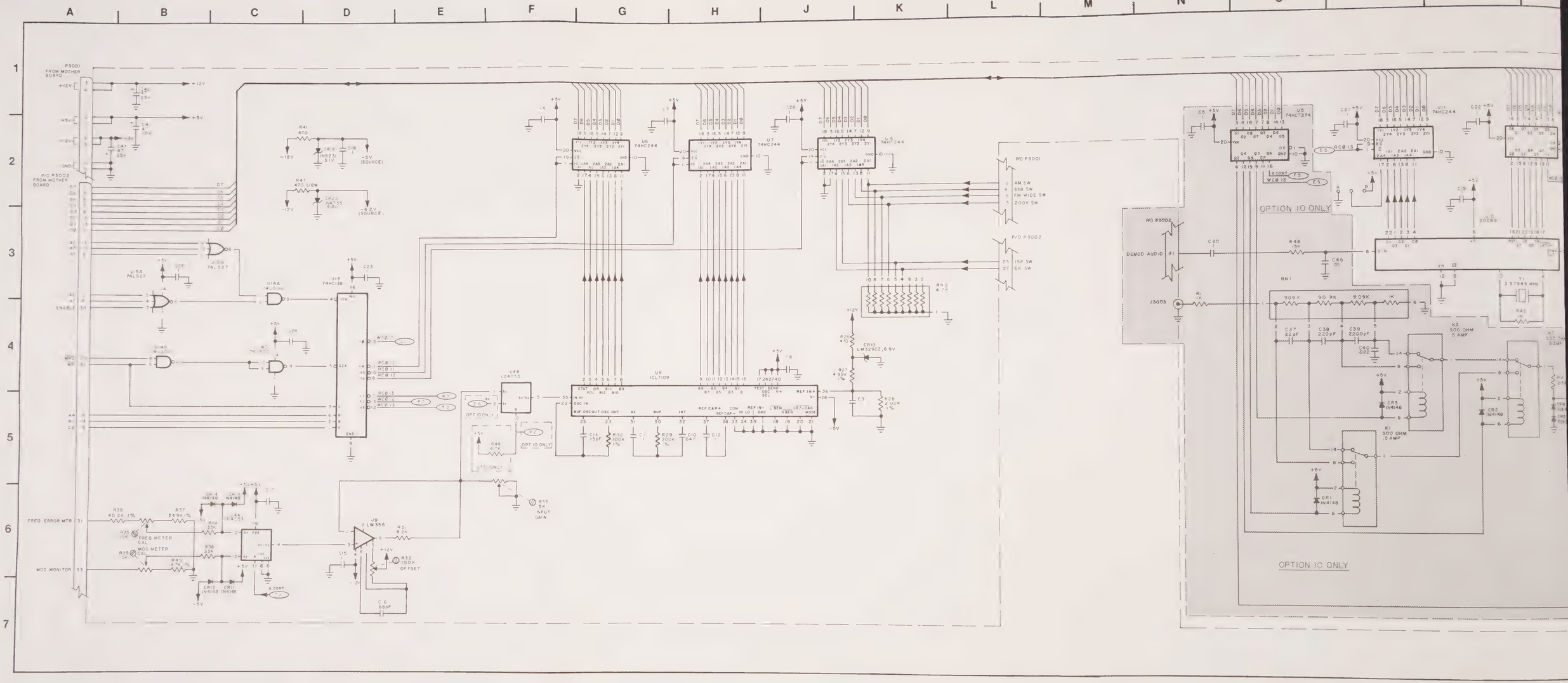
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3000 (I.E., R1 IS R3001).
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4. NOT USED.
5. DEMOD AUDIO IN (PIN 21 OF J3002 AND ASSOCIATED COMPONENTS) NOT CONNECTED IF OPTION 10 NOT INSTALLED.
6. SHADED AREAS DESIGNATE OPTION 10 CIRCUITRY.

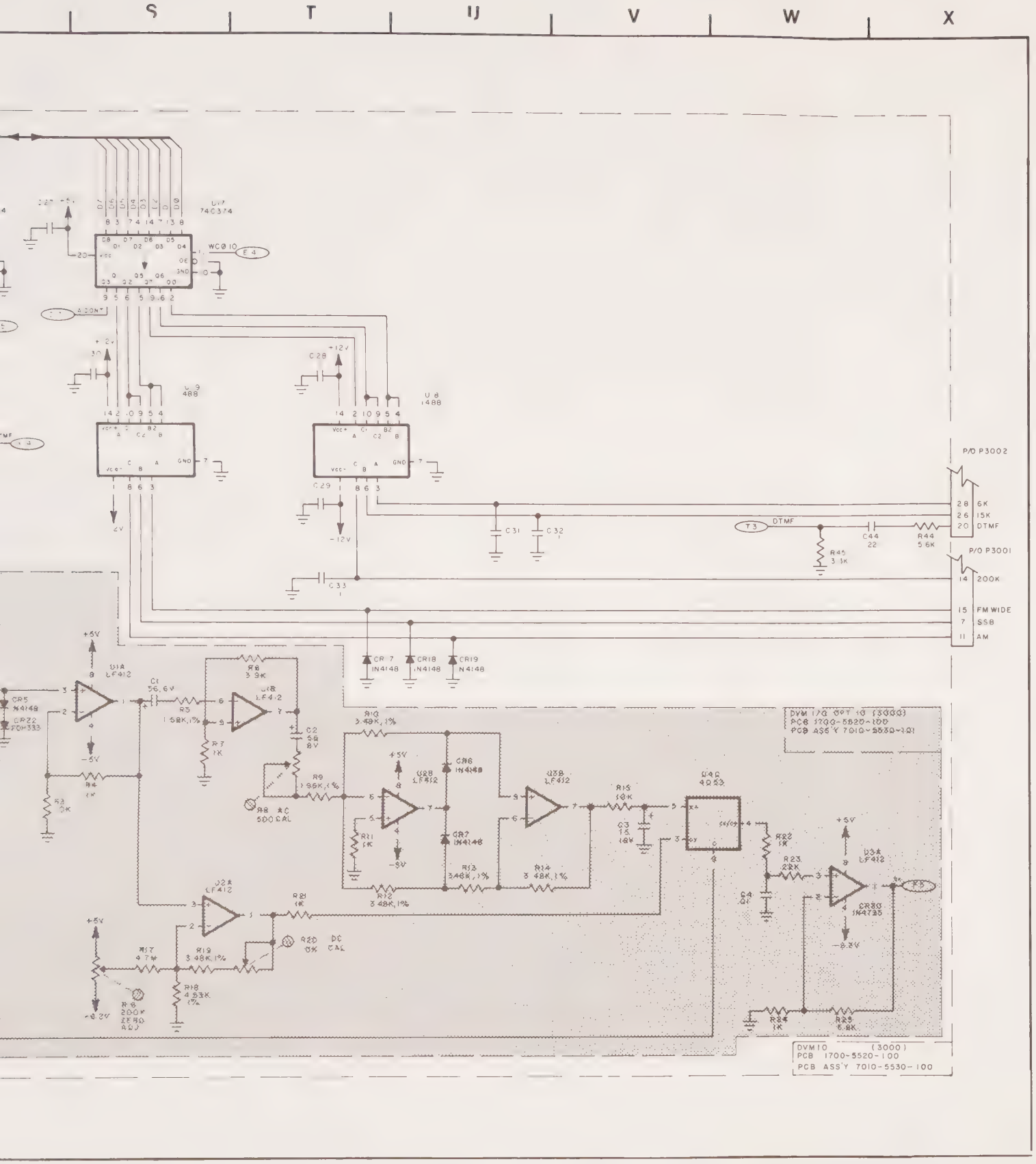


DETAIL **A**
U4B CONNECTION W/O OPTION 10

Figure 6-14 DVM I/O PC Board Assembly (& DVM I/O W/OPTION 10) (Sheet 2 of 3) (0000-5710-500-B)



DVM I/O SCHEMATIC (FM/AM-1200A)
(0000-5510-100-E4)



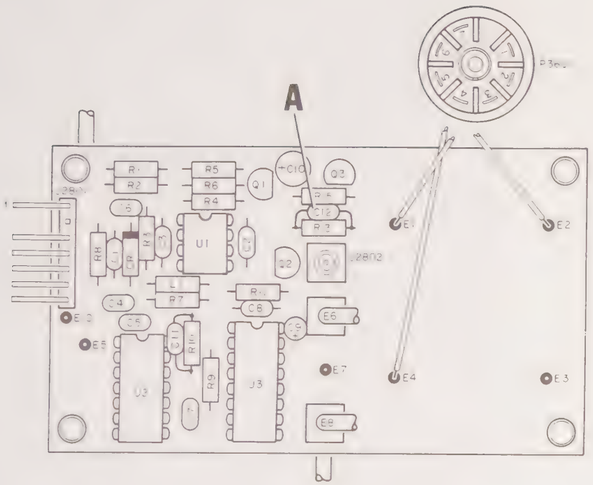
NOTES:

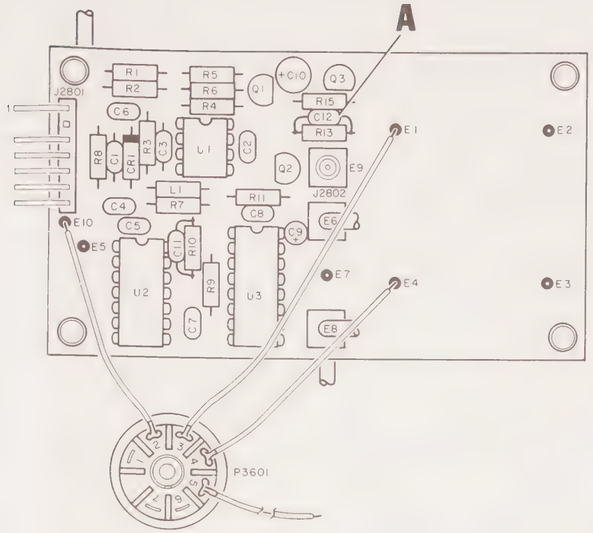
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3000 (I.E., R1 IS R3001).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

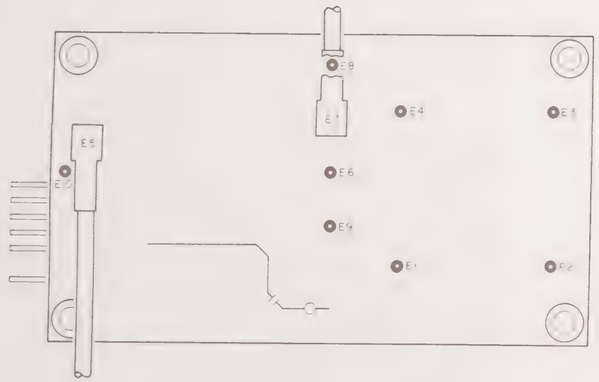
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-14 DVM I/O PC Board Assembly
(& DVM I/O W/OPTION 10)
(Sheet 3 of 3) (0000-5710-500-B)

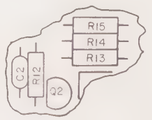




.05 PPM OVEN OSCILLATOR (OPTION 02) - FREQUENCY STANDARD PC BOARD ASSY (7010-5131-703-E5)

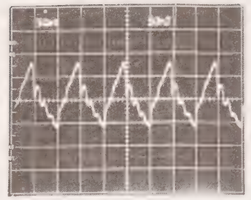


.2 PPM TCXO (STANDARD) - FREQUENCY STANDARD PC BOARD ASSY (7010-5131-702-E5)



DETAIL A

1



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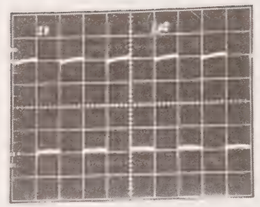
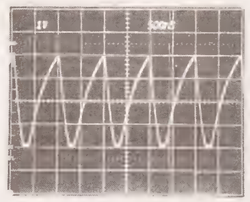


3



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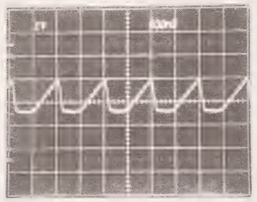
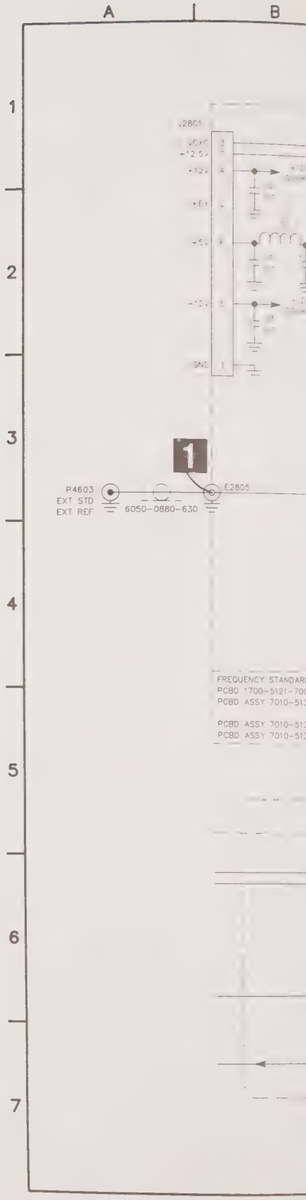
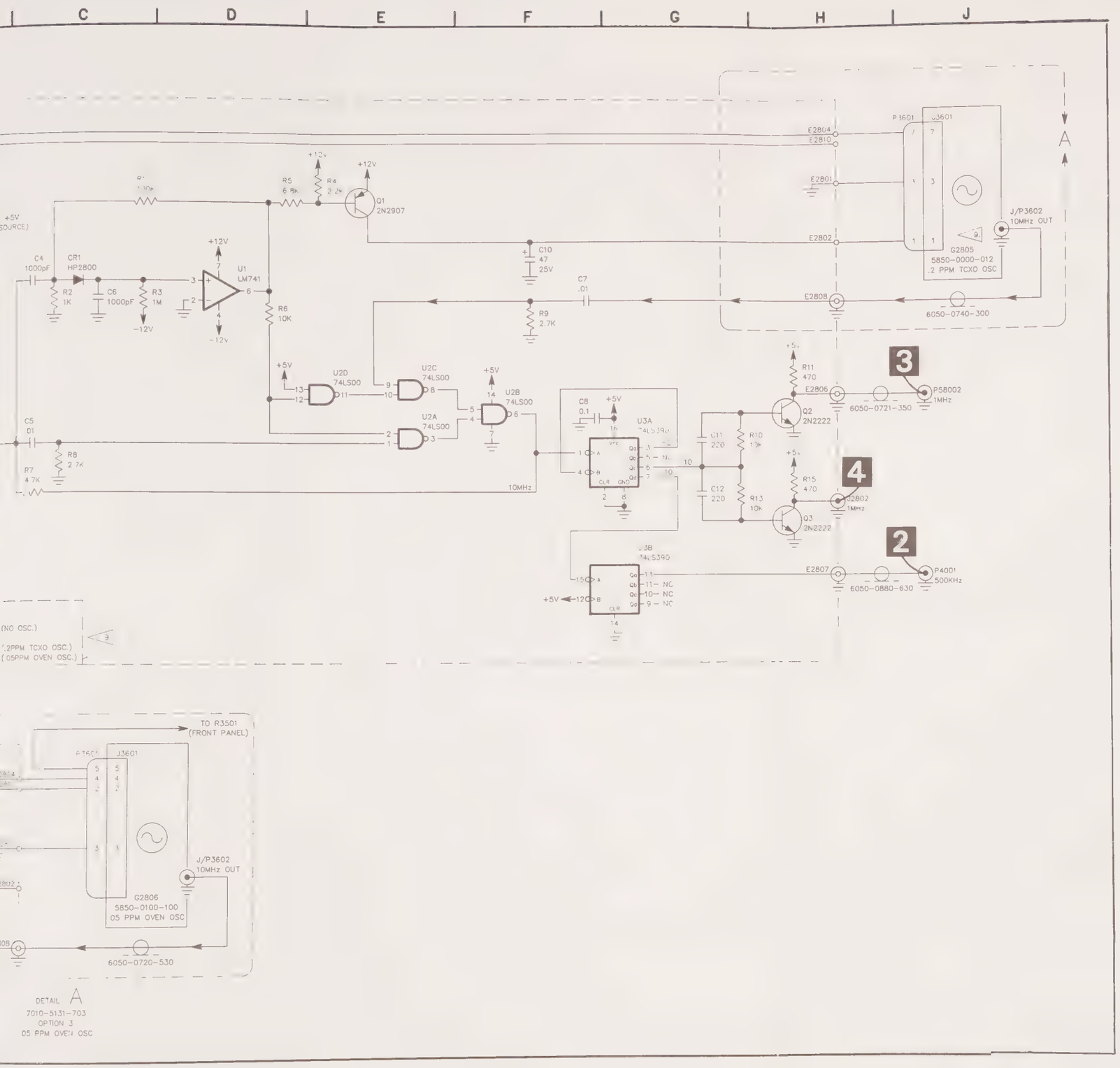


NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X1 PROBE, UNLESS OTHERWISE NOTED.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 2800, 3600 (I.E., R1 IS R2801, R101 IS R3601).

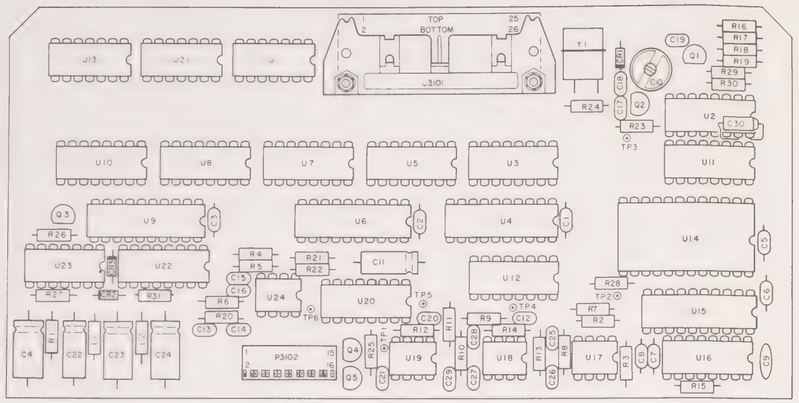
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4. THRU 8. NOT USED.

9. 7010-5131-702 (.2 PPM TCXO) IS STANDARD. 7010-5131-703 (.05 PPM OVEN OSCILLATOR) IS OPTIONAL.

Figure 6-15 Frequency Standard PC Board Assembly (0000-5111-700-E6)

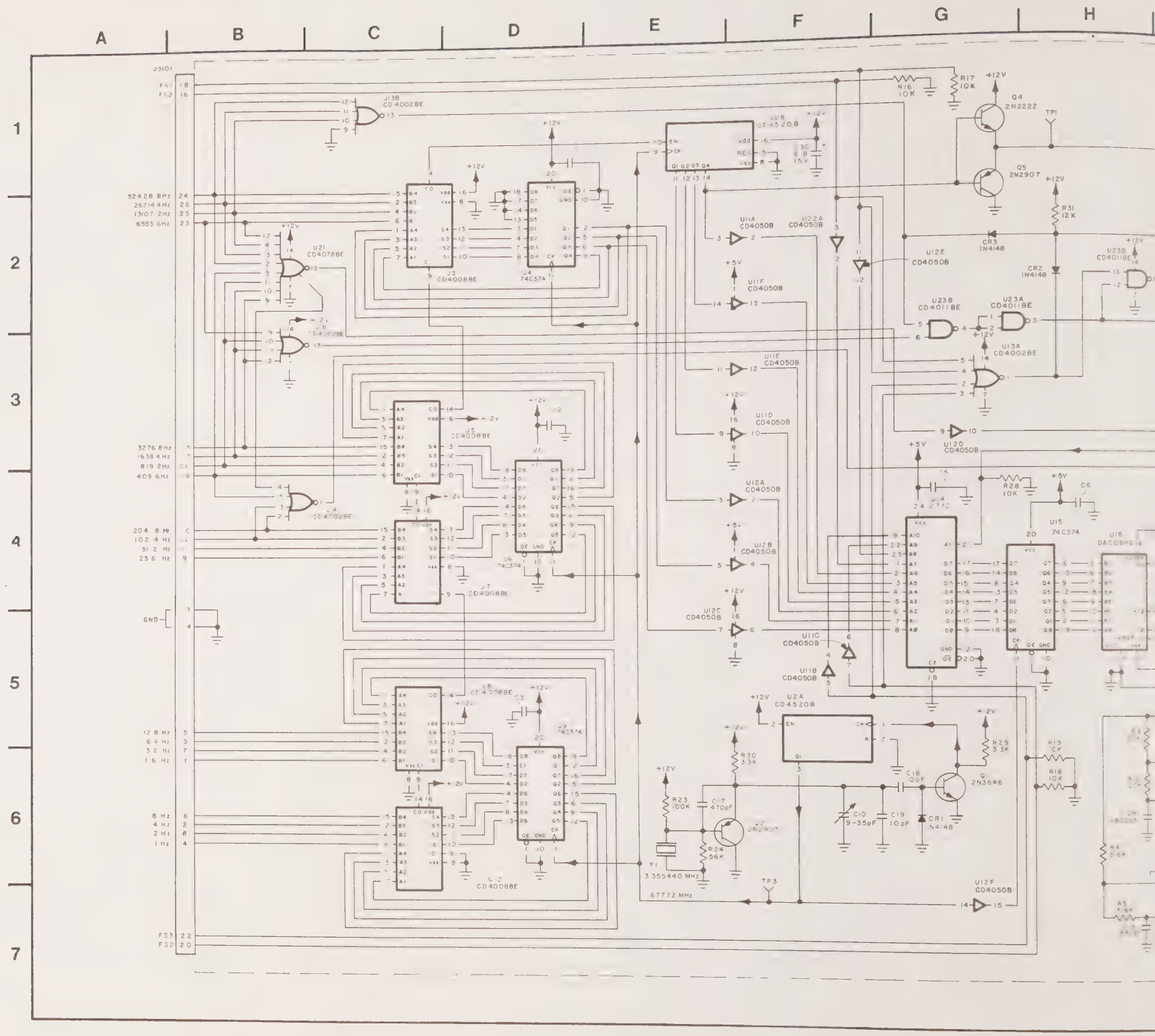


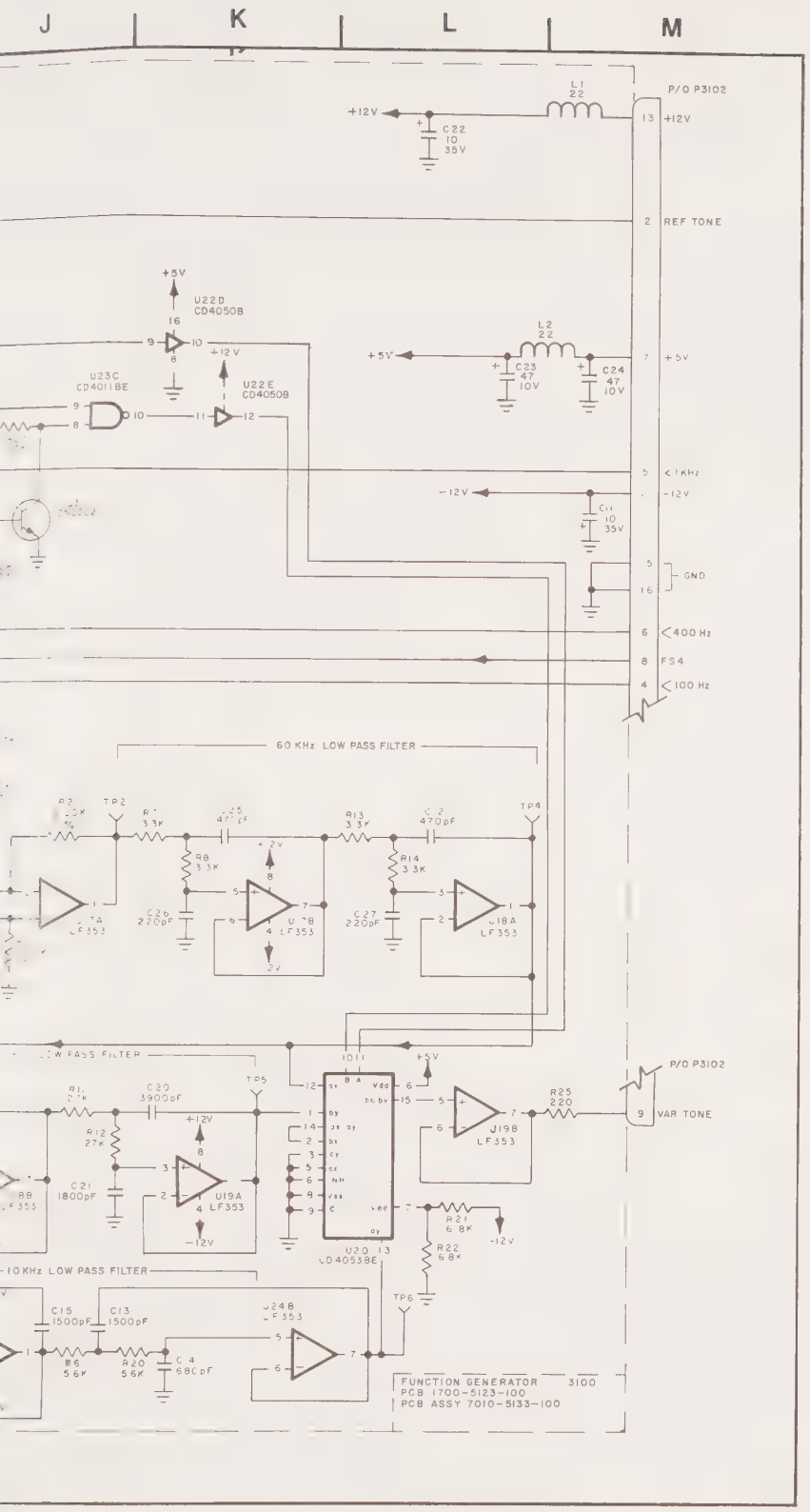
FUNCTION GENERATOR PC BOARD ASSY (7010-5133-100-C5)

P3102 PIN #	IDENTIFIER	REMARKS
4	<100 Hz	HIGH (+12 VDC) WHEN SELECTED TONE IS LESS THAN 102.4 Hz
6	<400 Hz	HIGH (+12 VDC) WHEN SELECTED TONE IS LESS THAN 409.6 Hz
8	< 1 kHz	HIGH (+12 VDC) WHEN SELECTED TONE IS LESS THAN 819.2 Hz

FUNCTION SELECT CONTROL LINES					
FUNCTION	A	B	C	D	E
SINE	0	0	0	0	0
SQUARE	1	0	0	0	0
RAMP	0	1	0	0	0
TRIANGLE	1	1	0	0	0
PULSE	0	0	0	0	0
DCS	0	0	0	1	1

FUNCTION SELECTED	FILTER USED
SINEWAVE AND DCS	
<819.2 Hz	1 kHz
819.2 THRU 13107.2 Hz	10 kHz
≥13107.2 Hz	60 kHz
SQUARE, RAMP, AND TRIANGLE	
<819.2 Hz	10 kHz
≥819.2 Hz	60 kHz
PULSE	10 kHz





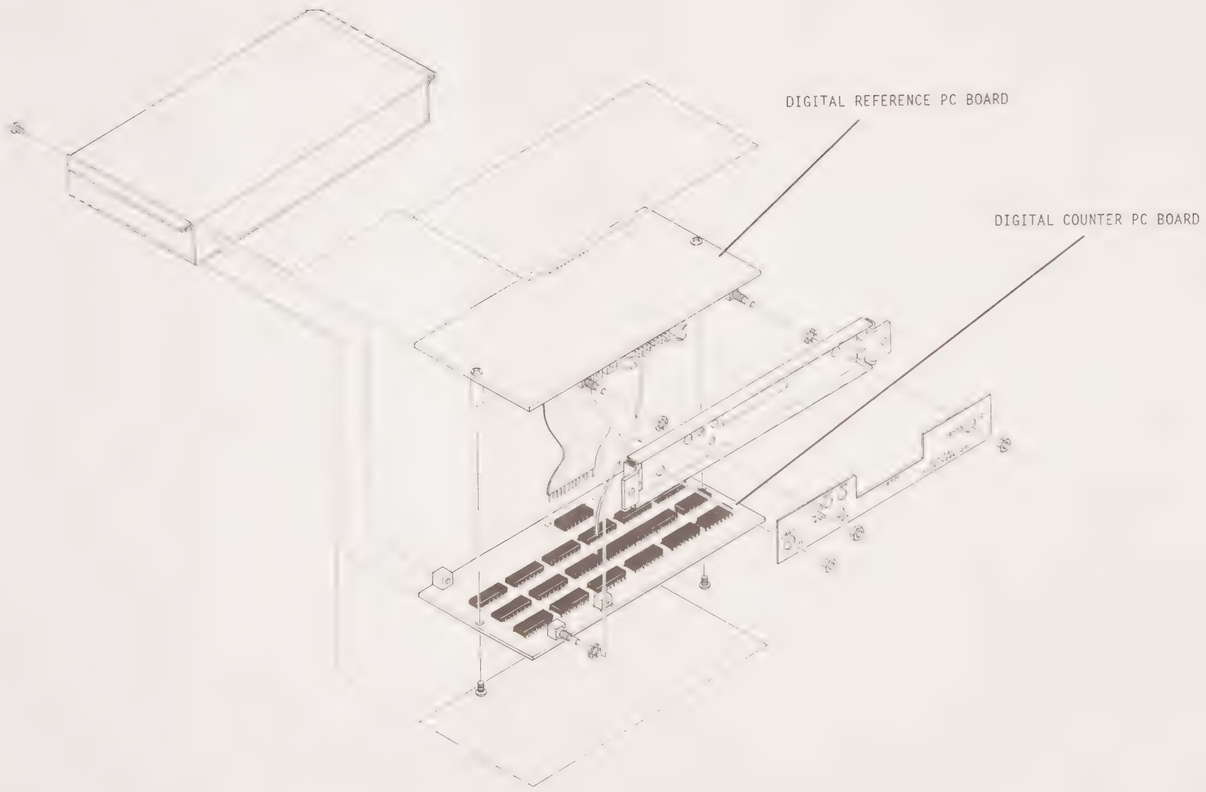
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3100 (I.E., R1 IS R3101).

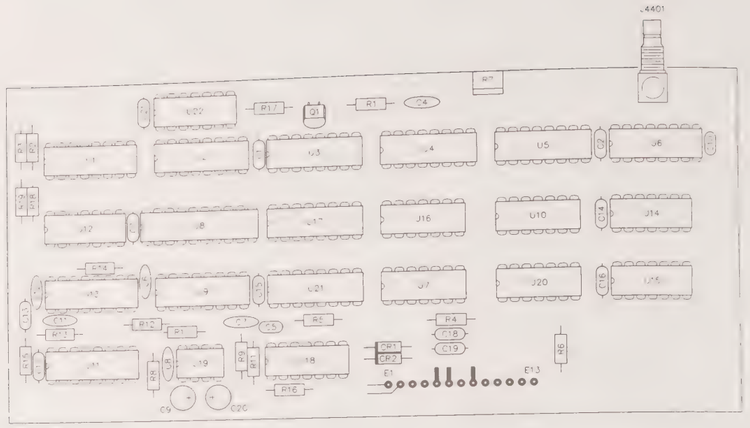
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

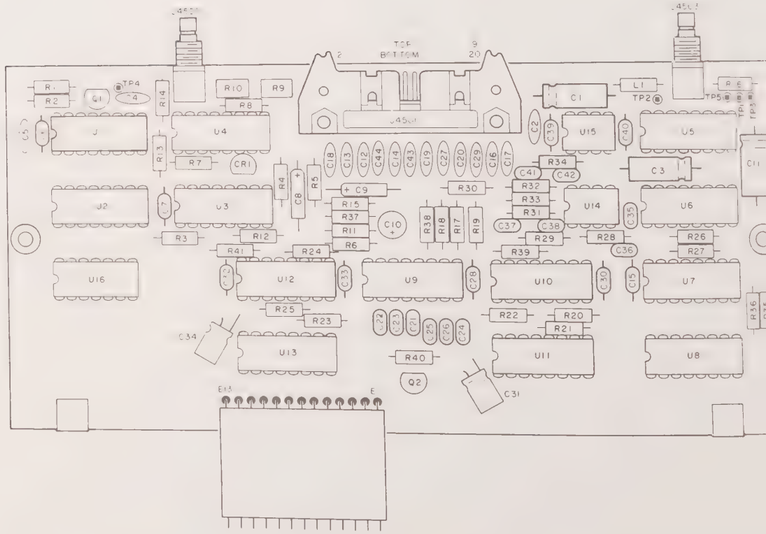
Figure 6-16 Function Generator PC Board Assembly (0000-5113-100-C2)



DIGITAL ASSEMBLY (7005-5244-401)



DIGITAL COUNTER PC BOARD ASSY (7010-523-401-A)

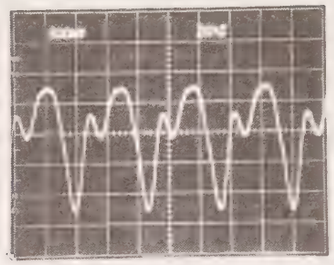


DIGITAL REFERENCE PC BOARD ASSY (7010-5234-500-F7)

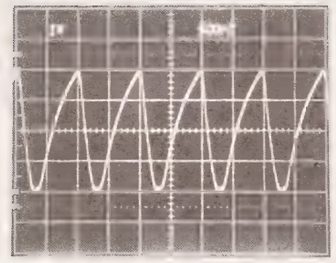
FREQ ERROR SELECT CODING										
J4501		S3702 FREQ ERROR METER RANGE POSITION								
		RF						AUDIO		
PIN #	IDENTIFIER	30	100	300	1K	3K	10K	3	30	300
1	$\overline{X3}$/X10	0	1	0	1	0	1	0	0	0
11	AUDIO/$\overline{RF}$	0	0	0	0	0	0	1	1	1
19	XTB	0	0	1	1	0	0	1	0	1
20	YTB	0	0	0	0	1	1	0	1	1
TIME BASE		10 Hz		100 Hz		1 kHz		100 Hz	1 kHz	10 kHz
J4501 PIN #2 (GEN TUNE) IS TYPICALLY +5.0 VDC										

TEST POINTS	RF SETTINGS 30	100	300	1K	3K	10K
TP4401	0	0	1	1	0	0
TP4402	1	1	1	1	1	1
TP4403	0	0	0	0	1	1
TP4404	1	1	1	1	0	0
TP4405	1	1	0	0	0	0
TP4406	1	1	0	0	1	1
TP4407	0	0	1	1	1	1

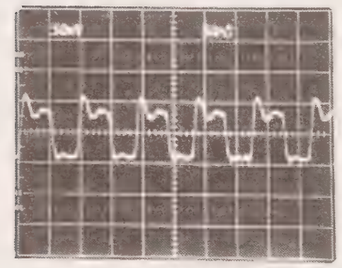
1



2

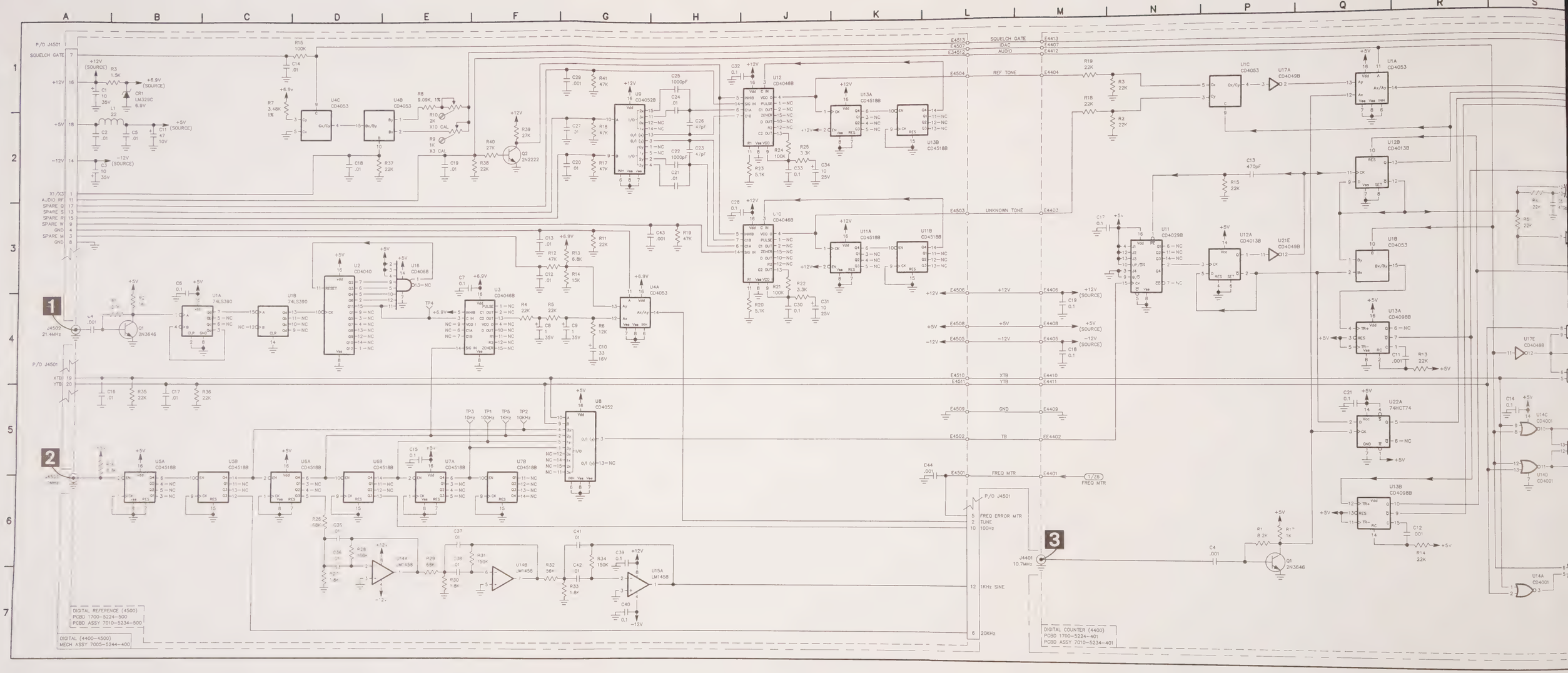


3



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X1 PROBE.

Figure 6-17 Digital PC Board Assembly (Sheet 1 of 2) (0000-5214-401-A/0000-5214-500-F)



DIGITAL REFERENCE (4500)
PCBD 1700-5224-500
PCBD ASSY 7010-5234-500
DIGITAL (4400-4500)
MECH ASSY 7005-5244-400
DIGITAL COUNTER (4400)
PCBD 1700-5224-401
PCBD ASSY 7010-5234-401
SQUELCH GATE
IDAC
AUDIO
REF TONE
UNKNOWN TONE
XTB
YTB
GND
TB
FREQ MTR
FREQ ERROR MTR
TUNE
100Hz
1KHz SINE
20KHz

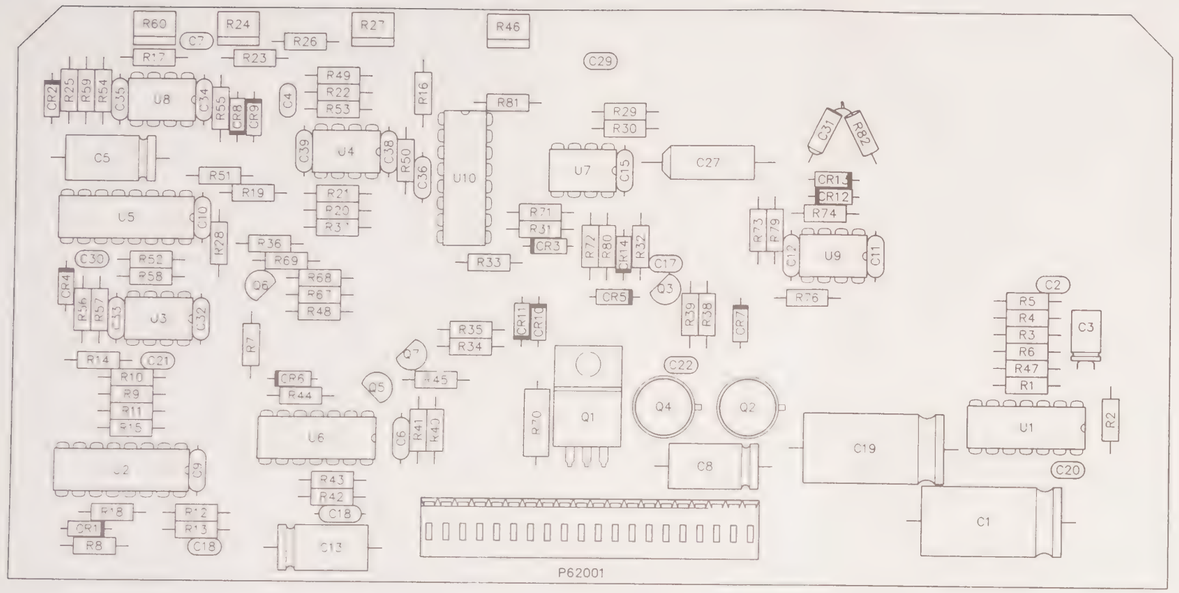
NOTES:

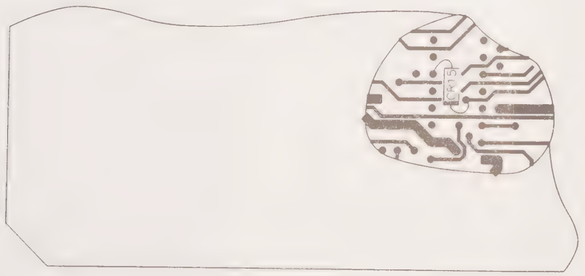
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 4500 (I.E., R1 IS R4501).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

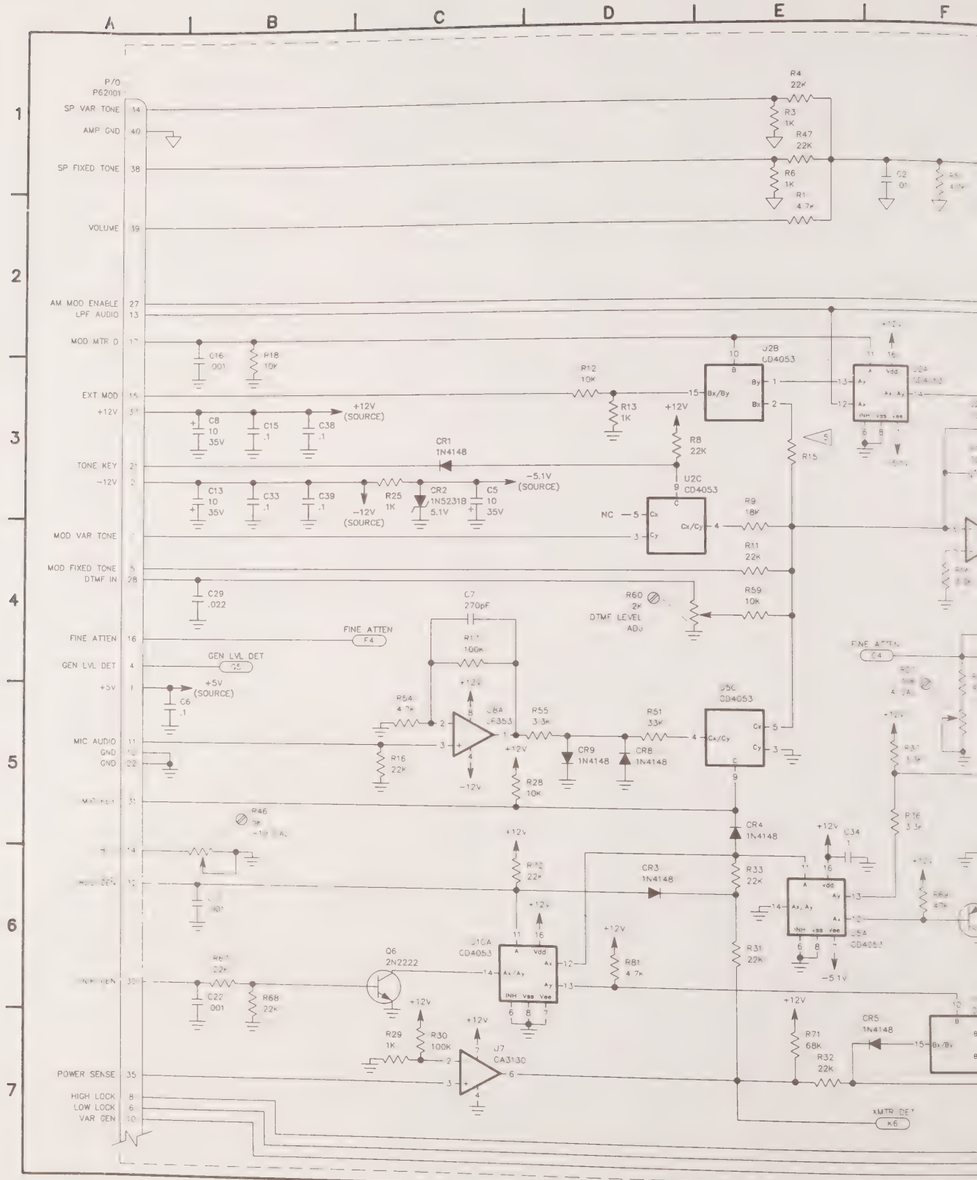
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

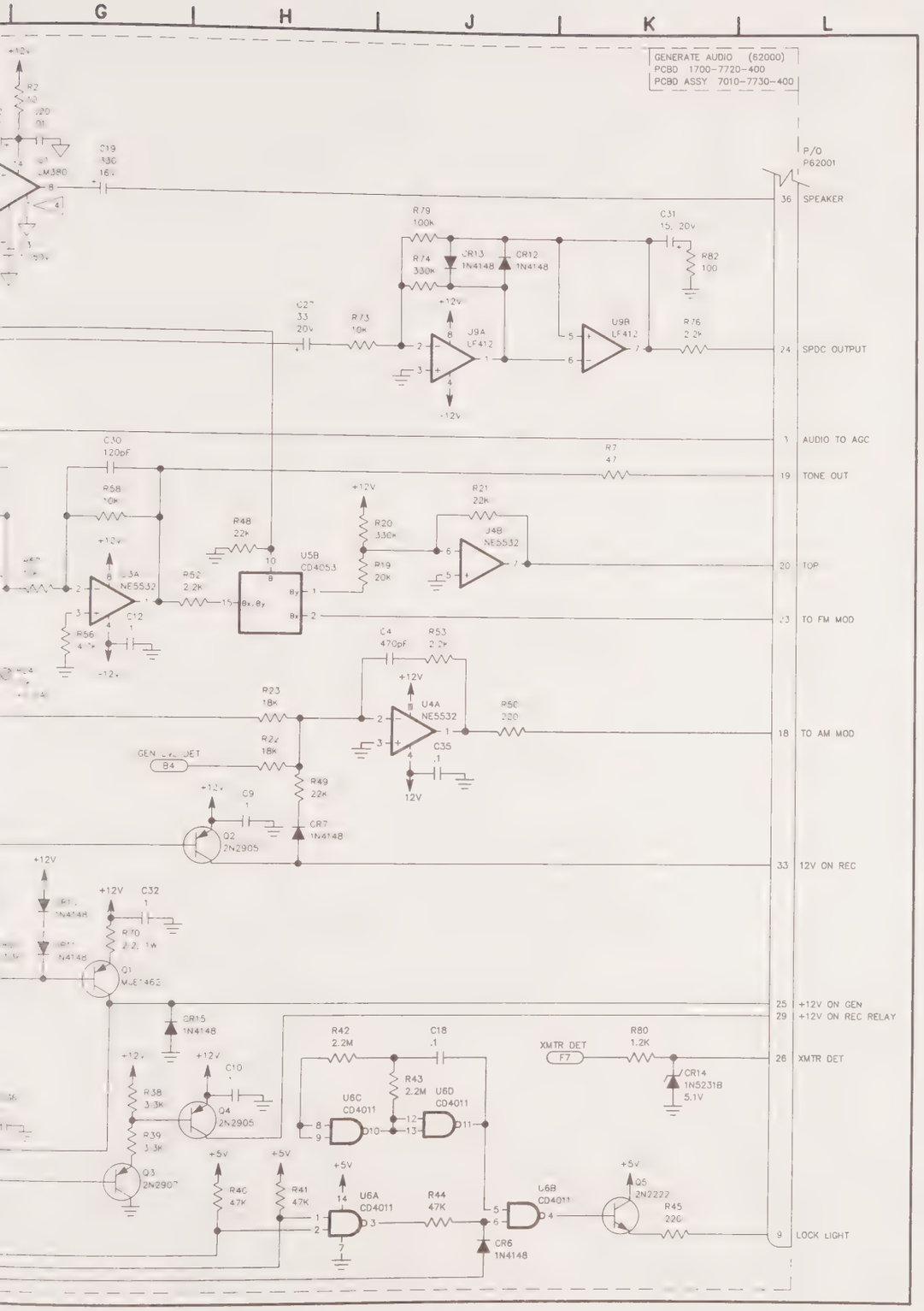
Figure 6-17 Digital PC Board Assembly (Sheet 2 of 2)
(0000-5214-401-A)0000-5214-500-F)





GENERATE AUDIO PC BOARD ASSY (FM/AM-1200S)
(7010-7730-400-B3)





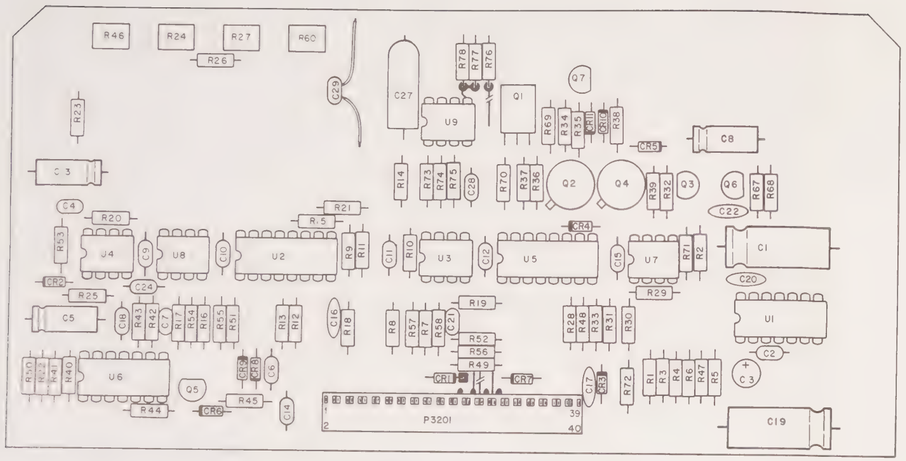
NOTES:

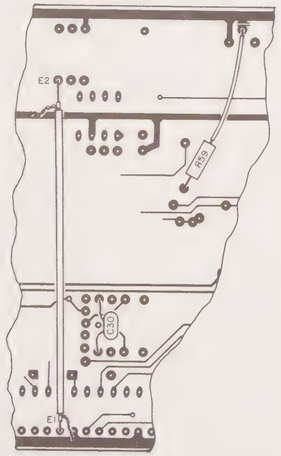
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 62000 (I.E., R1 IS R62001).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

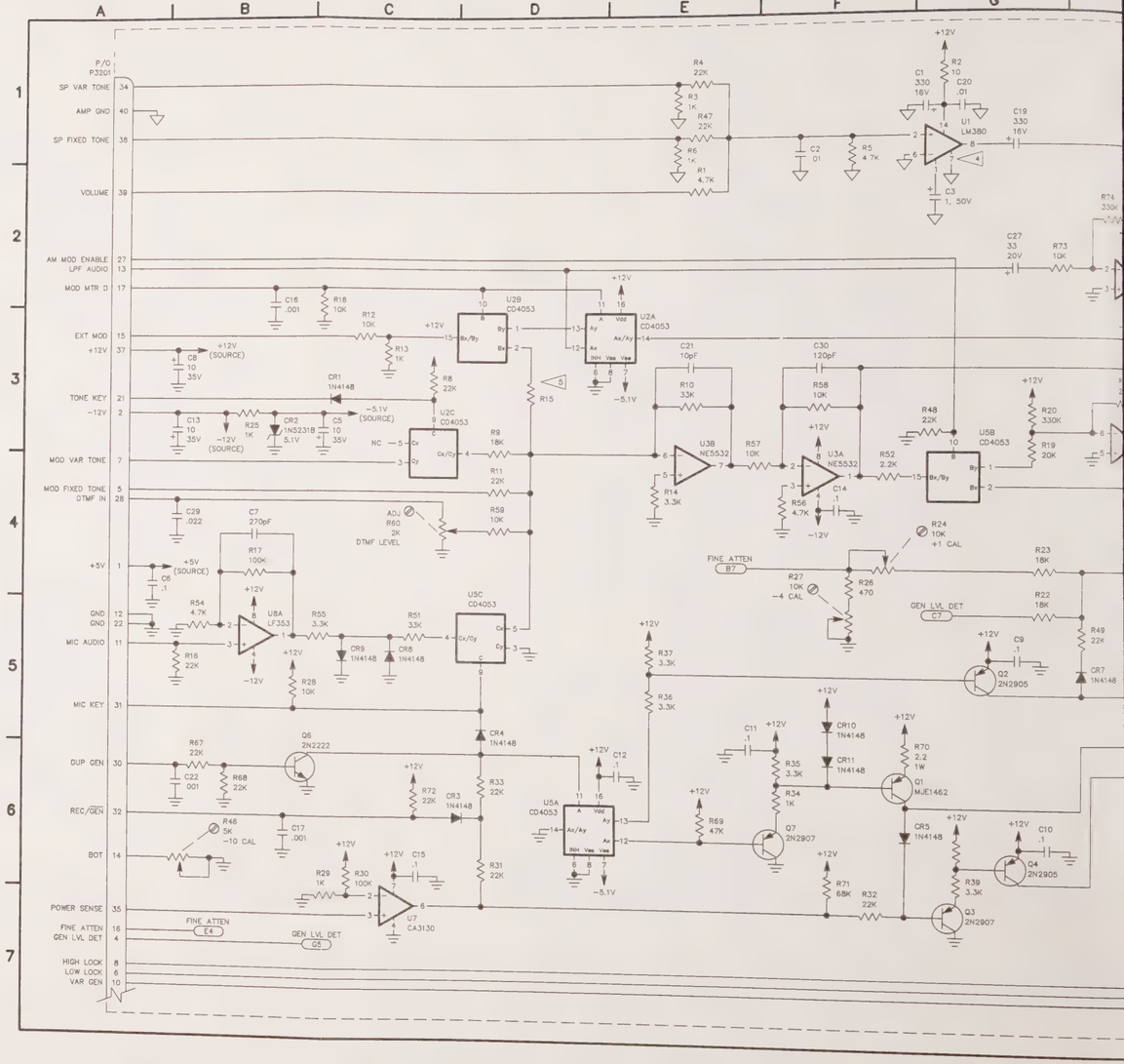
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

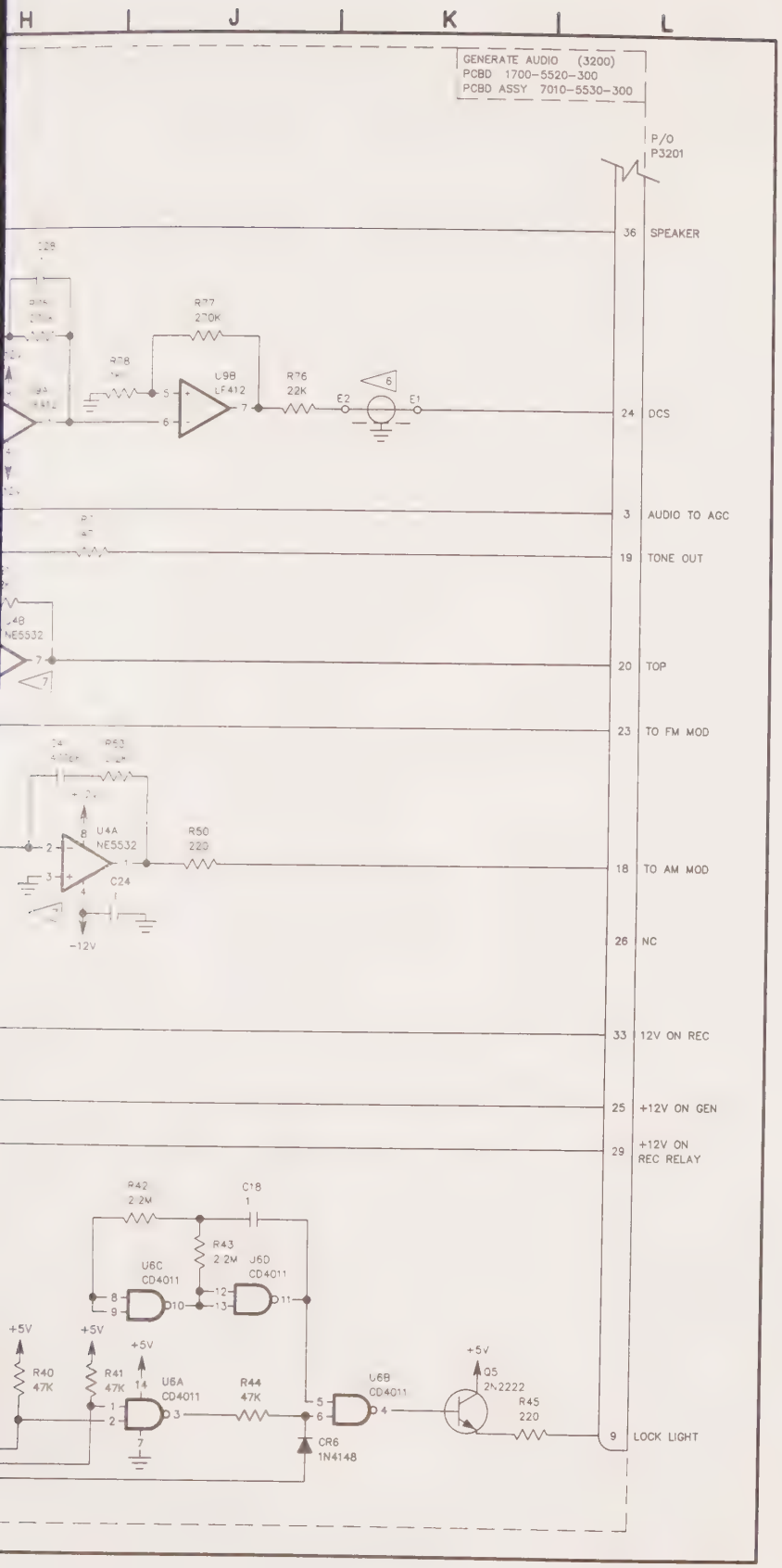
Figure 6-18 Generate Audio PC Board Assembly (FM/AM-1200S) (0000-7710-400-B3)





GENERATE AUDIO PC BOARD ASSY (FM/AM-1200A)
(7010-5530-300-B2)





NOTES:

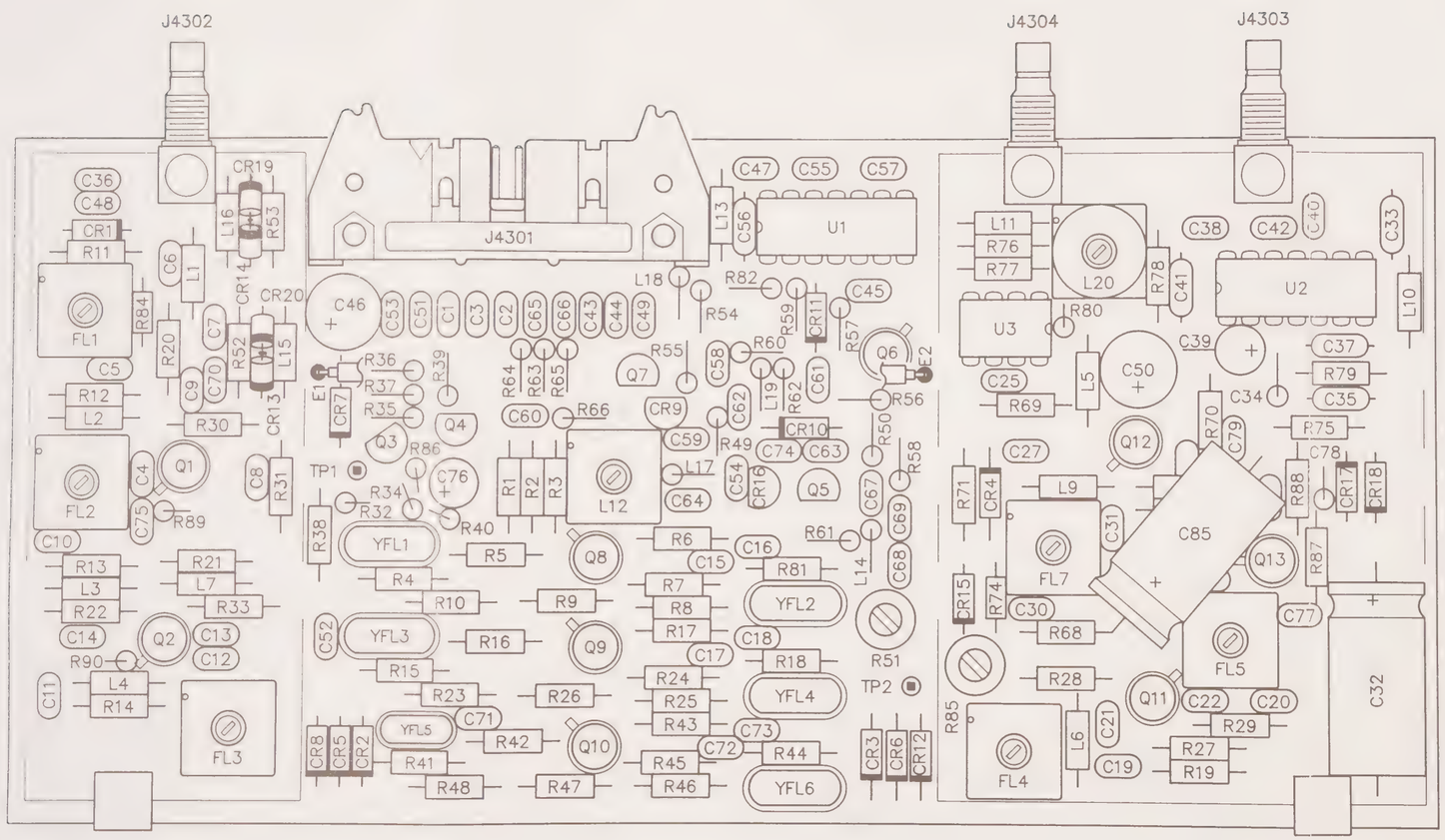
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3200 (I.E., R1 IS R3201).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

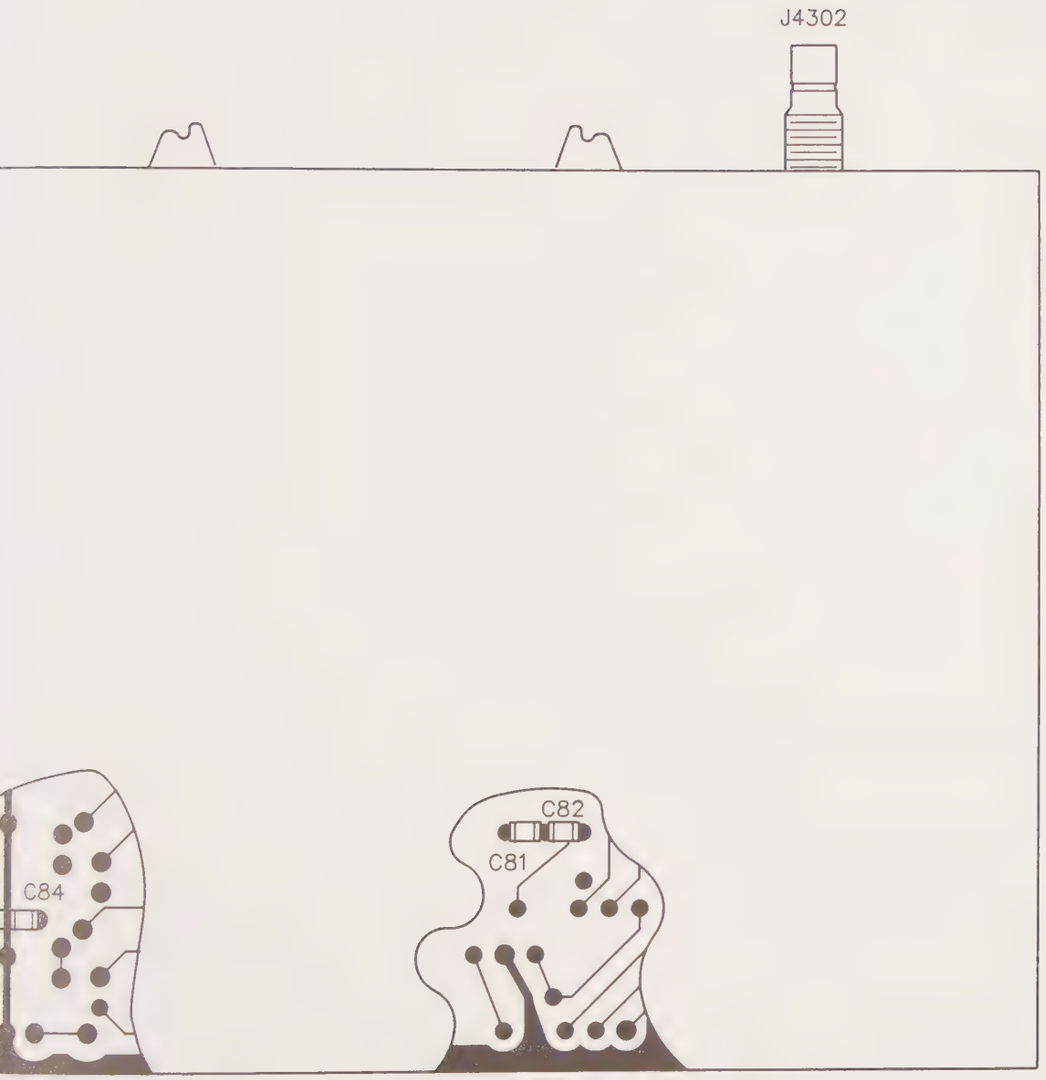
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS. UNLESS OTHERWISE SPECIFIED.

P3201		REMARKS
PIN	IDENTIFIER	
4	GEN LVL DET	POSITIVE D.C. VOLTAGE PROPORTIONAL TO R.F. DETECTED IN THE OUTPUT AMP
6	LOW LOCK	+5 VDC WHEN LOW LOOP IS PHASE LOCKED
8	HIGH LOCK	+5 VDC WHEN HIGH LOOP IS PHASE LOCKED
17	MOD MTR D	+12 VDC WHEN MODULATION METER CONTROL IS IN DIST OR SINAD
21	TONE KEY	GROUND ON THIS LINE, WHEN IN GEN MODE, DISABLES FUNCTION GENERATOR OUTPUT
27	AM	+12 VDC WHEN MODULATION SELECT CONTROL IS IN AM NORM, AM NAR, AND SSB
31	MIKE KEY	GROUND WHEN MICROPHONE PTT SWITCH IS DEPRESSED
35	POWER SENSE	POSITIVE DC VOLTAGE PROPORTIONAL TO THE STRENGTH OF ANY RF RECEIVED AT THE T/R CONN

Figure 6-19 Generate Audio PC Board Assembly (FM/am-1200A) (0000-5510-300-B2)



10.7 MHz GEN/REC PC BOARD ASSY (FM/AM-1200S)
(7010-5730-700-B1)



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 4300 (I.E., R1 IS R4301).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

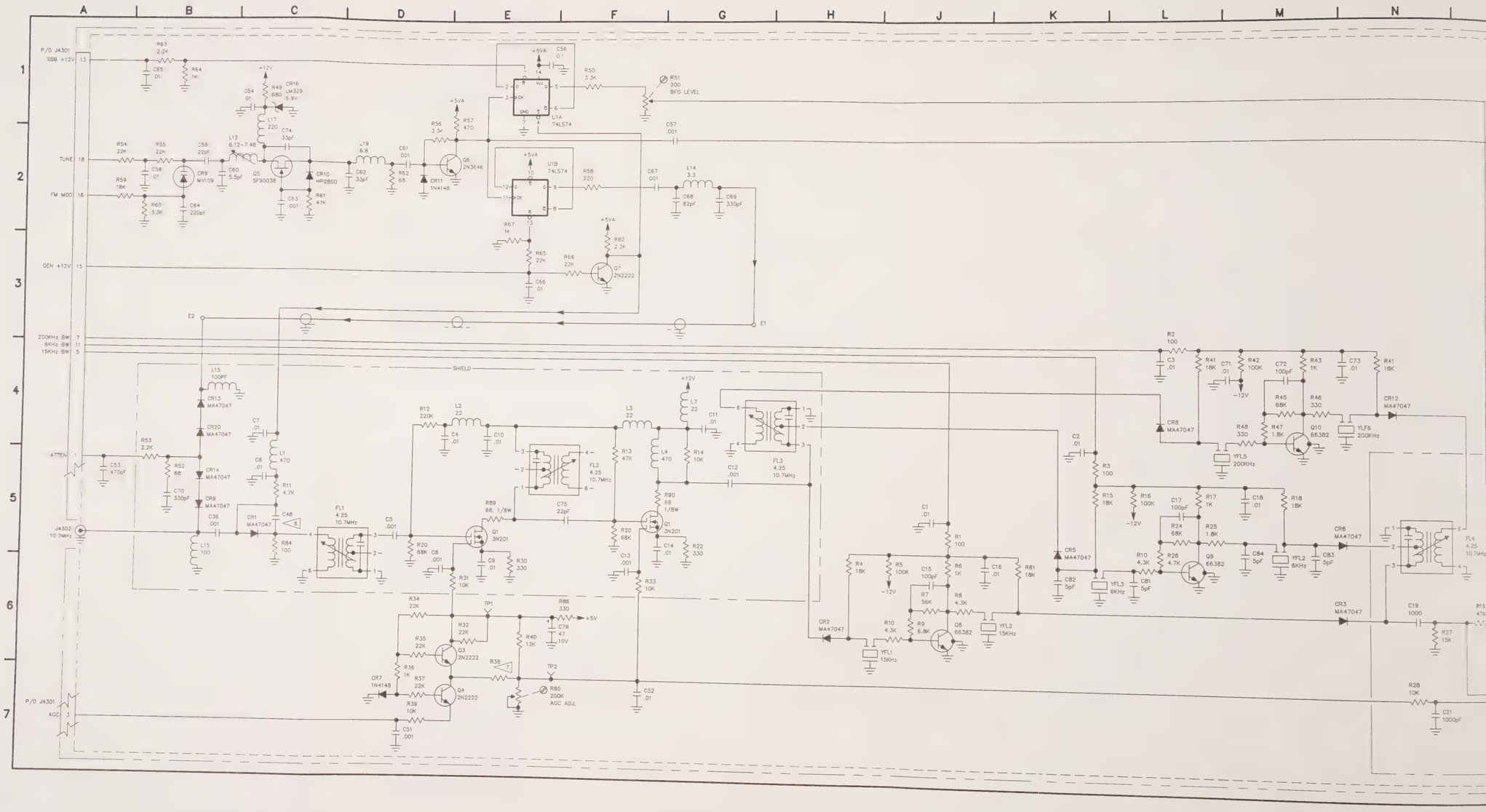
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4, 5. NOT USED

6. C4348 IS SELECTED AT TEST (S.A.T.):
RANGE: 10pF TO 100pF
NOMINAL: 100 pF

7. R4338 IS SELECTED AT TEST (S.A.T.):
RANGE: 4.7KΩ TO 15KΩ
NOMINAL: 6.8KΩ

Figure 6-20 10.7 MHz GEN/REC PC Board Assembly (FM/AM-1200S) (Sheet 1 of 2) (0000-5730-700-A1)


A
B
C
D
E
F
G
H
J
K
L
M
N
1
2
3
4
5
6
7
P/O J4301
SSB +12V 13
TUNE 18
FM MOD 16
GEN +12V 15
200KHz BW 7
6KHz BW 11
15KHz BW 5
ATTEN 1
J4302
10.7MHz
P/O J4301
AGC 3
+12V
+5VA
-12V
SHIELD
E1
E2
R63 2.2K
C65 .01
R64 1K
CR16 LM329 6.9V
C54 .01
R49 680
L17 220
C74 33pF
L12 6.12-7.48
R54 22K
R55 22K
C59 22pF
C58 .01
CR9 MV109
C60 5.5pF
Q5 SF90038
CR10 HP2800
C63 .001
R61 47K
C62 33pF
L19 6.8
C61 .001
R62 68
CR11 1N4148
R56 3.3K
R57 470
Q6 2N3646
R59 18K
R60 3.3K
C64 220pF
C56 .1
U1A 74LS574
R50 3.3K
R51 200 BFO LEVEL
C57 .001
U1B 74LS574
R58 220
C67 .001
L14 3.3
C68 82pF
C69 330pF
R67 1K
R65 22K
C66 .01
R66 22K
Q7 2N2222
R82 2.2K
R53 2.2K
C53 470pF
R52 68
C70 330pF
L15 100PF
CR13 MA47046
CR20 MA47046
CR14 MA47046
CR9 MA47046
C36 .001
L15 100
C7 .01
C8 .01
L1 470
R11 4.7K
CR1 MA47046
C48 6
R84 100
FL1 4.25 10.7MHz
R12 220K
L2 22
C4 .01
C10 .01
C5 .001
R20 68K
C8 .001
R89 68, 1/8W
Q1 3N201
C9 .01
R30 330
R31 10K
FL2 4.25 10.7MHz
C75 22PF
L3 22
R13 47K
L4 470
R14 10K
L7 22
C11 .01
C12 .001
FL3 4.25 10.7MHz
R90 68 1/8W
Q1 3N201
C14 .01
R22 330
C13 .001
R33 10K
R34 22K
TP1
R32 22K
R86 330
C78 47 10V
R35 22K
Q3 2N2222
R40 12K
R36 1K
R37 22K
Q4 2N2222
R38
TP2
CR7 1N4148
R39 10K
C51 .001
R85 200K AGC ADJ.
C52 .01
C1 .01
R1 100
R4 18K
R5 100K
C15 100pF
R6 1K
C16 .01
R81 18K
R7 56K
R8 4.3K
R10 4.3K
R9 6.8K
Q8 66382
YFL2 15KHz
YFL1 15KHz
CR2 MA47046
R2 100
C3 .01
R41 18K
C71 .01
R42 100K
C72 100pF
R43 1K
C73 .01
R41 18K
CR12 MA47046
CR8 MA47046
R45 68K
R46 330
R47 1.8K
Q10 66382
YLF6 200KHz
R48 330
YFL5 200KHz
C2 .01
R3 100
R15 18K
R16 100K
C17 100pF
R17 1K
C18 .01
R18 18K
CR5 MA47046
R24 68K
R25 1.8K
R10 4.3K
R26 4.7K
Q9 66382
C84 5pF
YFL2 6KHz
C83 5pF
C82 5pF
YFL3 6KHz
C81 5pF
CR6 MA47046
FL4 4.25 10.7MHz
CR3 MA47046
C19 1000
R19 47K
R27 15K
R28 10K
C21 1000pF

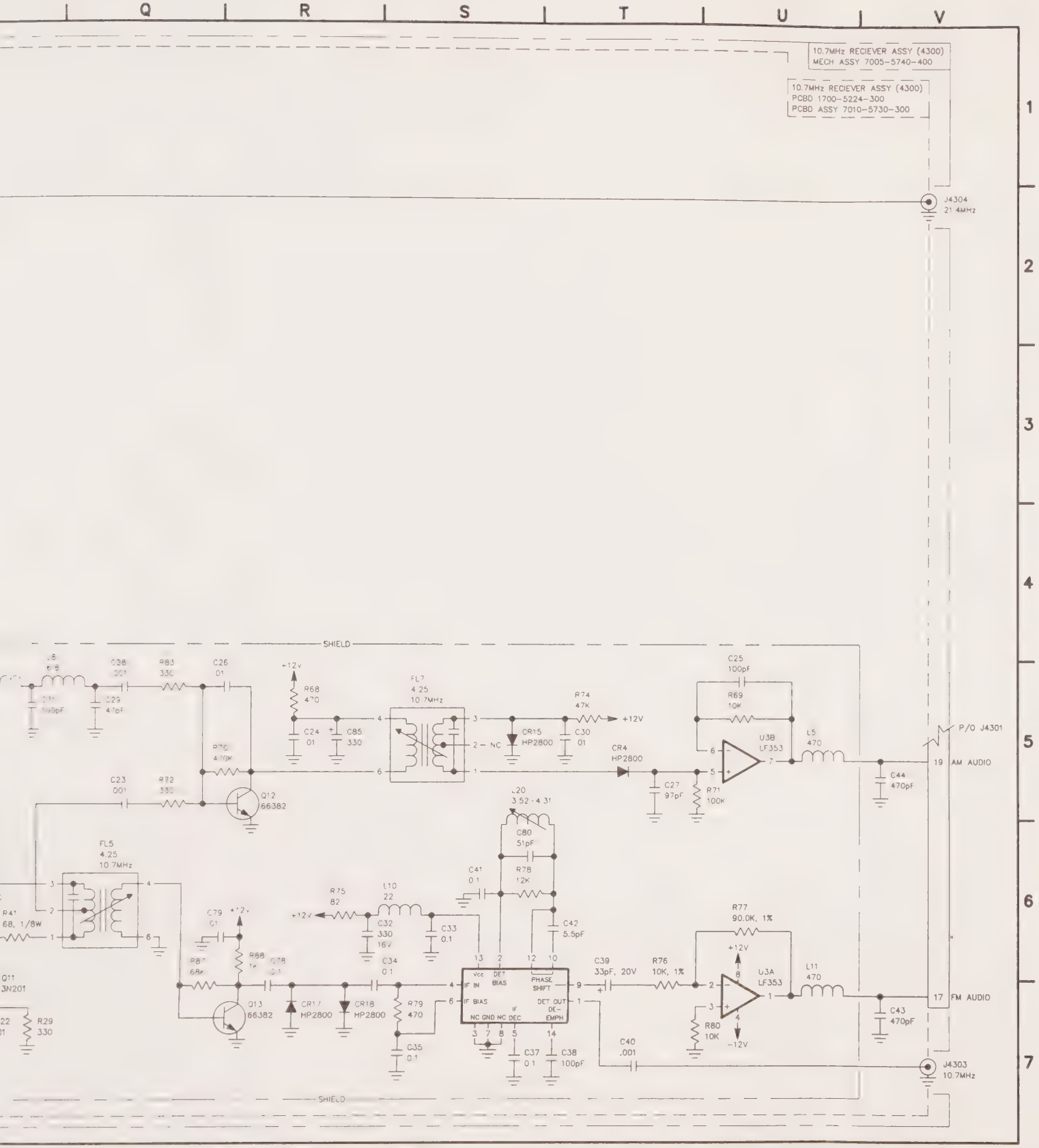
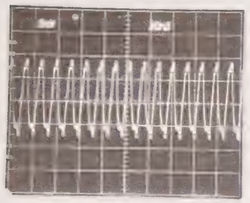


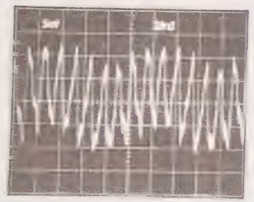
Figure 6-20 10.7 MHz GEN/REC PC Board Assembly (FM/AM-1200S (Sheet 2 of 2) (0000-5730-700-A1)

1



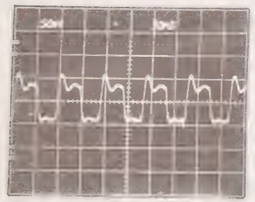
REC MODE:
NO SIGNAL PRESENT

1

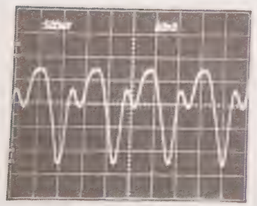


INPUT @ ANTENNA:
150.2 MHz @ -50 dB

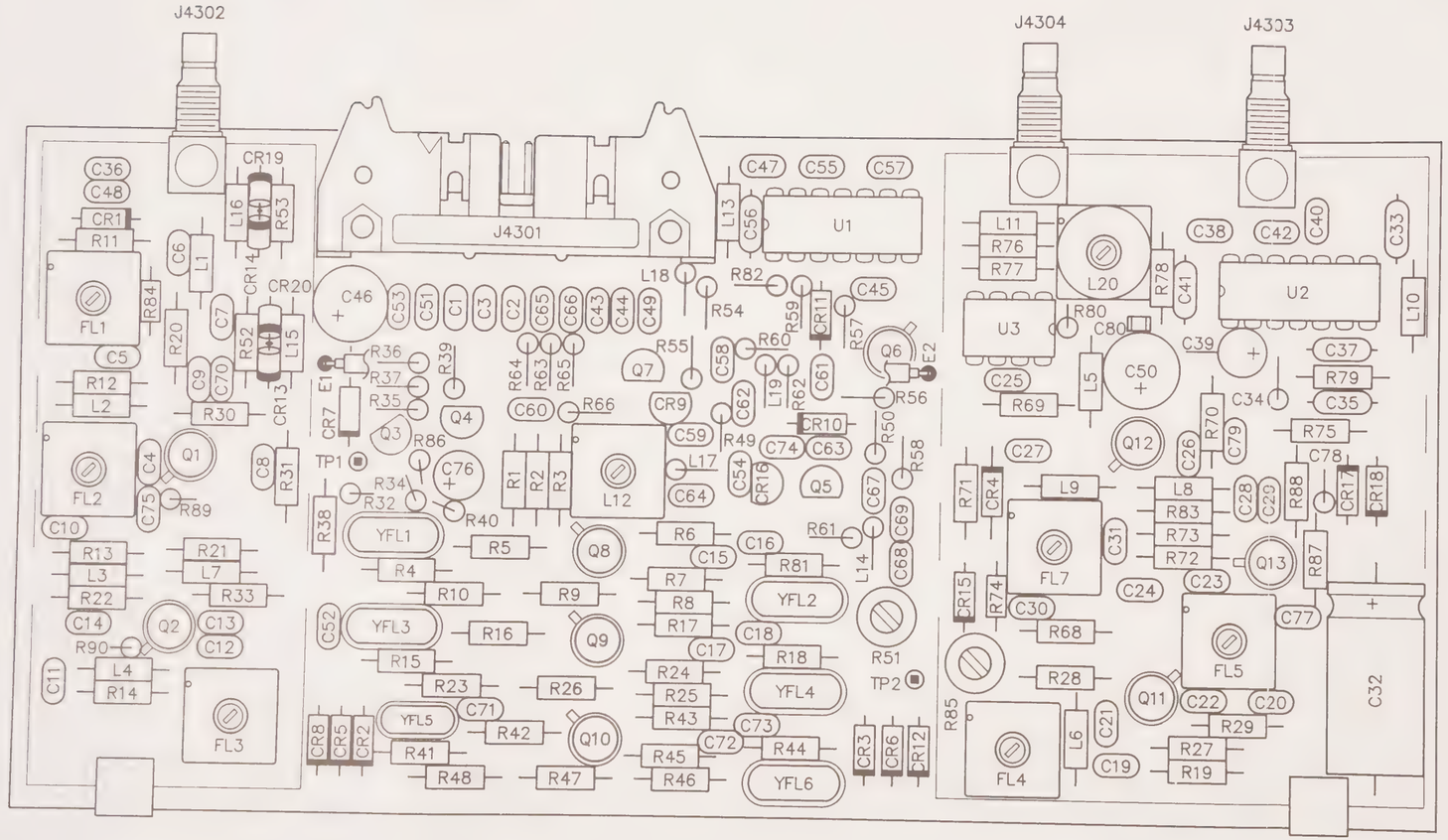
2



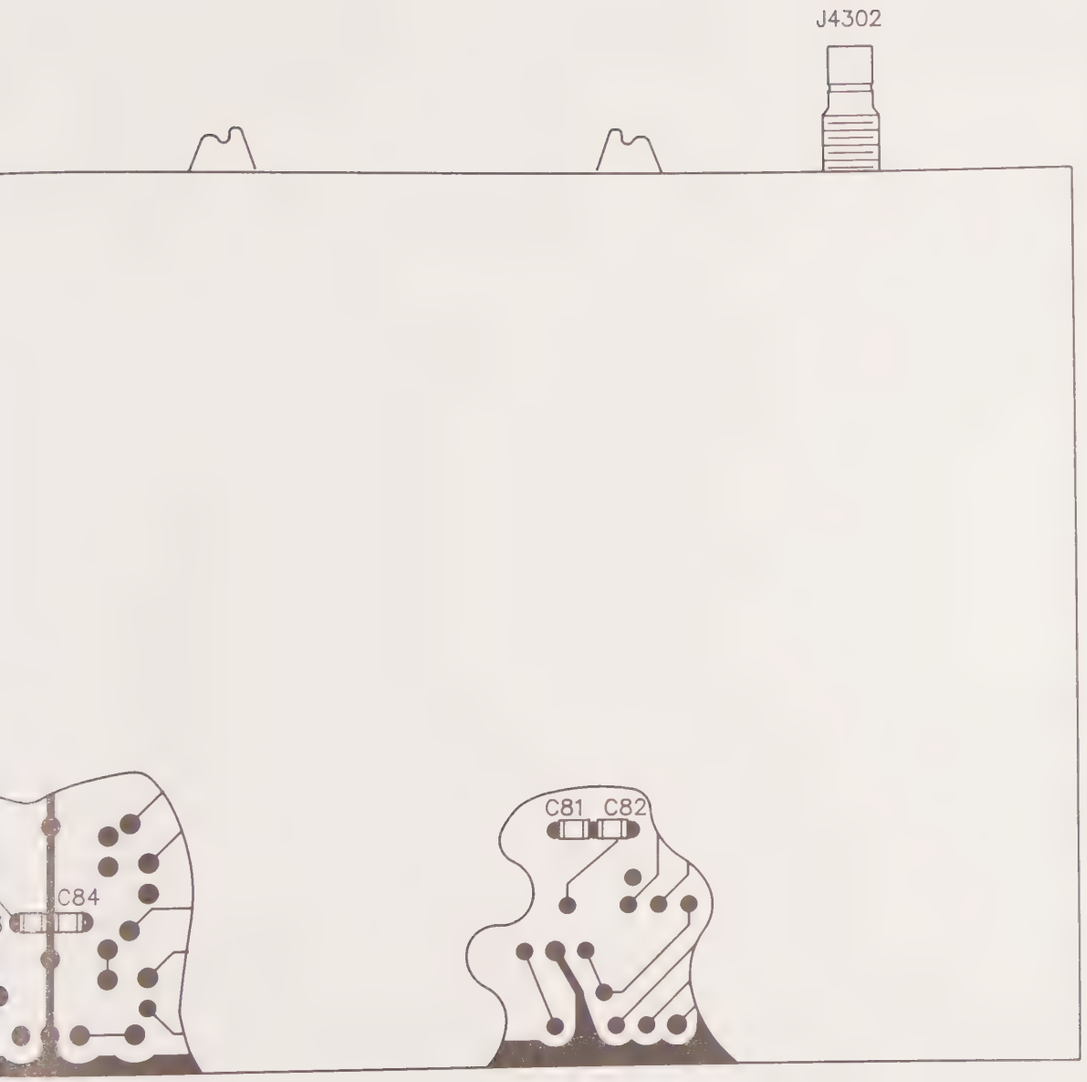
3



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200A SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X1 PROBE.



10.7 MHz GEN/REC PC BOARD ASSY (FM/AM-1200A)
(7010-5234-301-U4)



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 4300 (I.E., R1 is R4301).

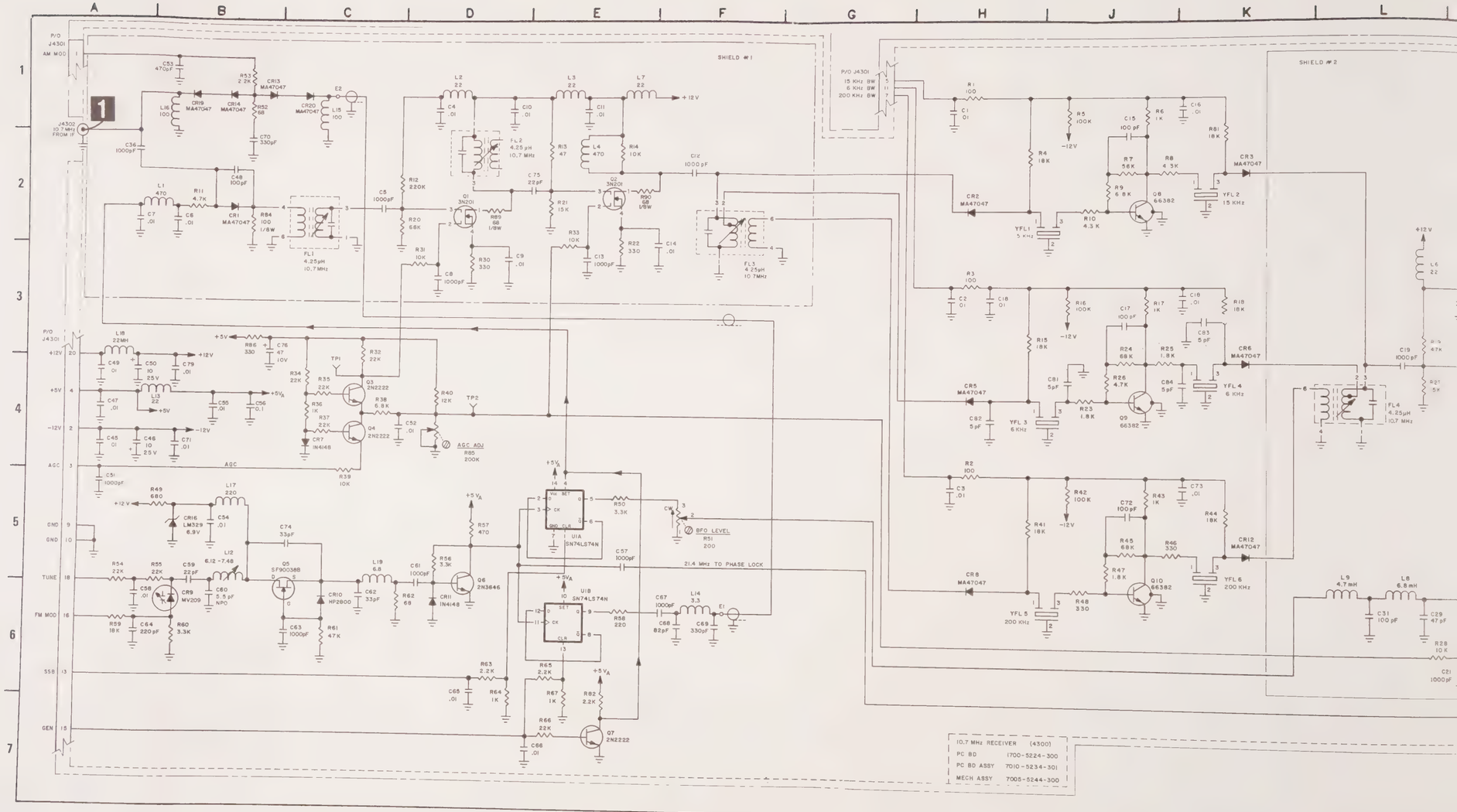
2. ALL RESISTORS ARE 1/4W. 5% TOLERANCE. UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS: ALL CAPACITANCE IS EXPRESSED IN MICROFARADS. AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS. UNLESS OTHERWISE NOTED.

4-11. NOT USED

12. R4338 IS SELECTED AT TEST (S.A.T.)
RANGE: 4.7K to 15K
NOMINAL: 6-8K

Figure 6-21 10.7 MHz GEN/REC PC Board Assembly (FM/AM-1200A) (Sheet 1 of 2) (0000-5214-300-R5)


SHIELD #1
SHIELD #2
P/O J4301 AM MOD
J4302 10.7 MHz FROM IF
P/O J4301 15 KHz BW 6 KHz BW 200 KHz BW
FL1 4.25μH 10.7 MHz
FL2 4.25 μH 10.7 MHz
FL3 4.25μH 10.7MHz
FL4 4.25μH 10.7 MHz
YFL1 5 KHz
YFL 2 15 KHz
YFL 3 6 KHz
YFL 4 6 KHz
YFL 5 200 KHz
YFL 6 200 KHz
AGC ADJ R65 200K
BFO LEVEL R51 200
21.4 MHz TO PHASE LOCK
U1A SN74LS74N
U1B SN74LS74N
Q1 3N201
Q2 3N201
Q3 2N2222
Q4 2N2222
Q5 SP90388
Q6 2N3646
Q7 2N2222
Q8 Q9 Q10 66382
CR9 MV209
CR16 LM329 6.9V
CR10 HP2800
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR11 CR12 CR13 CR14 CR19 CR20 MA47047
IN4148
+12V
+5V
+5VA
-12V
AGC
GND
TUNE
FM MOD
SSB
GEN
TP1
TP2
10.7 MHz RECEIVER (4300)
PC BD 1700-5224-300
PC BD ASSY 7010-5234-301
MECH ASSY 7005-5244-300

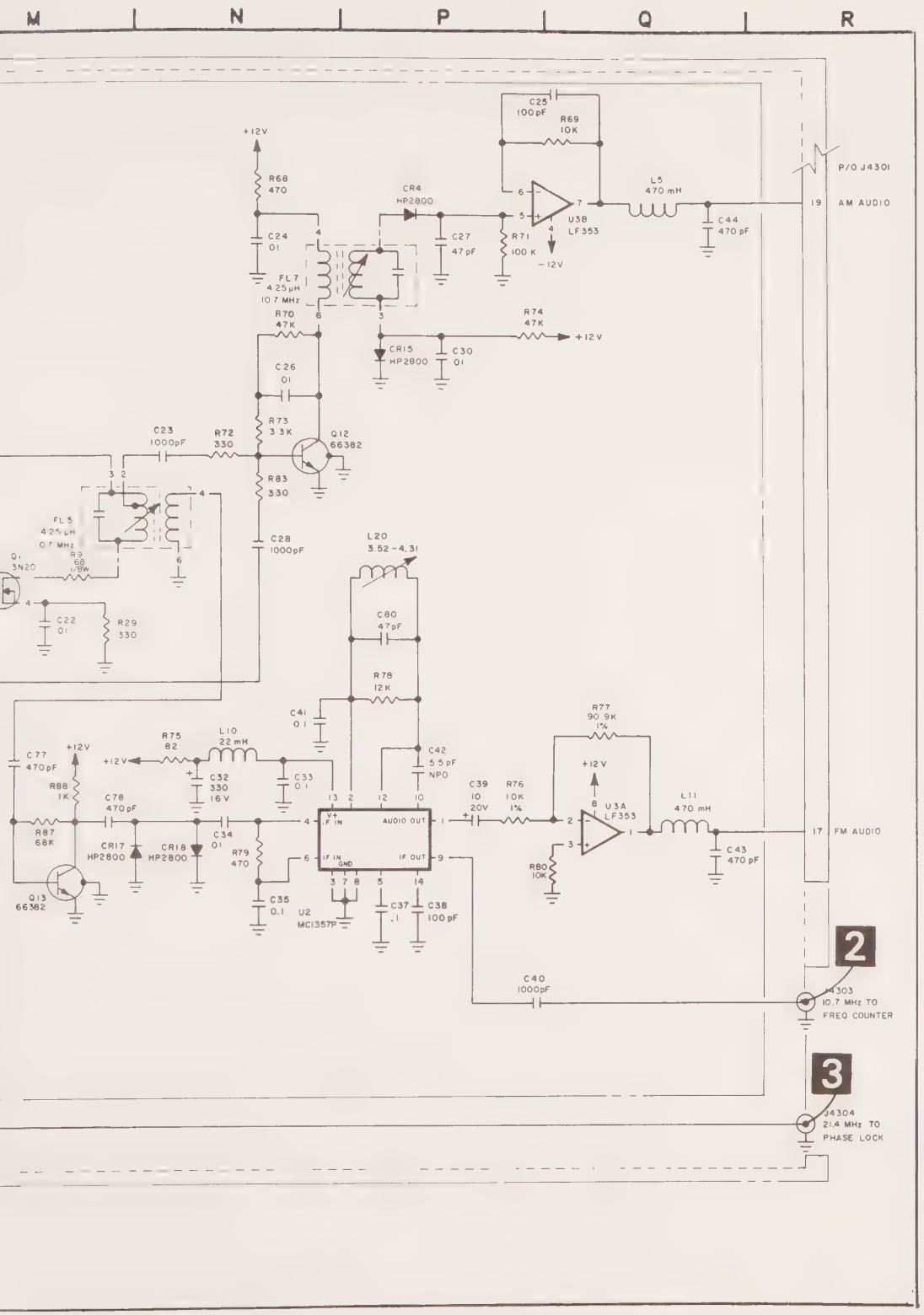
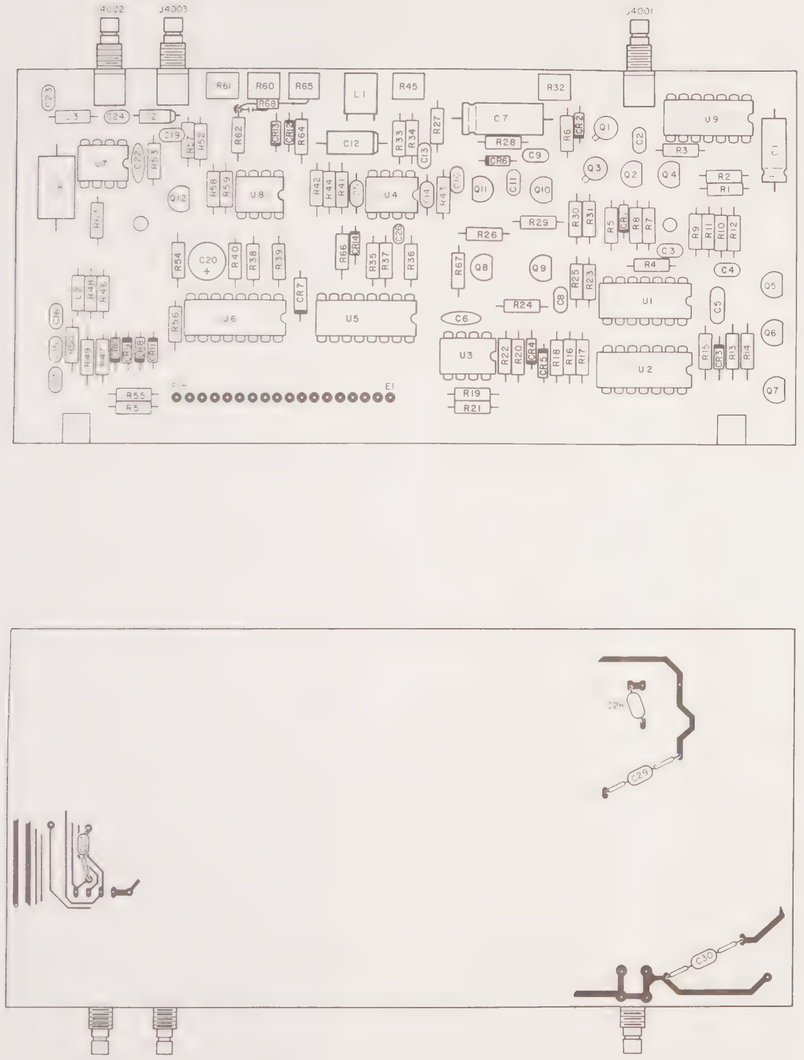
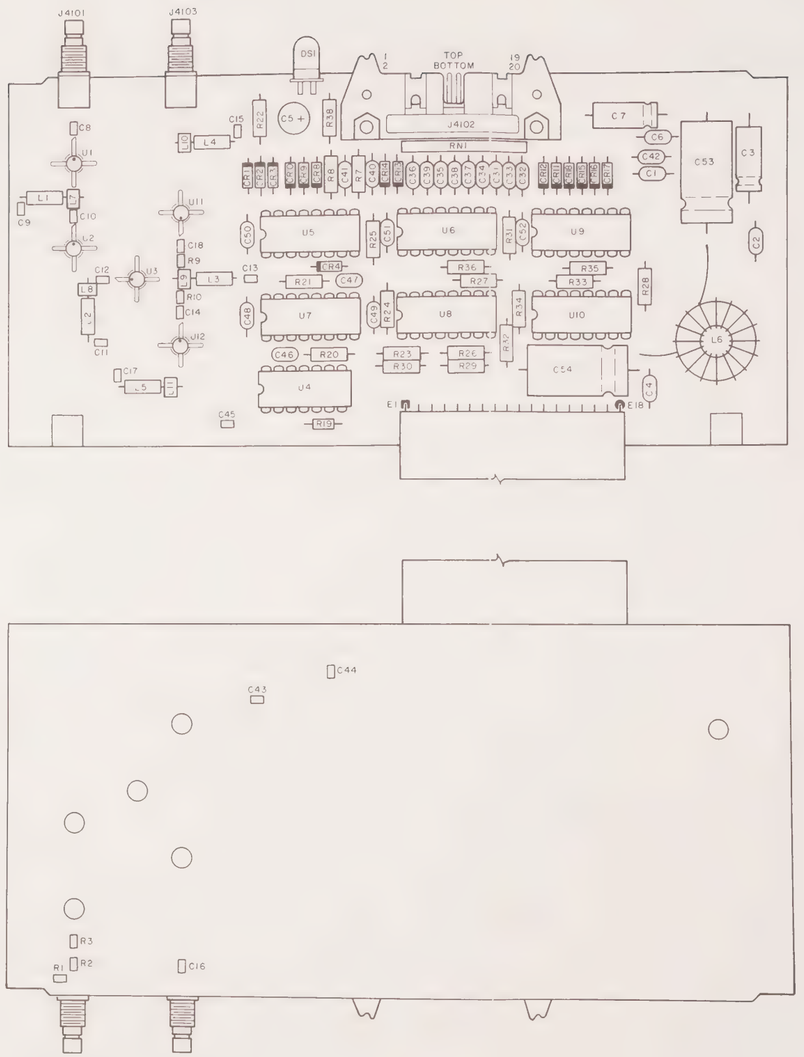


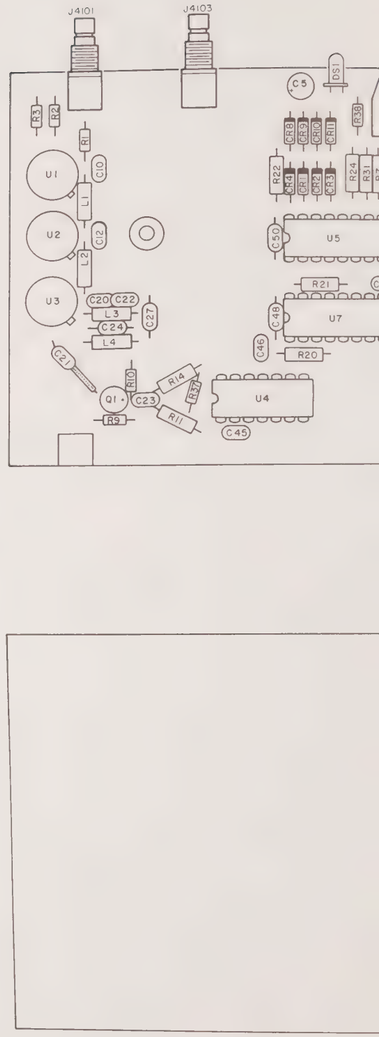
Figure 6-21 10.7 MHz GEN/REC PC Board Assembly (FM/AM-1200A) (Sheet 2 of 2) (0000-5124-300-R5)



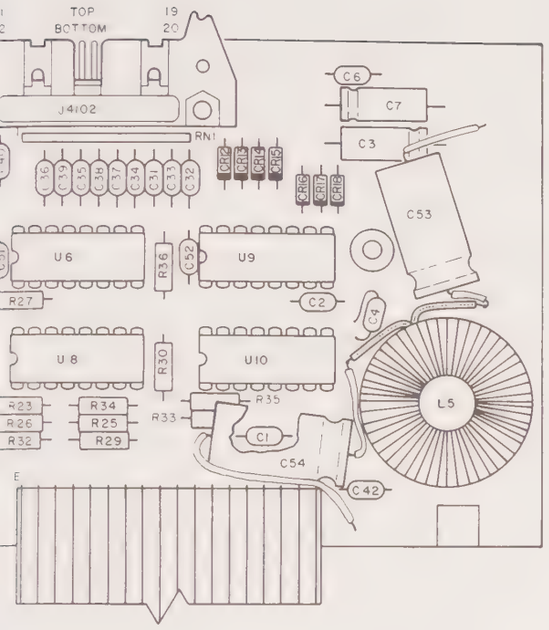
HIGH LOOP ANALOG PC BOARD ASSY (FM/AM-1200S/A)
(7010-5134-000-E2)

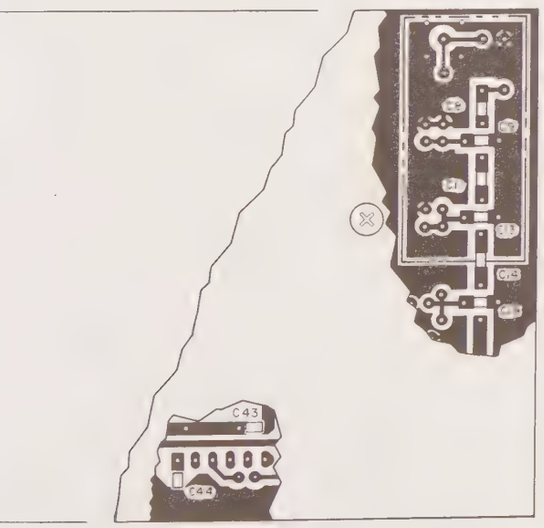


HIGH LOOP DIVIDER PC BOARD ASSY (FM/AM-1200S)
(7010-7030-000-B)



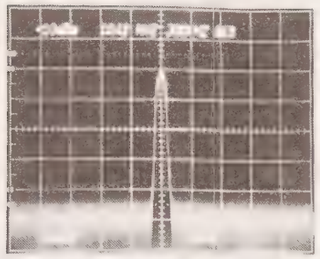
HIGH LOOP DIVIDER
(7010-5134-100-E9)



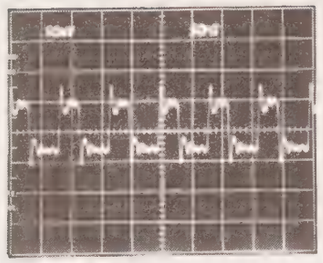


OARD ASSY (FM/AM-1200A)

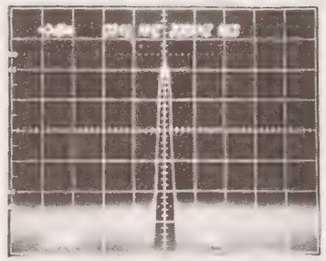
1



2



3



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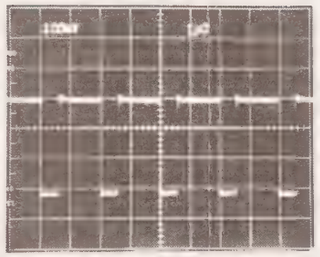

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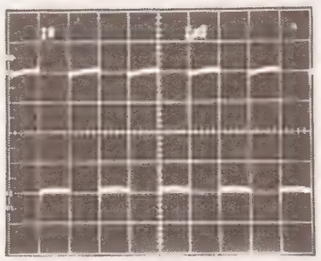
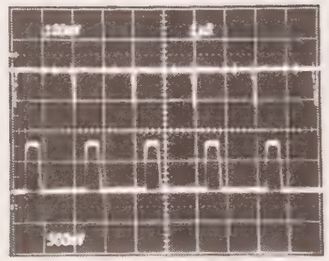


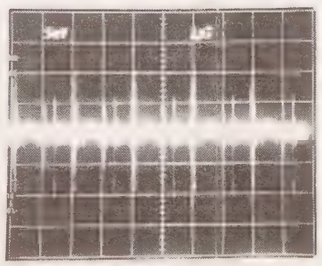
X1 PROBE

6



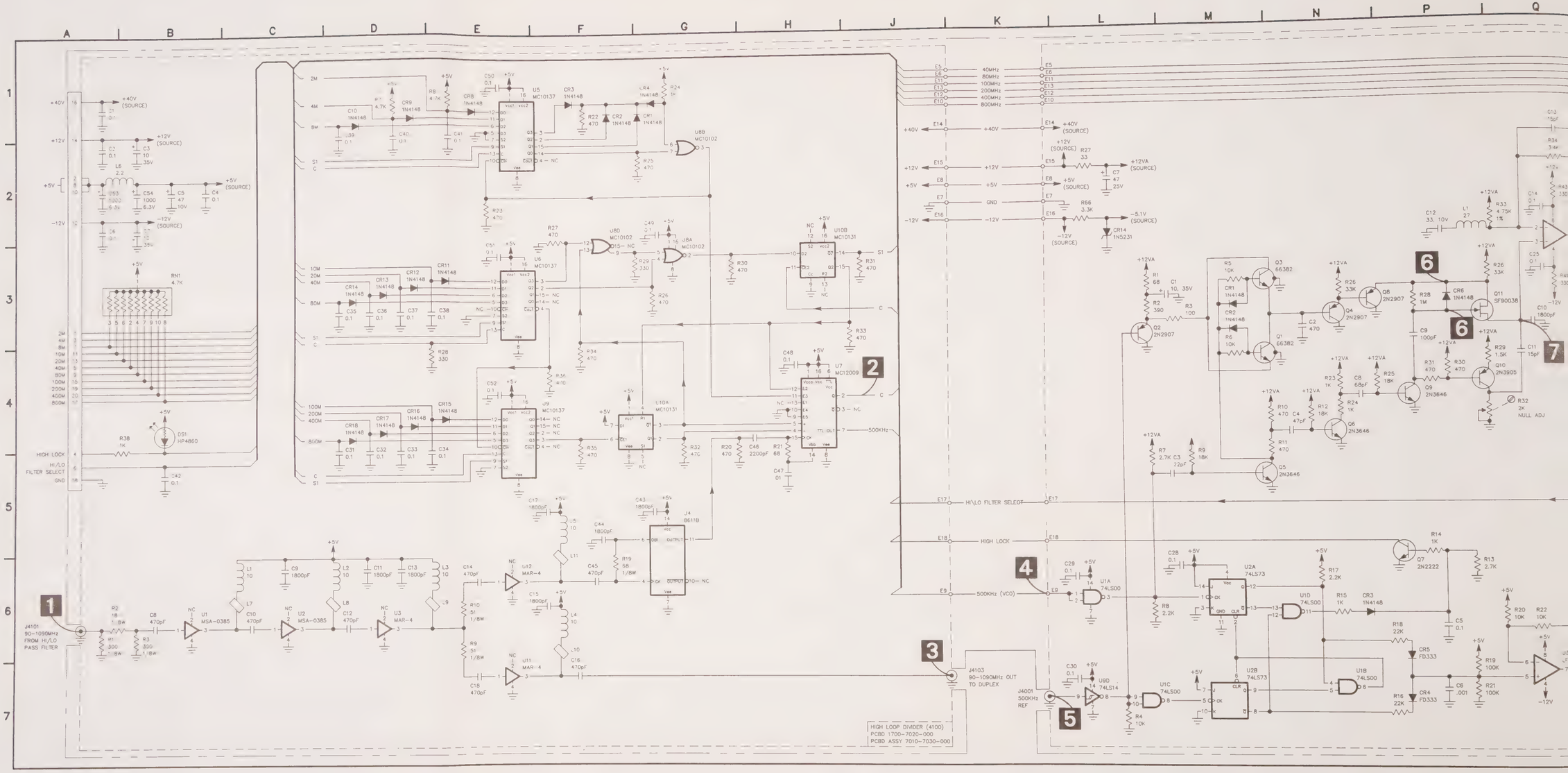
TOP TRACE: Q11, PIN S.
BOTTOM TRACE: Q11, PIN G

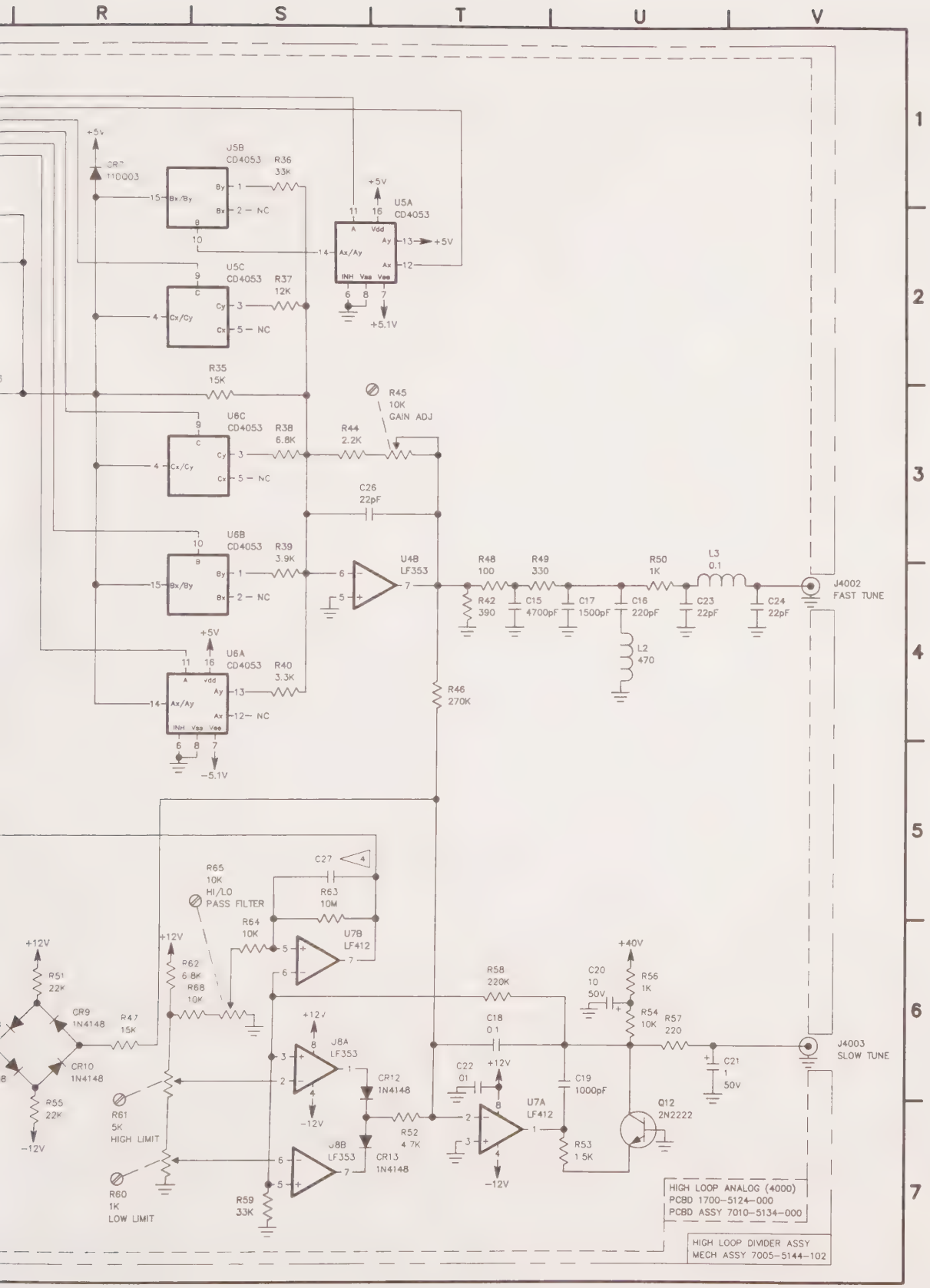
7



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X10 PROBE, UNLESS OTHERWISE NOTED.

Figure 6-22 High Loop PC Board Assembly (Sheet 1 of 3)
(0000-5114-000-E2/0000-7010-000-B


HIGH LOOP DIVIDER (4100)
PCBD 1700-7020-000
PCBD ASSY 7010-7030-000



NOTES:

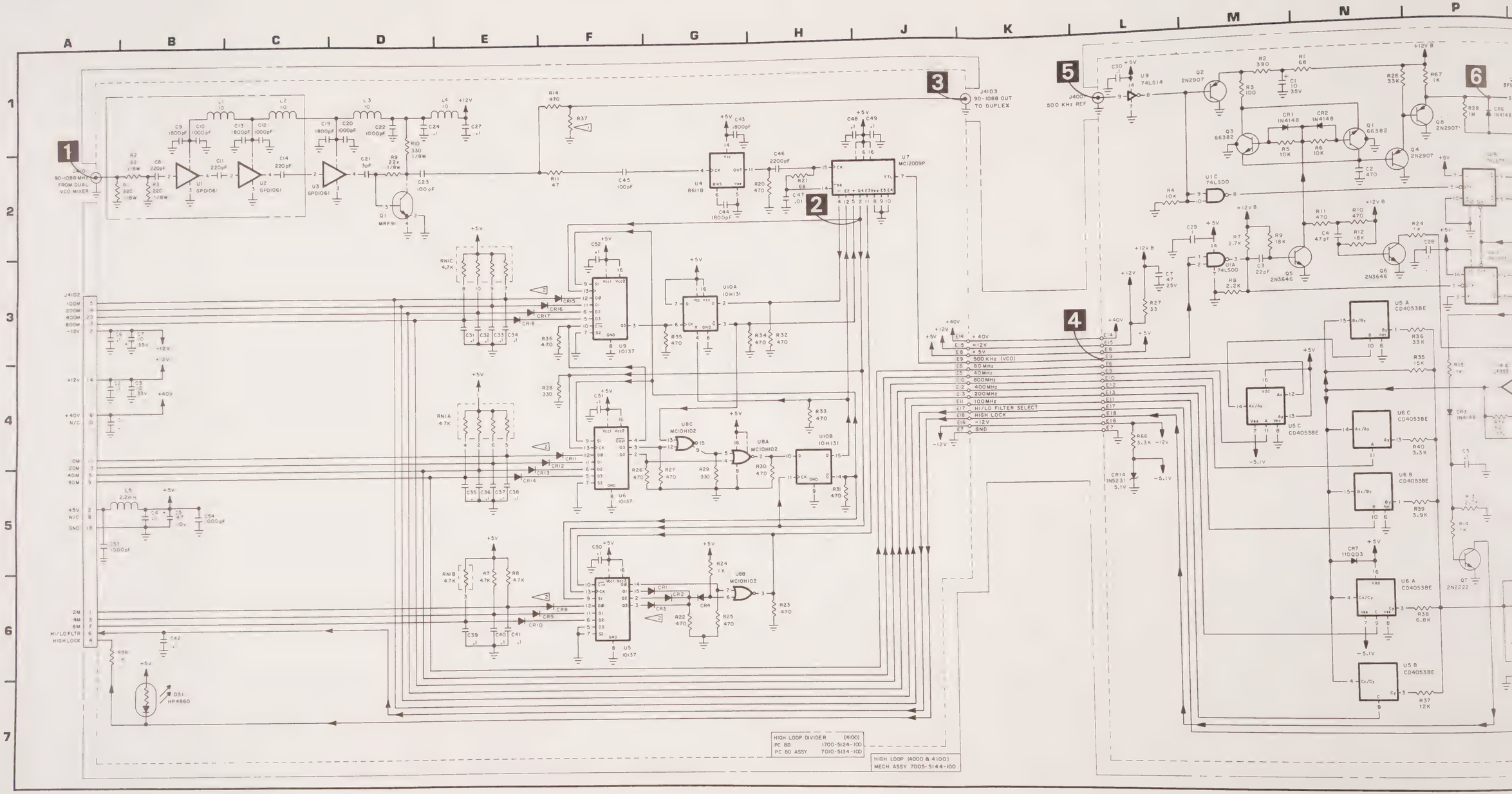
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 4000 (I.E., R1 IS R4001).

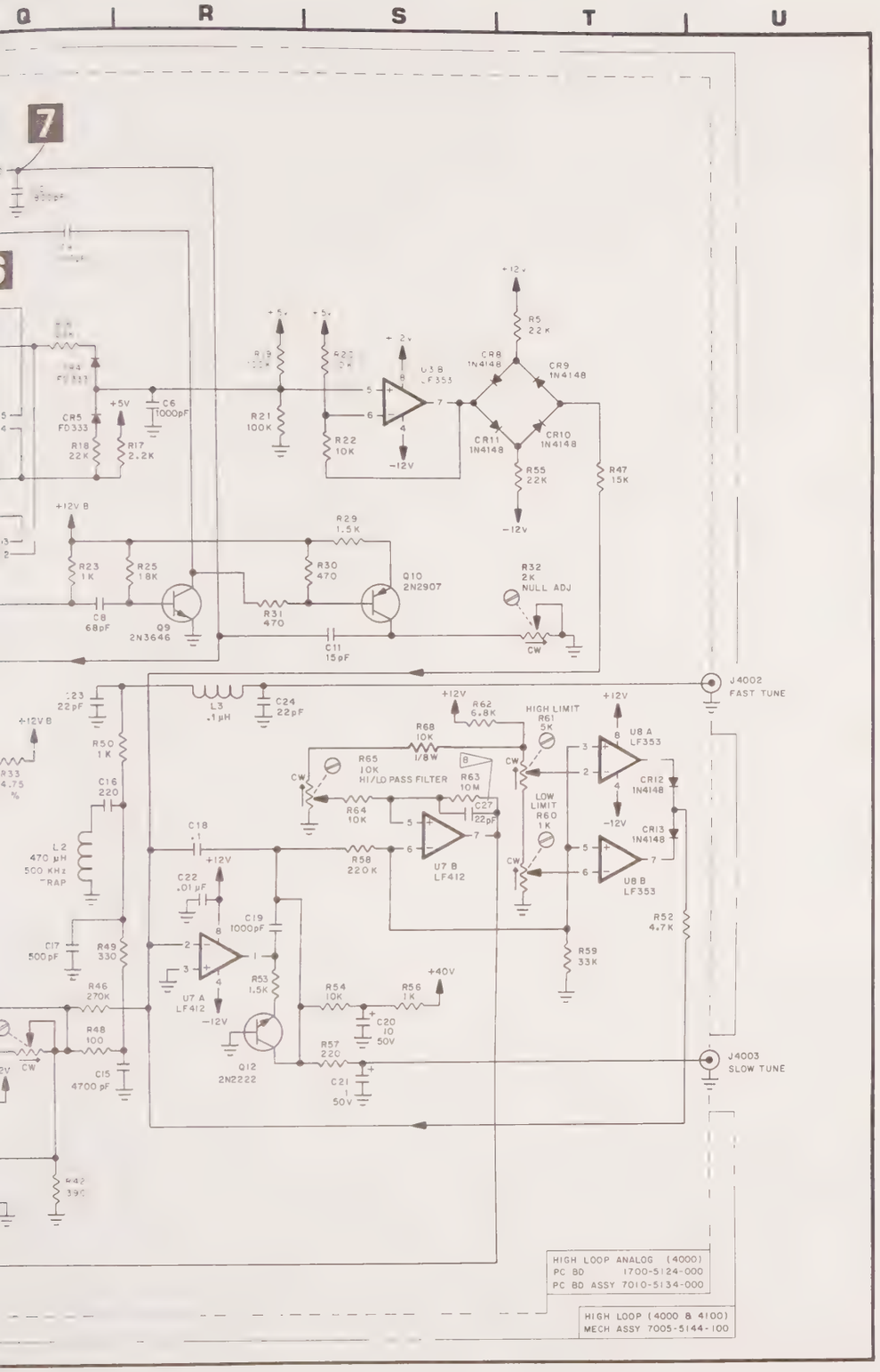
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4. C4027 IS SELECTED AT TEST (S.A.T.):
   RANGE: 10pF TO 47 pF
   NOMINAL: 22 pF.

Figure 6-22 High Loop PC Board Assembly (Sheet 2 of 3)
(0000-5114-000-E2/0000-7010-000-B)


A B C D E F G H J K L M N P
1 2 3 4 5 6 7
J400 90-1088 MHz FROM DUAL VCO MIXER
J4103 90-1088 OUT TO DUPLEX
J400 500 KHz REF
J4102
100M 200M 400M 800M -12V +12V +40V N/C 0M 20M 40M 80M +5V N/C GND 2M 4M 8M HI/LO FLTR HIGH LOCK
+40V +12V +5V 500 KHz (VCO) 80MHz 40MHz 800MHz 400MHz 200MHz 100MHz HI/LO FILTER SELECT HIGH LOCK -12V GND
DS1 HP4860
HIGH LOOP DIVIDER (4100)
PC BD 1700-5124-100
PC BD ASSY 7010-5134-100
HIGH LOOP (4000 & 4100)
MECH ASSY 7005-5144-100



NOTES:

1. R4137 IS SELECTED AT TEST (S.A.T.):
   RANGE: 22Ω TO 56Ω
   NOMINAL: 33Ω

2. ALL DIODES ARE IN4148.

3. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. HIGH LOOP ANALOG - 4000 (I.E., R1 IS R4001).
   B. HIGH LOOP DIVIDER - 4100 (I.E., R1 IS R4101).

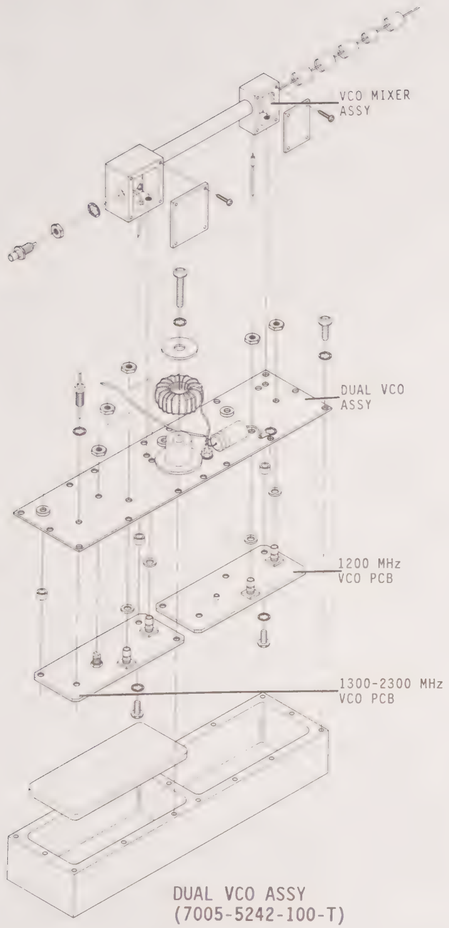
4. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

5. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

6,7. NOT USED.

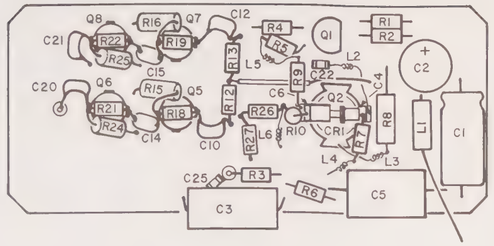
8. C4027 IS SELECTED AT TEST (S.A.T.):
   RANGE: 10 pF TO 47 pF
   NOMINAL: 22 pF

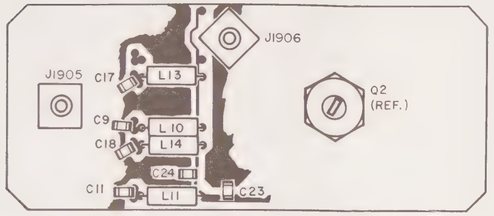
Figure 6-22 High Loop PC Board Assembly (Sheet 3 of 3)
(0000-5114-000-E2/0000-7010-000-B)



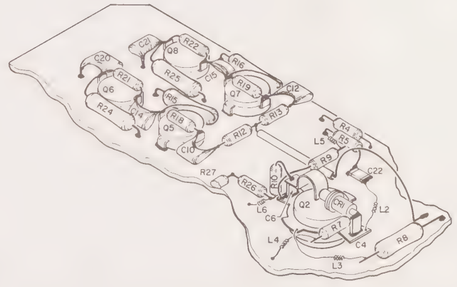
DUAL VCO ASSY (7005-5242-100-T)

VCO MIXER ASSY (7005-5241-900-T)

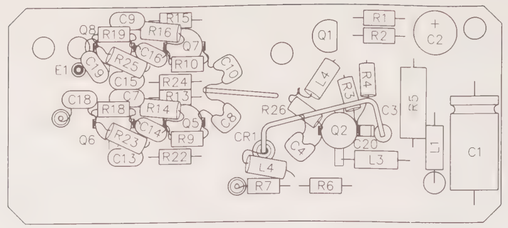


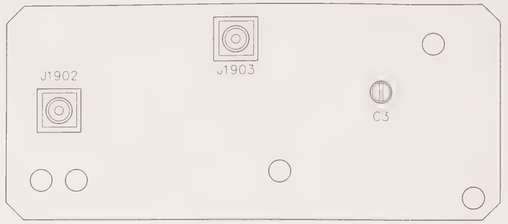


1300-2300 MHz VCO PC BOARD ASSY (7010-5232-100-AK)



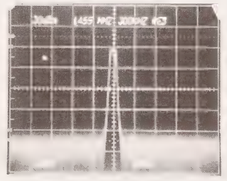
DETAIL **A**



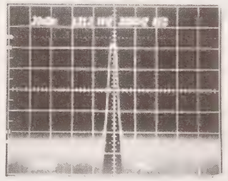


1210 MHz PC BOARD ASSY (7010-5232-000-L3)

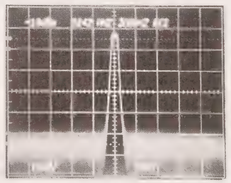
1



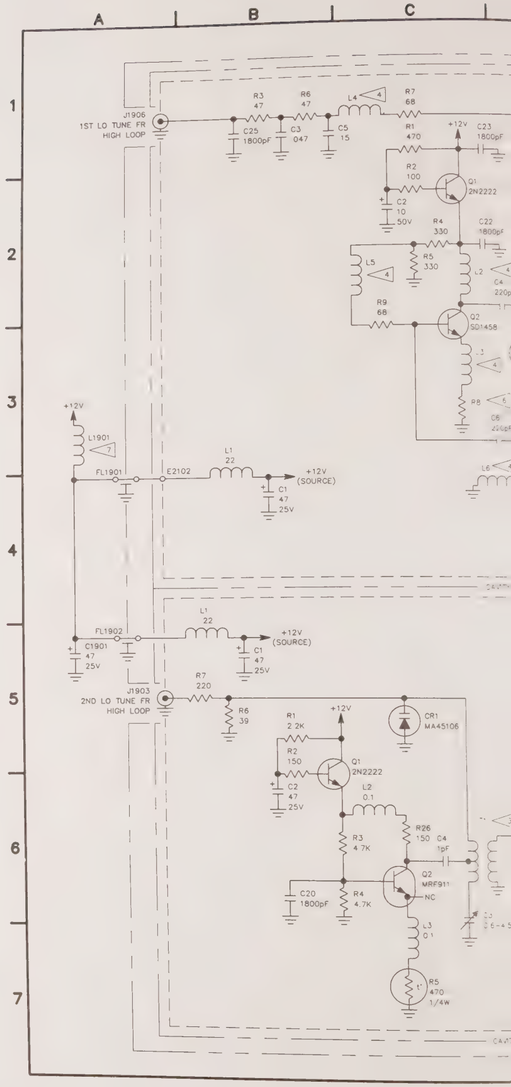
2

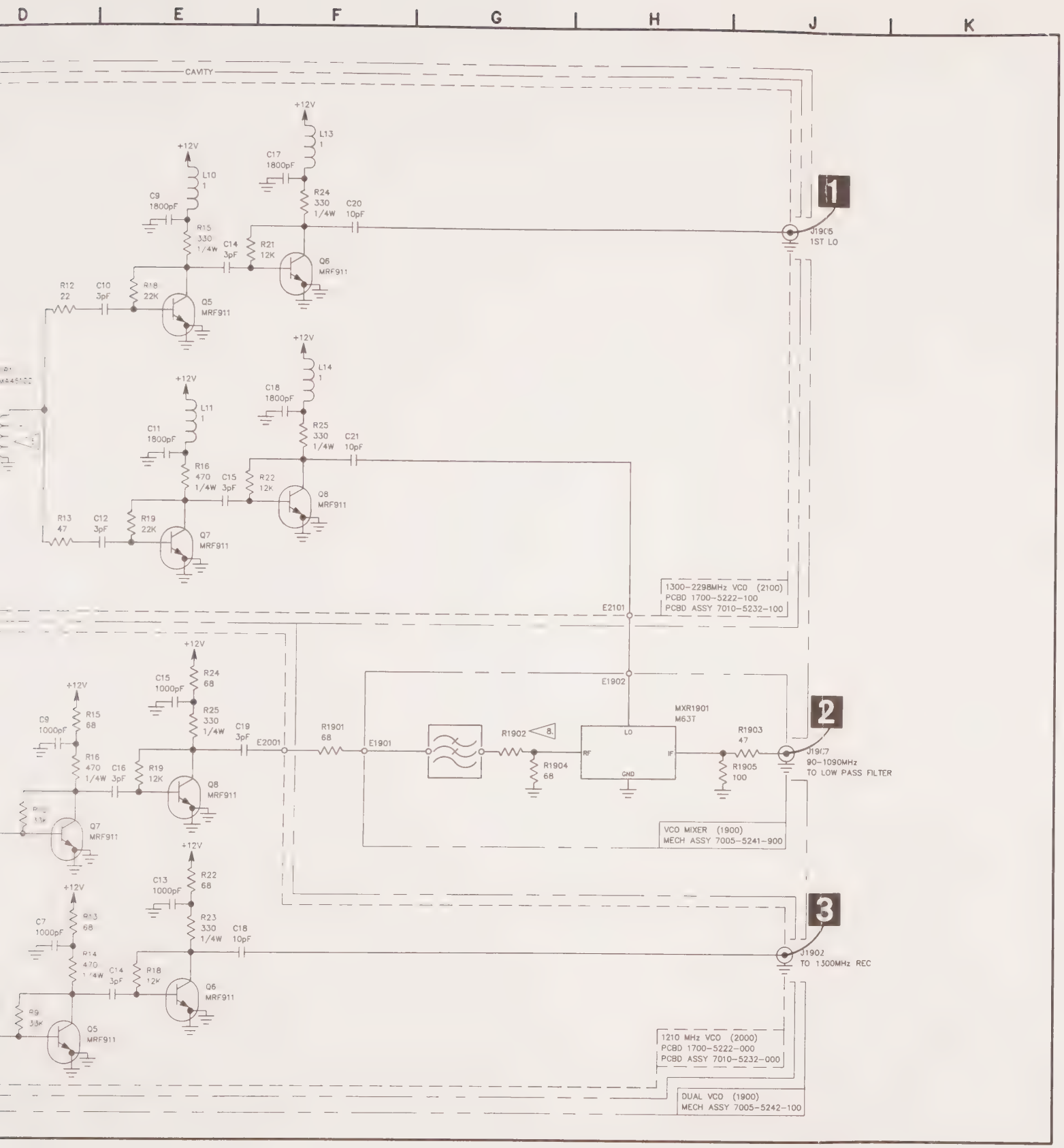


3



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S/A SET AT 150.2 MHz IN RECEIVE MODE WITH NO INPUT SIGNAL.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. VCO MIXER - 1900 (I.E., R1 IS R1901).
   B. 1210 MHZ PCB - 2000 (I.E., R1 IS R2001).
   C. 1300 MHZ-2298 MHZ PCB - 2100 (I.E., R1 IS R2101).

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. PRIMARY (T2001) IS FORMED BY LEAD OF C2004 PLACED 0.38" FROM SECONDARY. SECONDARY IS FORMED BY 0.8" LENGTH 22 GA. WIRE.

4. INDUCTORS ARE MADE FROM 10 TURNS OF 38 GA. WIRE.

5. PRIMARY (T2101) IS FORMED BY LEAD OF C2106 SOLDERED TO CR2101. LENGTH SELECTED AT TEST (S.A.T.). SECONDARY IS 22 GA. WIRE, BENT WITHIN 0.4" OF BOARD SURFACE, THEN BACK WITHIN 0.2" OF PRIMARY.

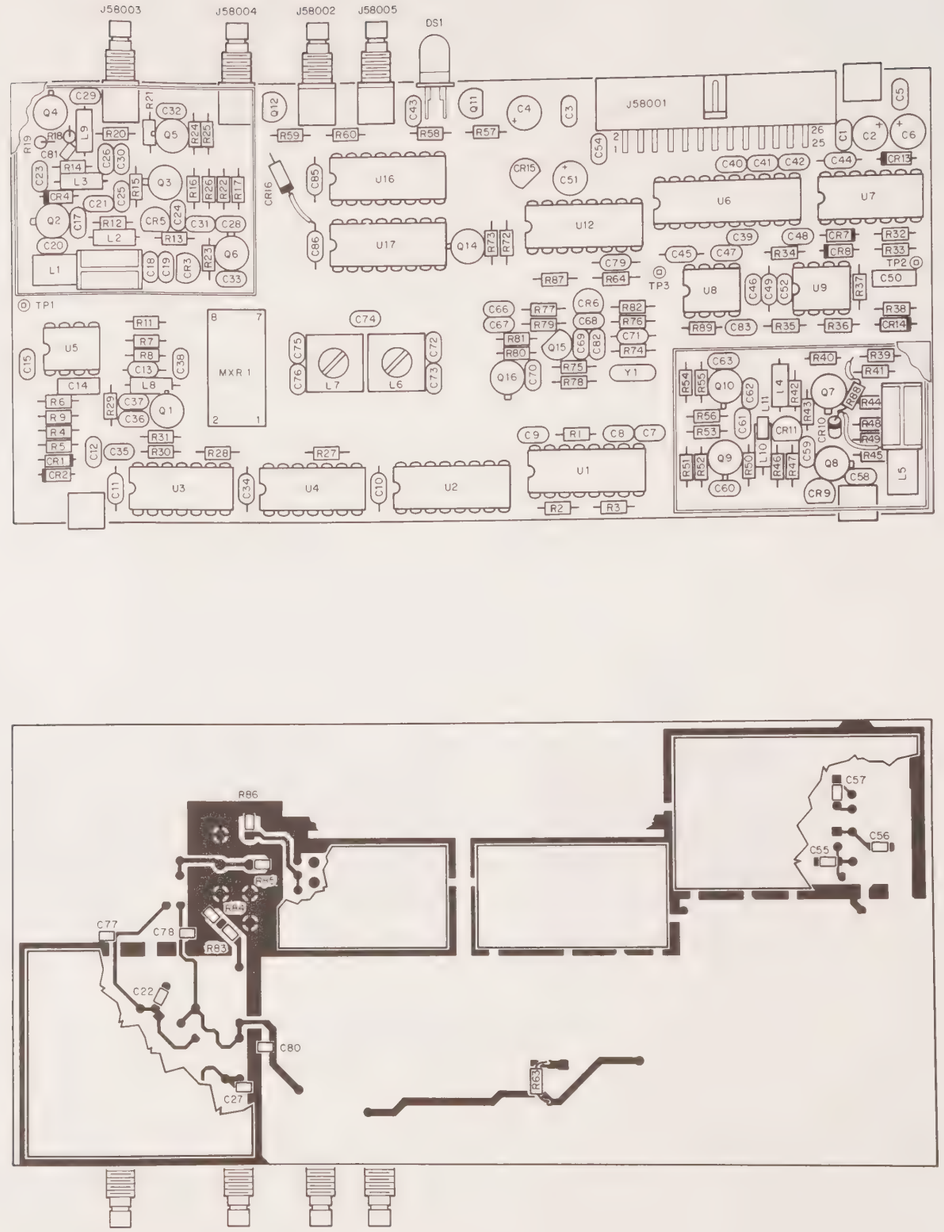
6. R2108 IS SELECTED AT TEST (S.A.T.):
   RANGE: 47Ω TO 220Ω
   NOMINAL: 180Ω

7. TOROID IS 18 GA., 30 TURNS.

8. R1902 IS SELECTED AT TEST (S.A.T.):
   RANGE: 68Ω TO 330Ω
   NOMINAL: 150Ω

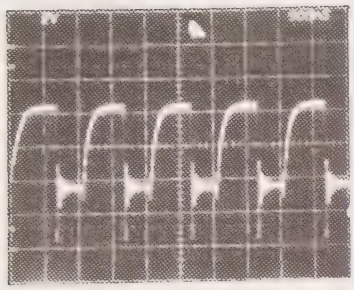
9. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-23 Dual VCO Assembly
(0000-5212-000-L2/0000-5212-100-AA)

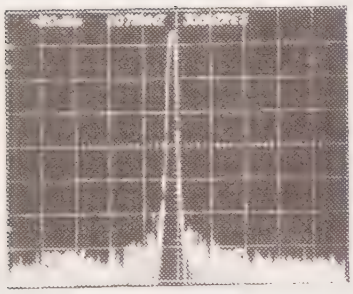


FAST LOW LOOP PC BOARD ASSY
(7010-5931-000-E5)

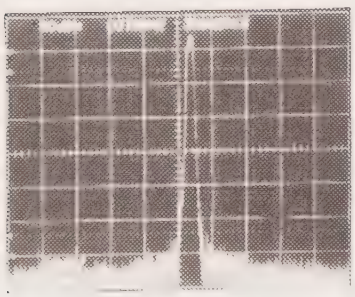
1



2

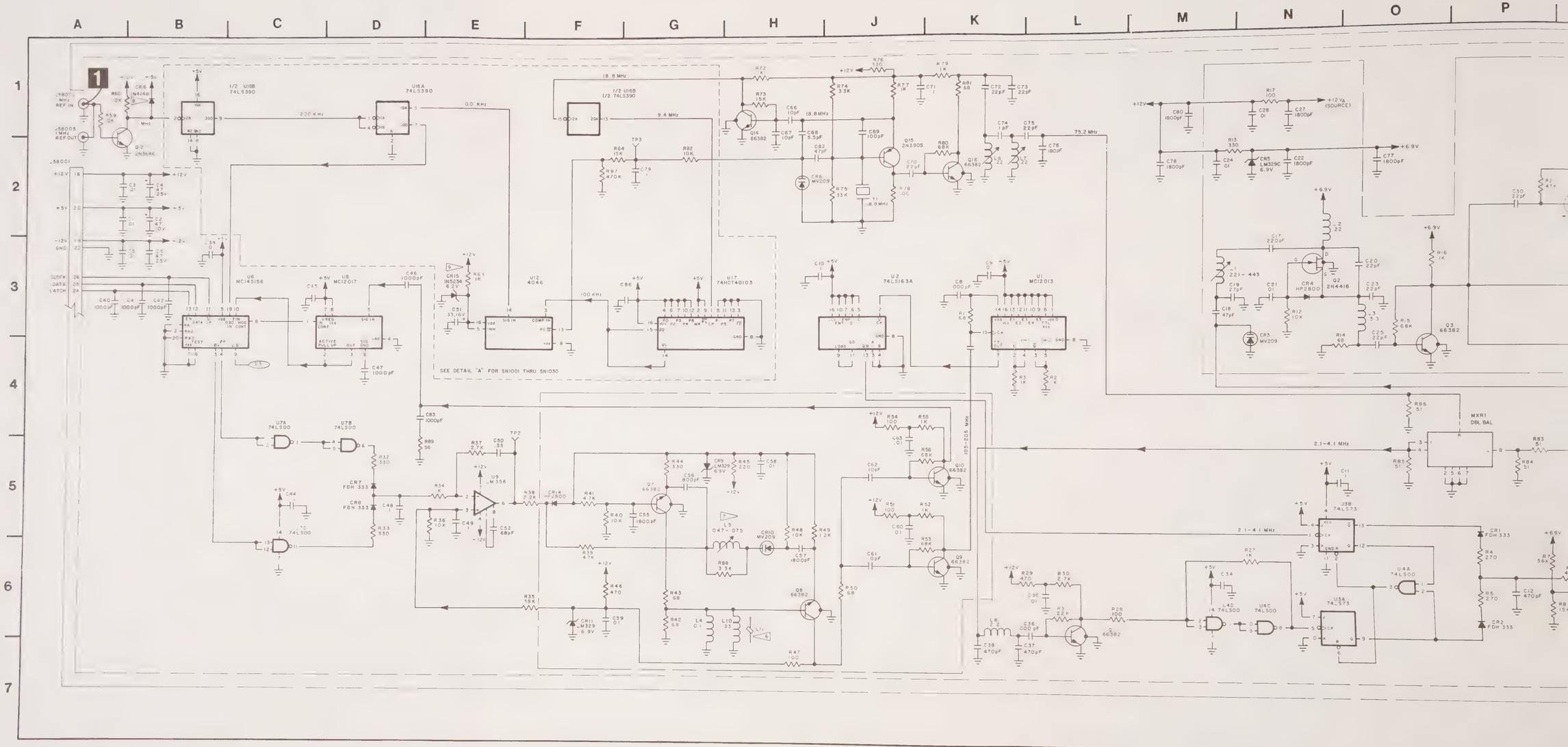


3

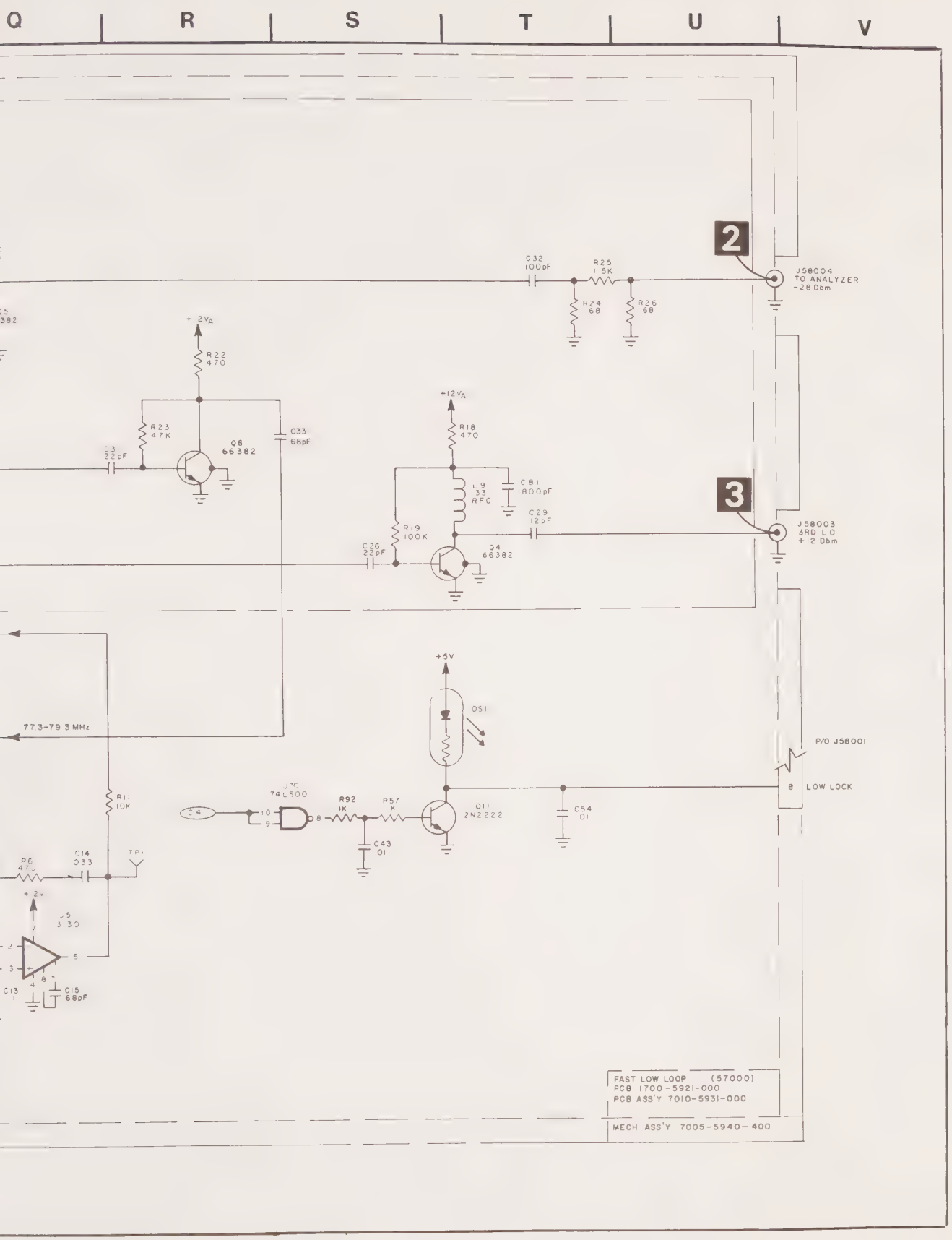


NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S/A SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X1 PROBE.

Figure 6-24 Fast Low Loop PC Board Assembly (Sheet 1 of 2) (0000-5911-000-E3)



A B C D E F G H J K L M N O P
1 2 3 4 5 6 7
1
1/2 U16B 74LS390
U16A 74LS390
1/2 U16B 1/2 74LS390
U6 MC145156
U8 MC12017
U12 4046
U17 74HCT40103
U2 74LS163A
U1 MC12013
U7A 74LS00
U7B 74LS00
U9 LM356
U3B 74LS73
U3A 74LS73
U4A 74LS00
U4C 74LS00
U4D 74LS00
MXR1 DBL BAL
SEE DETAIL "A" FOR SN1001 THRU SN1030
+12V
+6.9V
+12V Va (SOURCE)



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 57000 (I.E., R1 IS R57001).

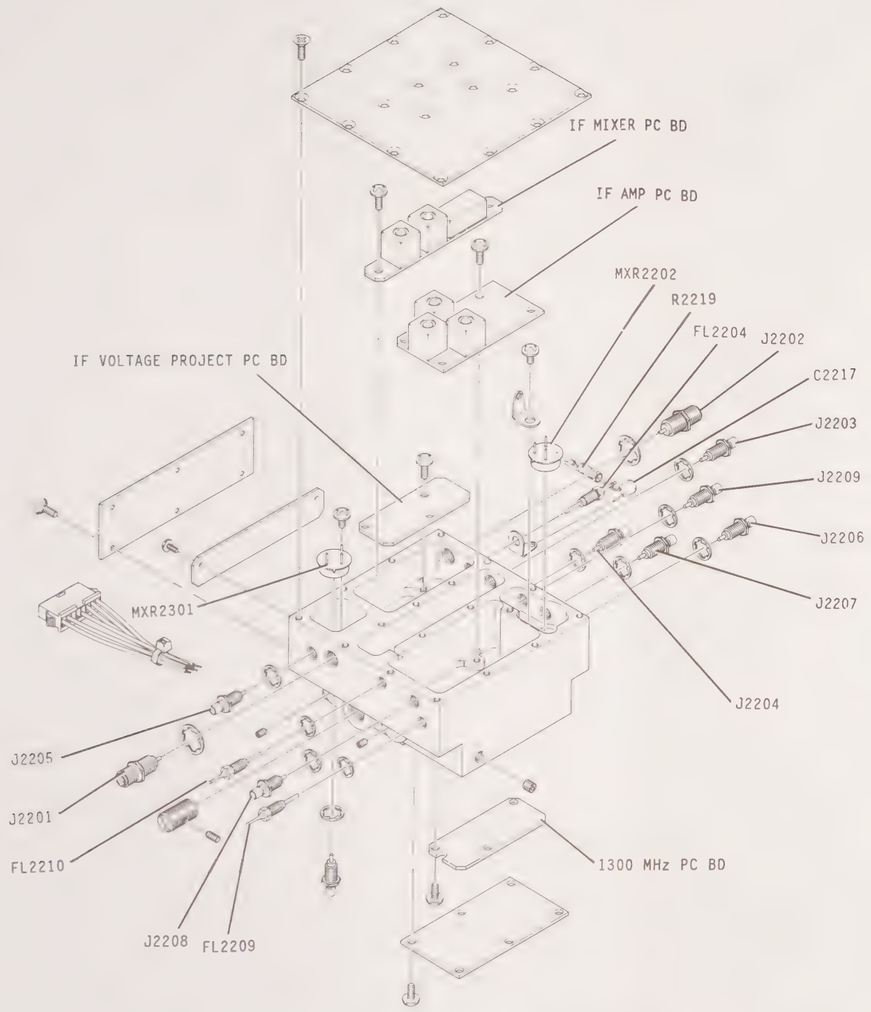
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

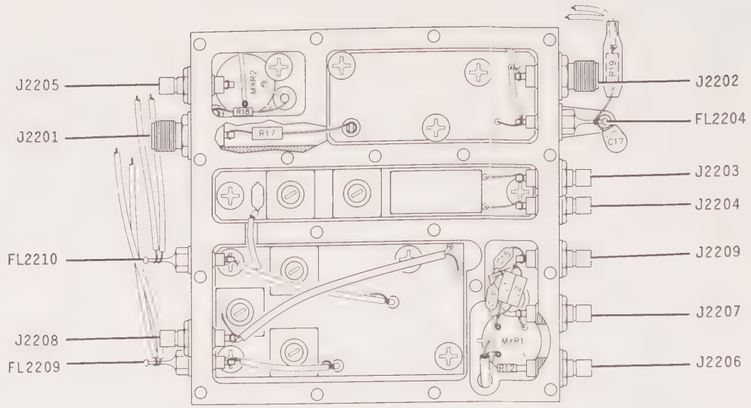
4, 5. NOT USED.

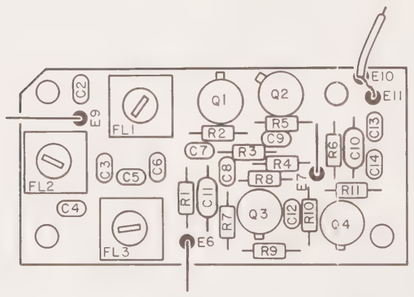
6. FERRITE BEAD IS LOCATED ADJACENT TO L57010 TO "DE-Q" THE RF CIRCUIT, PREVENTING SELF-OSCILLATION.

Figure 6-24 Fast Low Loop PC Board Assembly (Sheet 2 of 2) (0000-5911-000-E3)

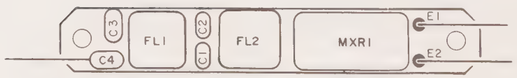


IF ASSY (7005-5141-900-Y)

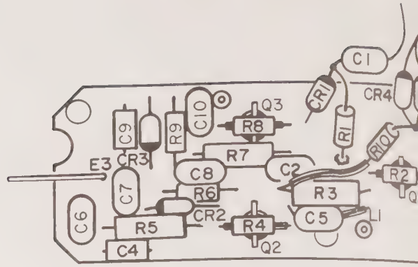


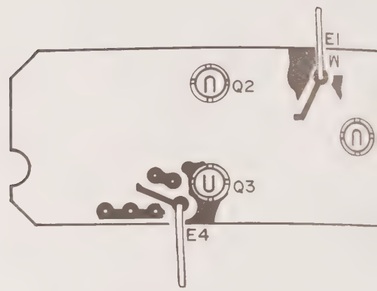


IF AMP PC BOARD ASSY
(7010-5131-900-C7)

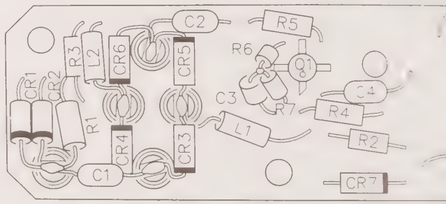


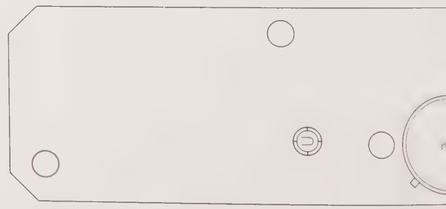
IF MIXER PC BOARD ASSY
(7010-5232-300-A4)



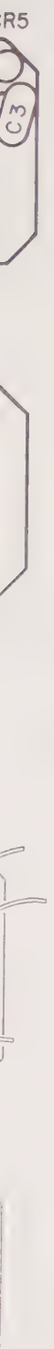


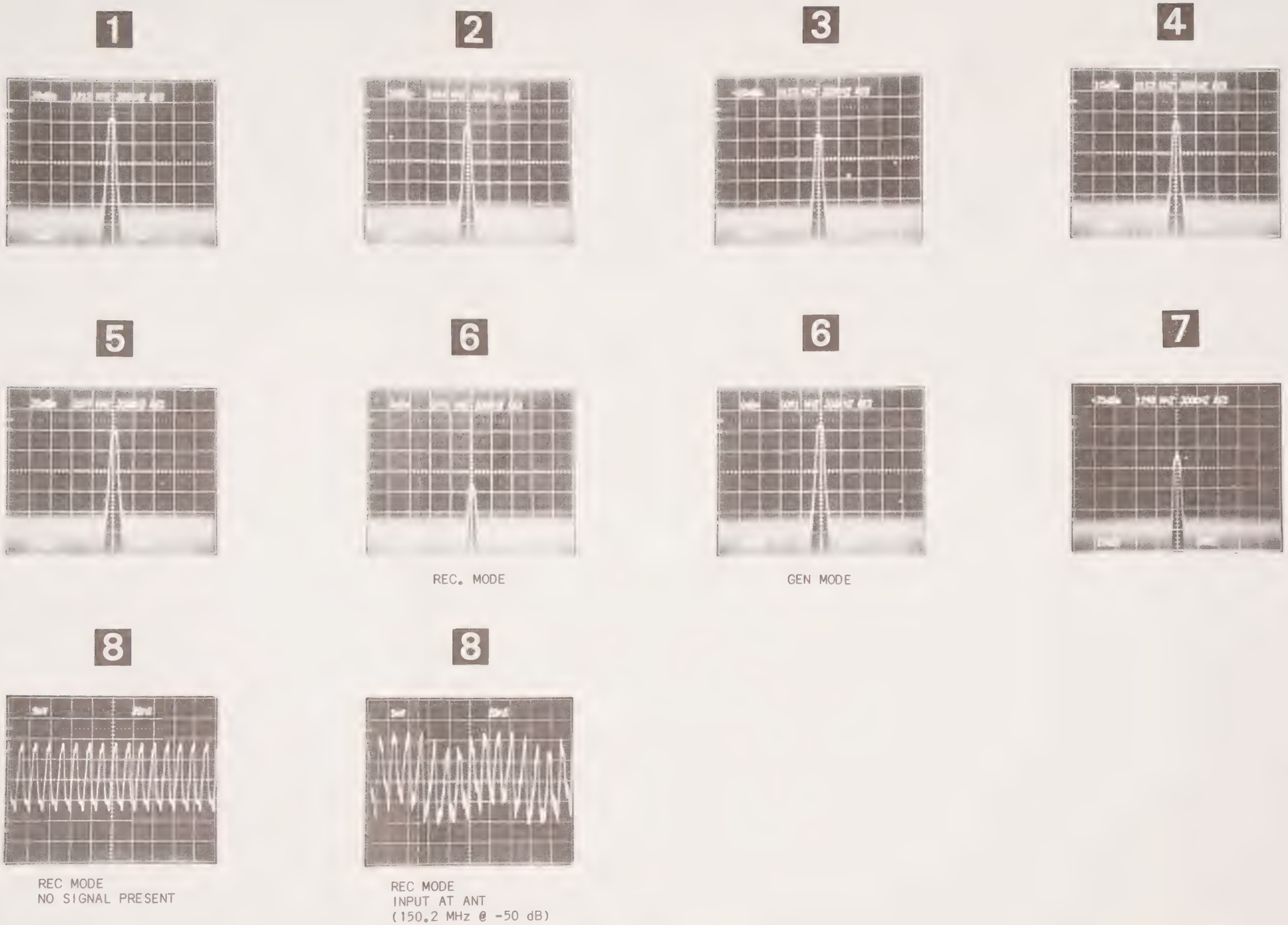
1300 MHz PC BOARD ASSY
7010-5232-400C





IF VOLTAGE PROJECT PC BOARD A
(7010-5133-700-B7)





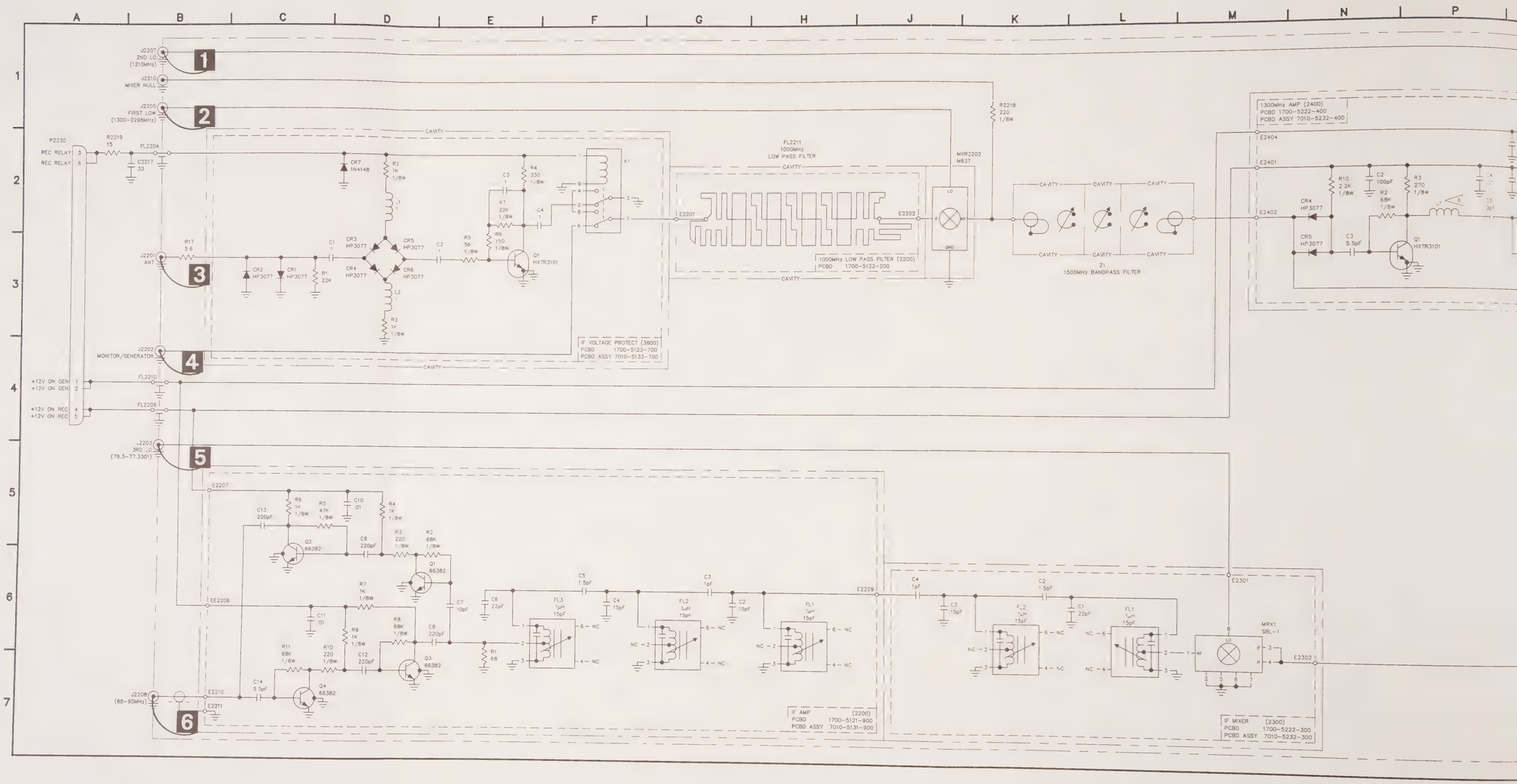
REC. MODE

GEN MODE

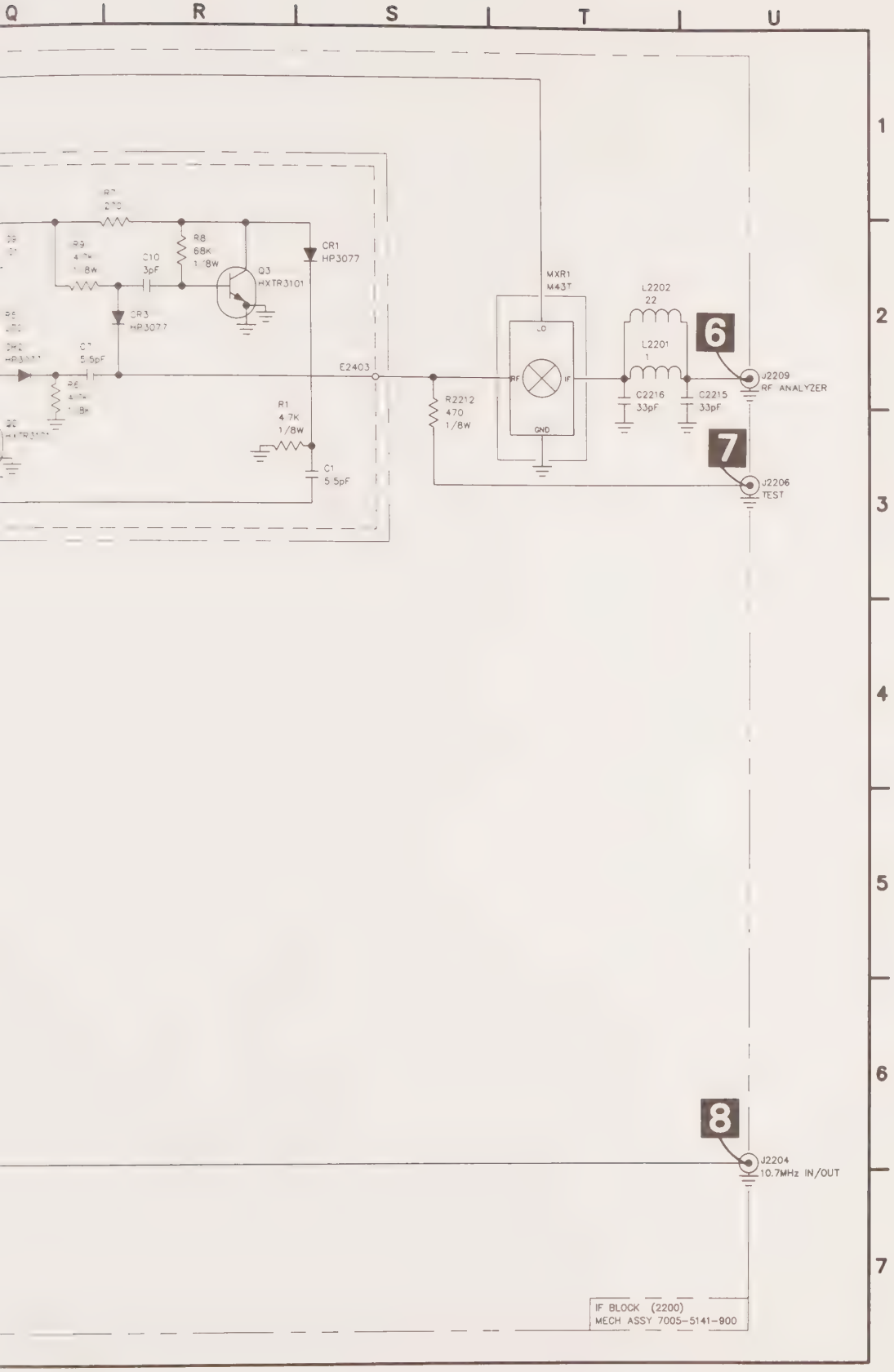
REC MODE
NO SIGNAL PRESENT

REC MODE
INPUT AT ANT
(150.2 MHz @ -50 dB)

Figure 6-25 IF Block Assembly (Sheet 1 of 2)
(000-5111-900-K)



J2207 2ND LO (1210MHz)
J2210 MIXER NULL
J2205 FIRST LOW (1300-2298MHz)
P2230
REC RELAY
REC RELAY
R2219 15
FL2204
C2217 33
J2201 ANT
R17 5.6
J2202 MONITOR/GENERATOR
+12V ON GEN
+12V ON GEN
+12V ON REC
+12V ON REC
FL2210
FL2209
J2203 3RD LO (79.3-77.3301)
J2208 (88-90MHz)
CAVITY
CR7 1N4148
R2 1K 1/8W
CR3 HP3077
CR5 HP3077
CR4 HP3077
CR6 HP3077
CR2 HP3077
CR1 HP3077
R1 22K
R3 1K 1/8W
R4 330 1/8W
R5 56 1/8W
R6 150 1/8W
R7 22K 1/8W
Q1 HXTR3101
K1
IF VOLTAGE PROTECT (3800)
PCBD 1700-5123-700
PCBD ASSY 7010-5133-700
FL2211 1000MHz LOW PASS FILTER
E2201
E2202
1000MHz LOW PASS FILTER (2200)
PCBD 1700-5122-200
MXR2202 M63T
R2218 220 1/8W
Z1 1500MHz BANDPASS FILTER
1300MHz AMP (2400)
PCBD 1700-5222-400
PCBD ASSY 7010-5232-400
E2404
E2401
E2402
R10 2.2K 1/8W
C2 100pF
R3 270 1/8W
R2 68K 1/8W
CR4 HP3077
CR5 HP3077
C3 5.5pF
Q1 HXTR3101
E2207
EE2206
E2210
E2211
Q2 66382
Q1 66382
Q3 66382
Q4 66382
R6 1K 1/8W
R5 47K 1/8W
C10 01
R4 1K 1/8W
C13 220pF
C9 220pF
R3 220 1/8W
R2 68K 1/8W
R7 1K 1/8W
C11 01
R9 1K 1/8W
R8 68K 1/8W
C8 220pF
C7 10pF
R11 68K 1/8W
R10 220 1/8W
C12 220pF
C14 5.5pF
R1 68
C6 22pF
FL3 1μH 15pF
FL2 1μH 15pF
FL1 1μH 15pF
C5 1.5pF
C4 15pF
C3 1pF
C2 15pF
E2209
IF AMP (2200)
PCBD 1700-5121-900
PCBD ASSY 7010-5131-900
C4 1pF
C3 15pF
C2 1.5pF
C1 22pF
E2301
MRX1 SBL-1
E2302
IF MIXER (2300)
PCBD 1700-5222-300
PCBD ASSY 7010-5232-300



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. IF ASSY - 2200 (I.E., L1 IS L2201).
   B. IF MIXER - 2300 (I.E., R1 IS R2301).
   C. 1300 MHZ AMP - 2400 (I.E., R1 IS R2401).
   D. IF VOLTAGE PROTECT - 3800 (I.E., R1 IS R3801).

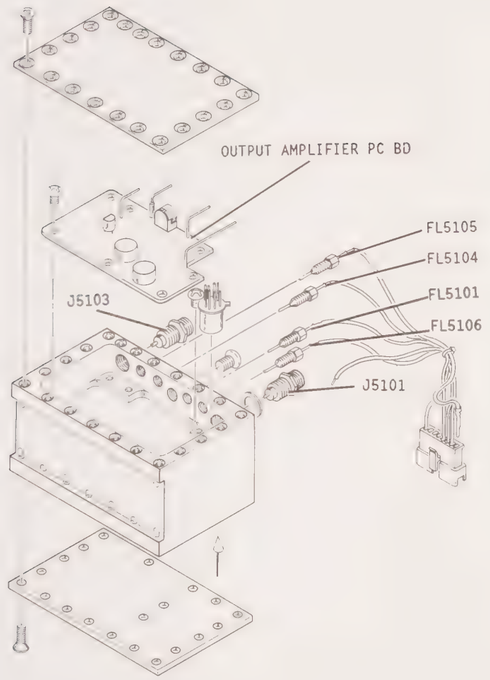
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

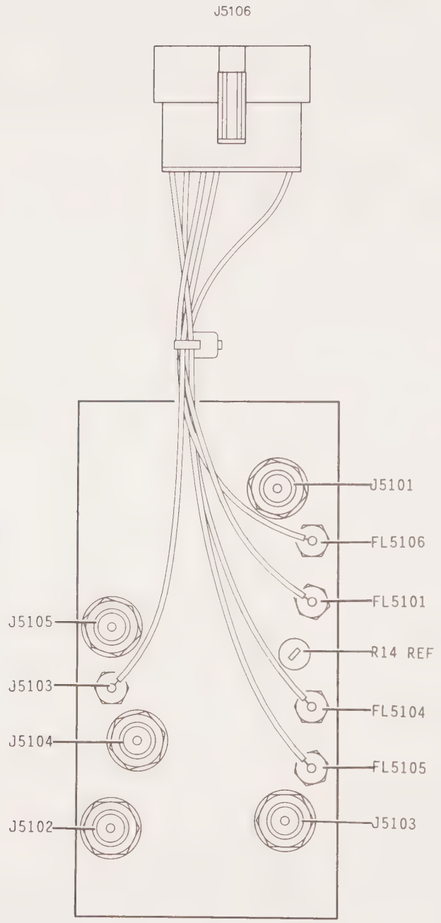
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

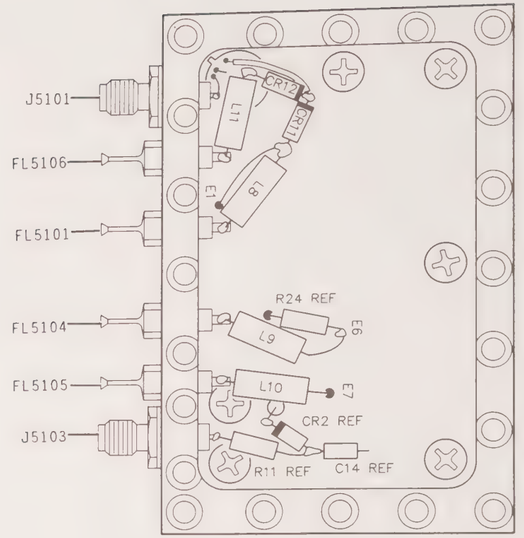
4, 5. NOT USED.

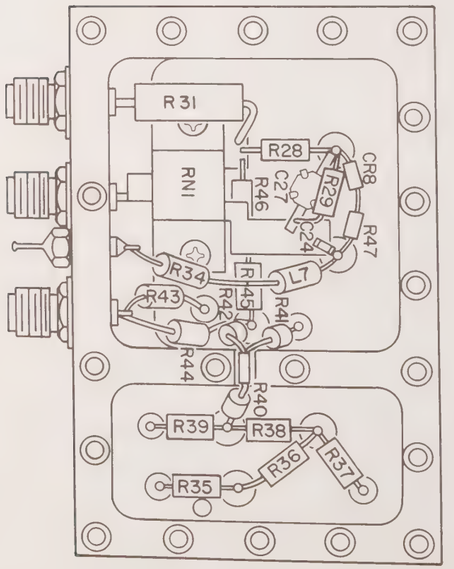
6. L2401 IS FORMED FROM .2" LEAD OF C2405.

Figure 6-25 IF Block Assembly (Sheet 2 of 2) (0000-5111-900-K)

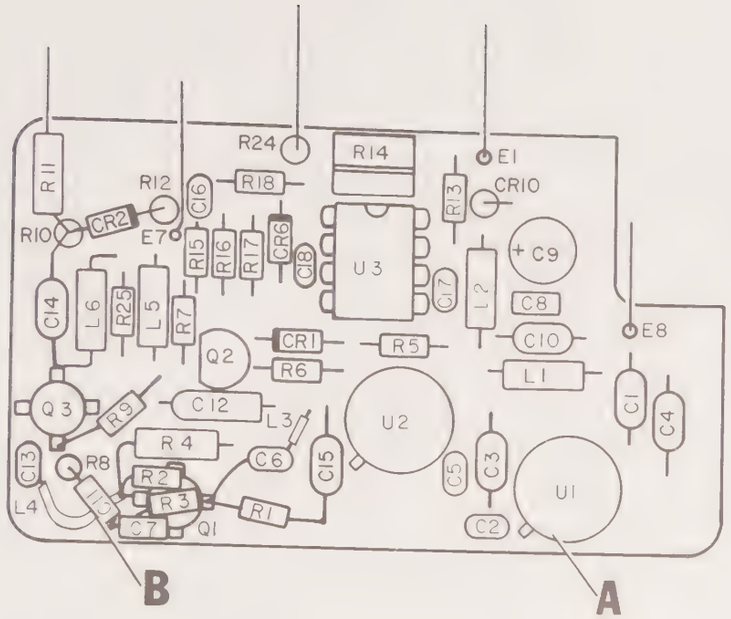


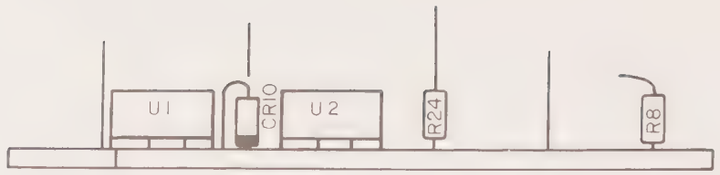




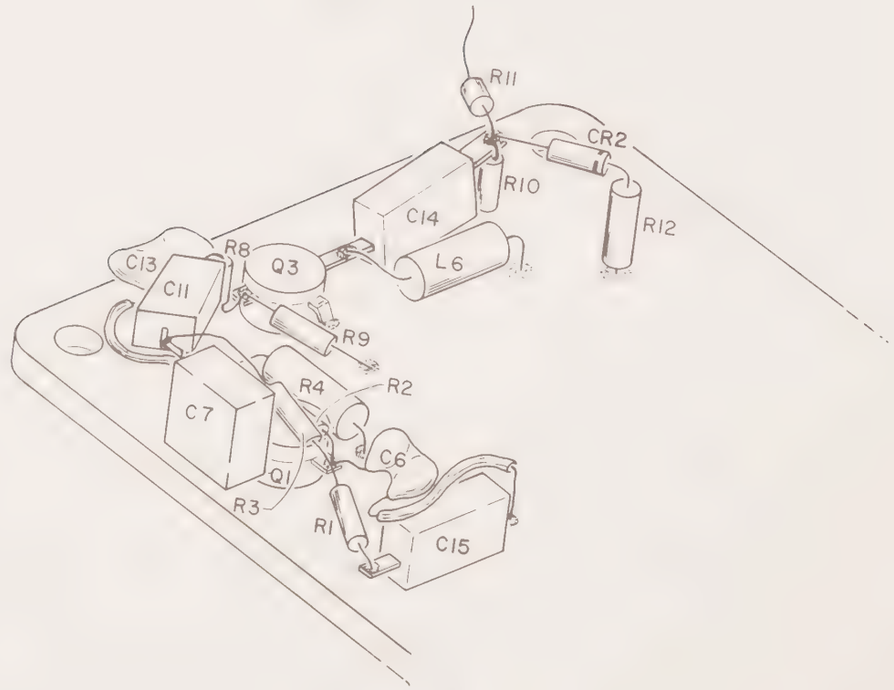


OUTPUT AMPLIFIER BLOCK ENCLOSURE ASSY (7005-5140-500-V)

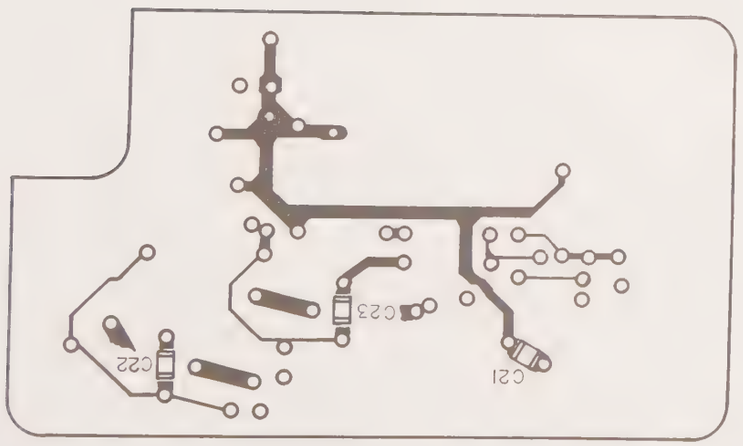




DETAIL **A**



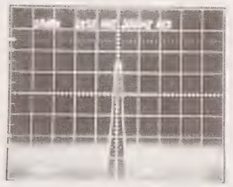
DETAIL **B**



OUTPUT AMPLIFIER PC BOARD ASSY
(7010-5131-500-D6)

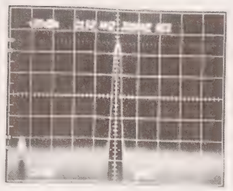
Figure 6-26 Output Amplifier Assembly (Sheet 1 of 2)
(0000-5111-500-D2)

1



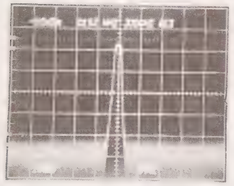
GEN MODE ONLY

2

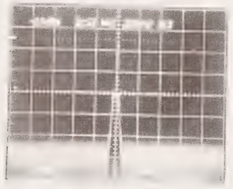


DUPLEX MODE ONLY
(150.2 MHz WITH +2 MHz OFFSET)

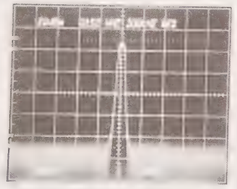
3



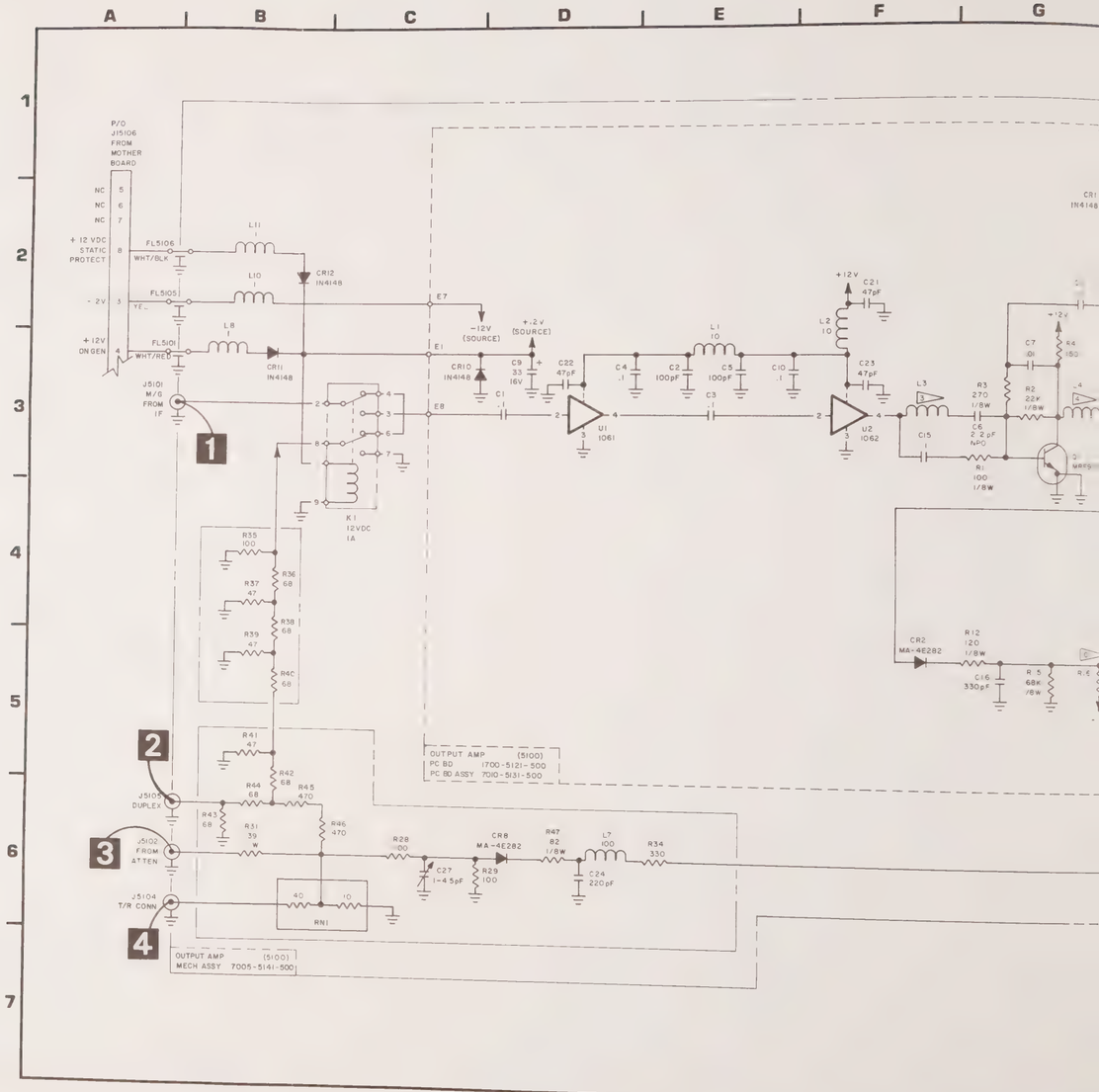
4

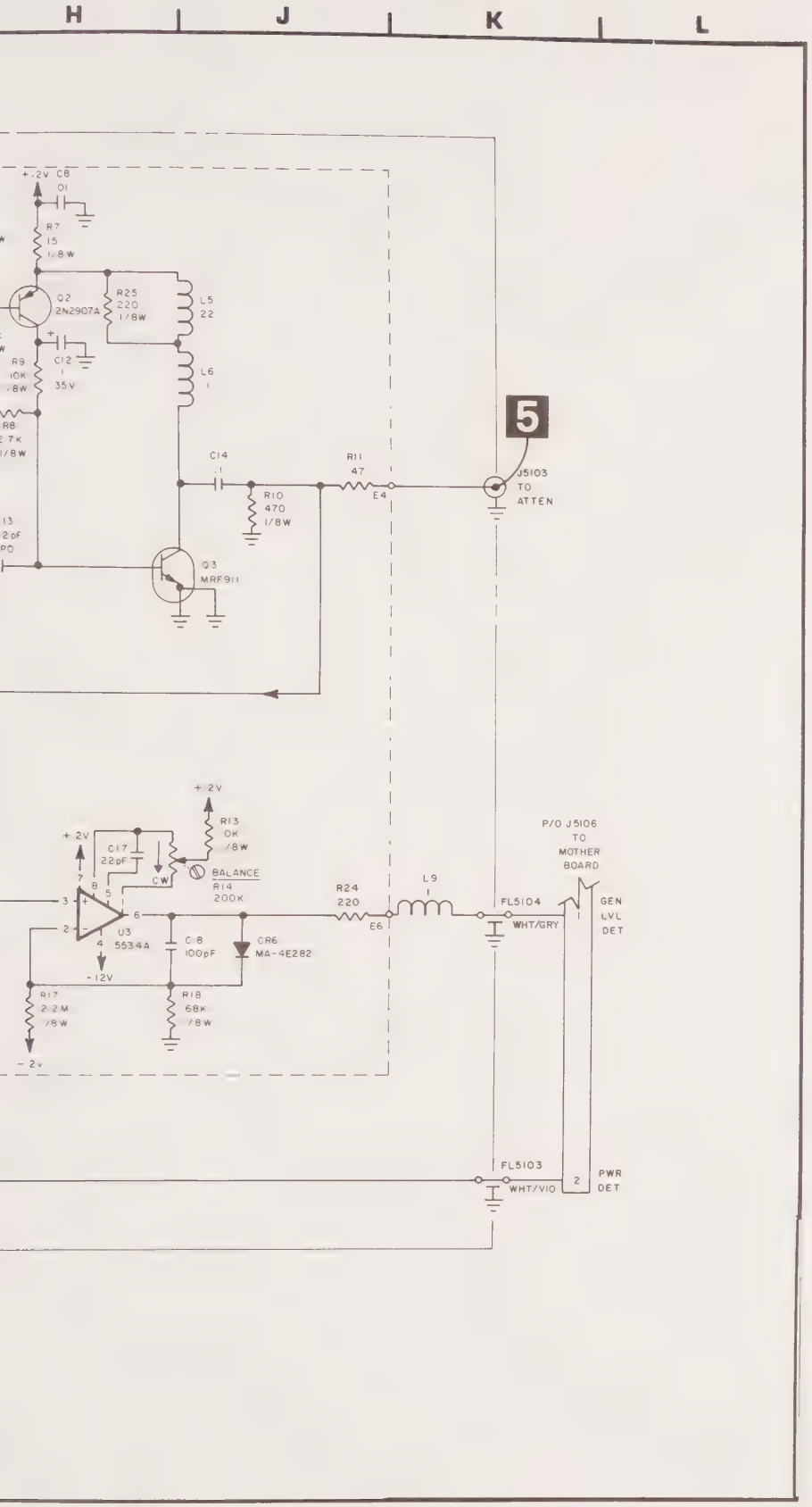


5



NOTE: UNLESS OTHERWISE NOTED, ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S/A IN GEN OR DUP GEN MODE AT A FREQUENCY OF 150.2 MHz @ -50 dBm WITH A +2 MHz OFFSET.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 5000 (I.E., R1 IS R5001).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. L5003 IS FORMED BY THE LEAD OF C5006, CUT TO 0.4" LENGTH.

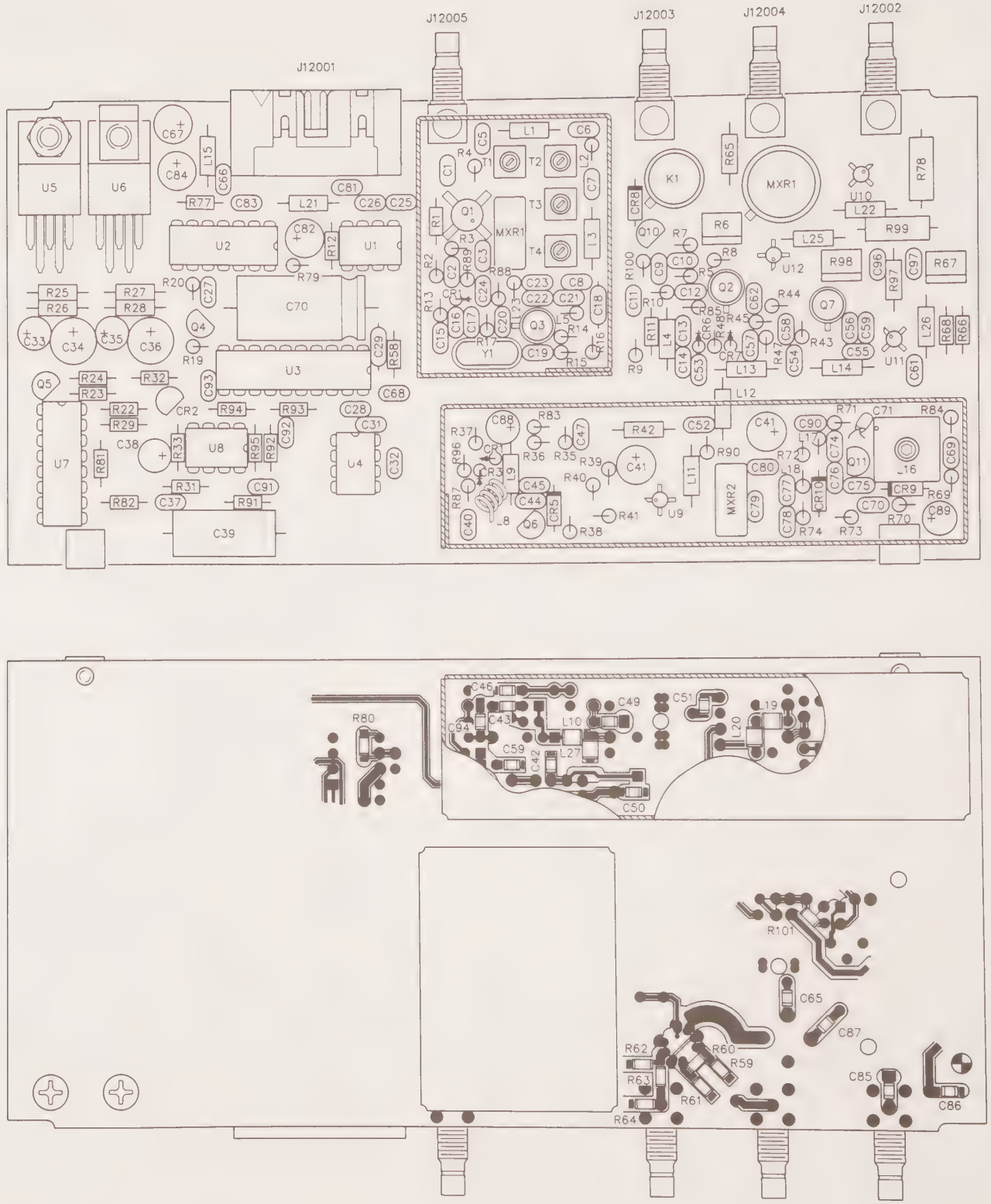
4. L5004 IS FORMED BY THE LEAD OF C5013, CUT TO 0.4" LENGTH.

5. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

6 THRU 9. NOT USED.

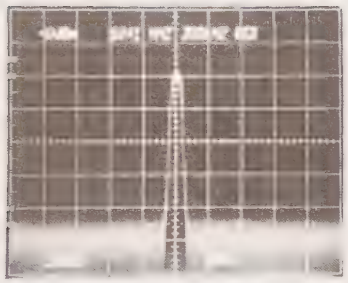
10. R5016 IS SELECTED AT TEST (S.A.T.):
RANGE: 2.2 MΩ TO 2.7 MΩ
NOMINAL: 2.7 MΩ.

Figure 6-26 Output Amplifier Assembly (Sheet 2 of 2) (0000-5111-500-D2)

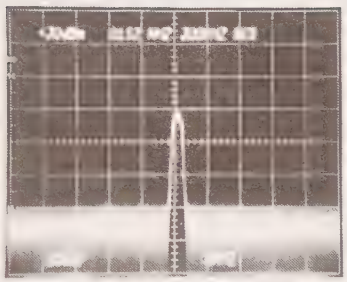


DUPLEX/TRACKING GENERATOR PC BOARD ASSY
(7010-7030-300-E)

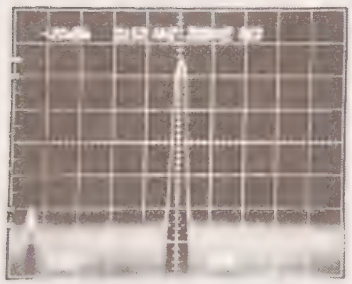
1



2

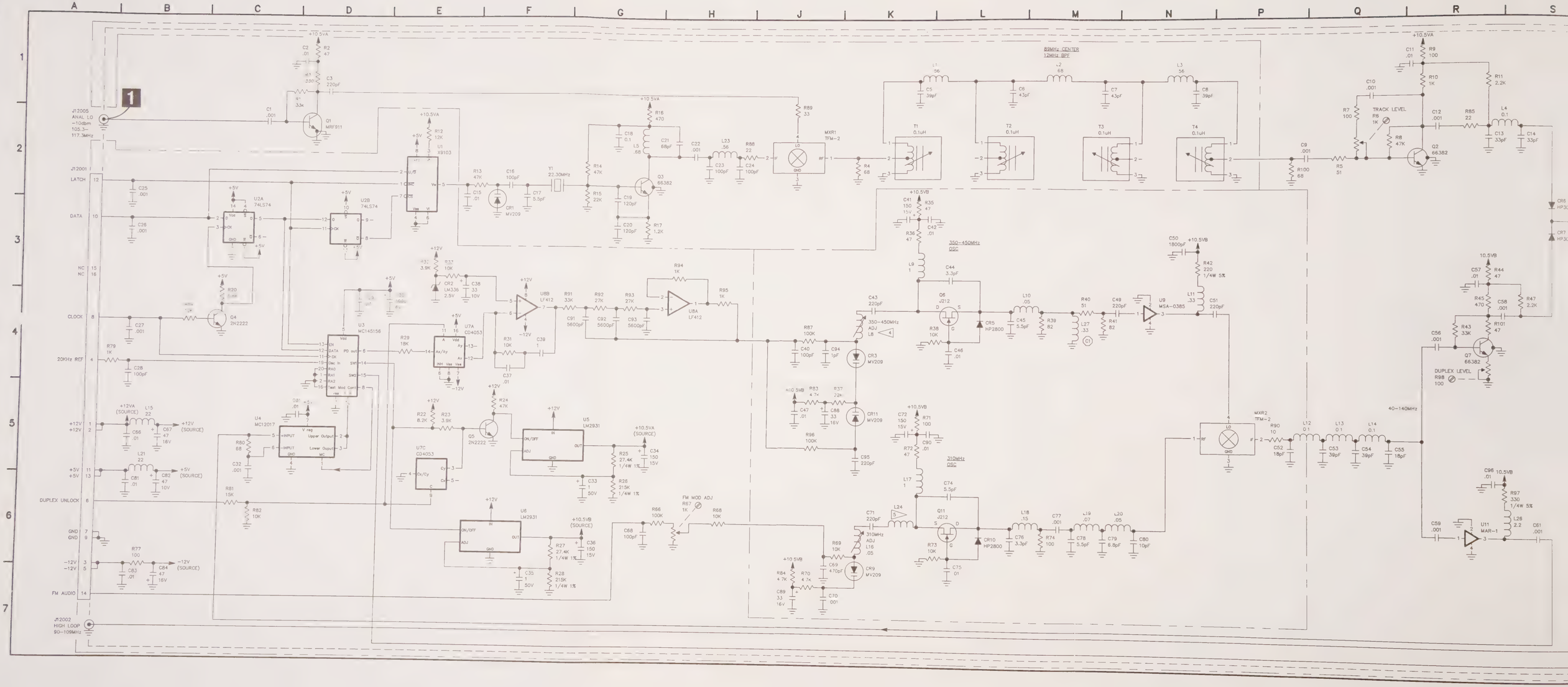


3

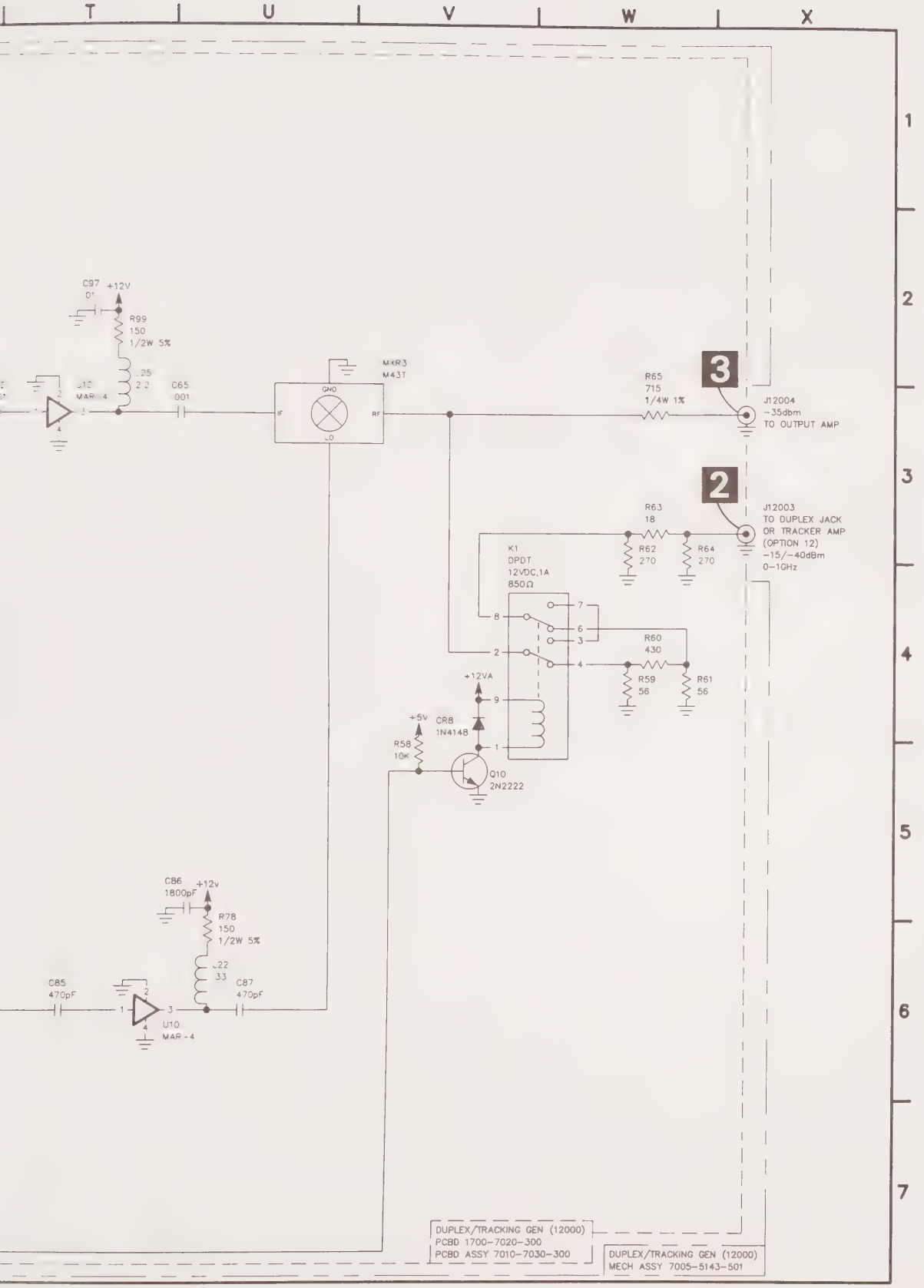


NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz WITH +2 MHz OFFSET IN DUPLEX MODE.

Figure 6-27 Duplex/Tracking Generator PC Board Assembly (FM/AM-1200S) (Sheet 1 of 2) (0000-7010-300-E)



J12005
ANAL LO
-10dbm
105.3-
117.3MHz
J12001
LATCH
DATA
NC
NC
CLOCK
20KHz REF
+12V
+12V
+5V
+5V
DUPLEX UNLOCK
GND
GND
-12V
-12V
FM AUDIO
J12002
HIGH LOOP
90-109MHz
89MHz CENTER
12MHz BPF
350-450MHz
OSC
310MHz
OSC
TRACK LEVEL
DUPLEX LEVEL
40-140MHz
FM MOD ADJ
MXR1
TFM-2
MXR2
TFM-2
U1
X9103
U2A
74LS74
U2B
74LS74
U3
MC145156
U4
MC12017
U5
LM2931
U6
LM2931
U7A
CD4053
U7C
CD4053
U8B
LF412
U8A
LF412
U9
MSA-0385
U11
MAR-1
Q1
MRF911
Q2
66382
Q3
66382
Q4
2N2222
Q5
2N2222
Q6
J212
Q7
66382
Q11
J212
CR1
MV209
CR2
LM336
CR3
MV209
CR5
HP2800
CR9
MV209
CR10
HP2800
CR11
MV209
Y1
22.30MHz



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 12000 (I.E., R1 IS R12001).

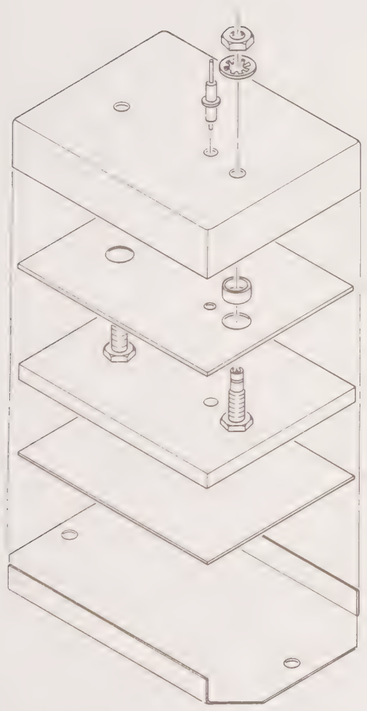
2. ALL RESISTORS ARE 1/8W. 5% TOLERANCE. UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS: ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS. UNLESS OTHERWISE NOTED.

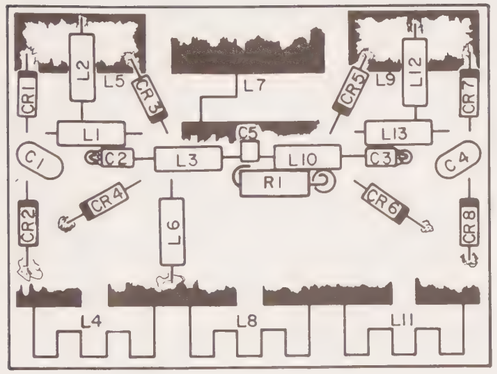
4. L12008 IS FORMED BY 4 TURNS OF 22 GA. WIRE.

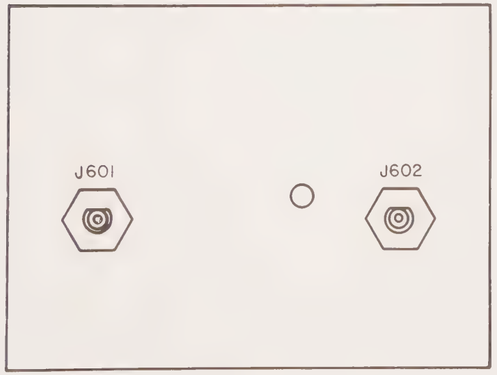
5. L12024 IS FORMED BY TRIMMED .3" LEAD OF C12071.

Figure 6-27 Duplex/Tracking Generator PC Board Assembly (FM/AM-1200S) (Sheet 2 of 2) (0000-7010-300-E)



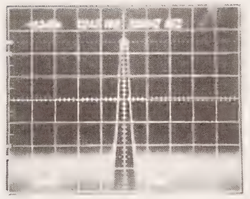
HIGH/LOW-PASS FILTER ASSY
(7005-5040-700-F)



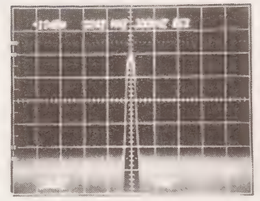


HIGH/LOW-PASS FILTER PC BOARD ASSY
(7010-5030-700-D3)

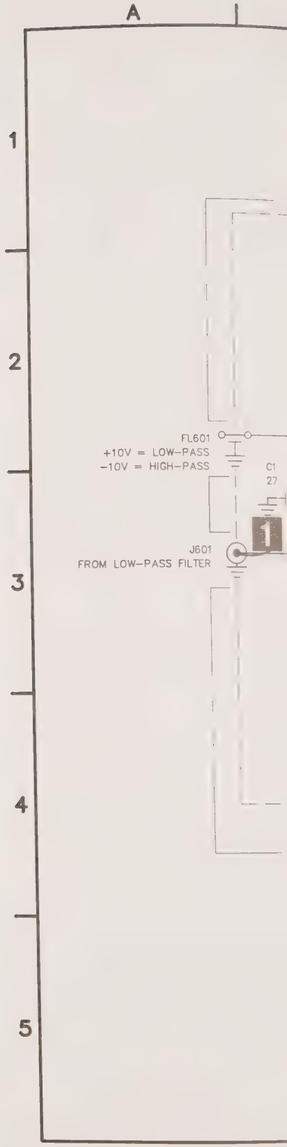
1

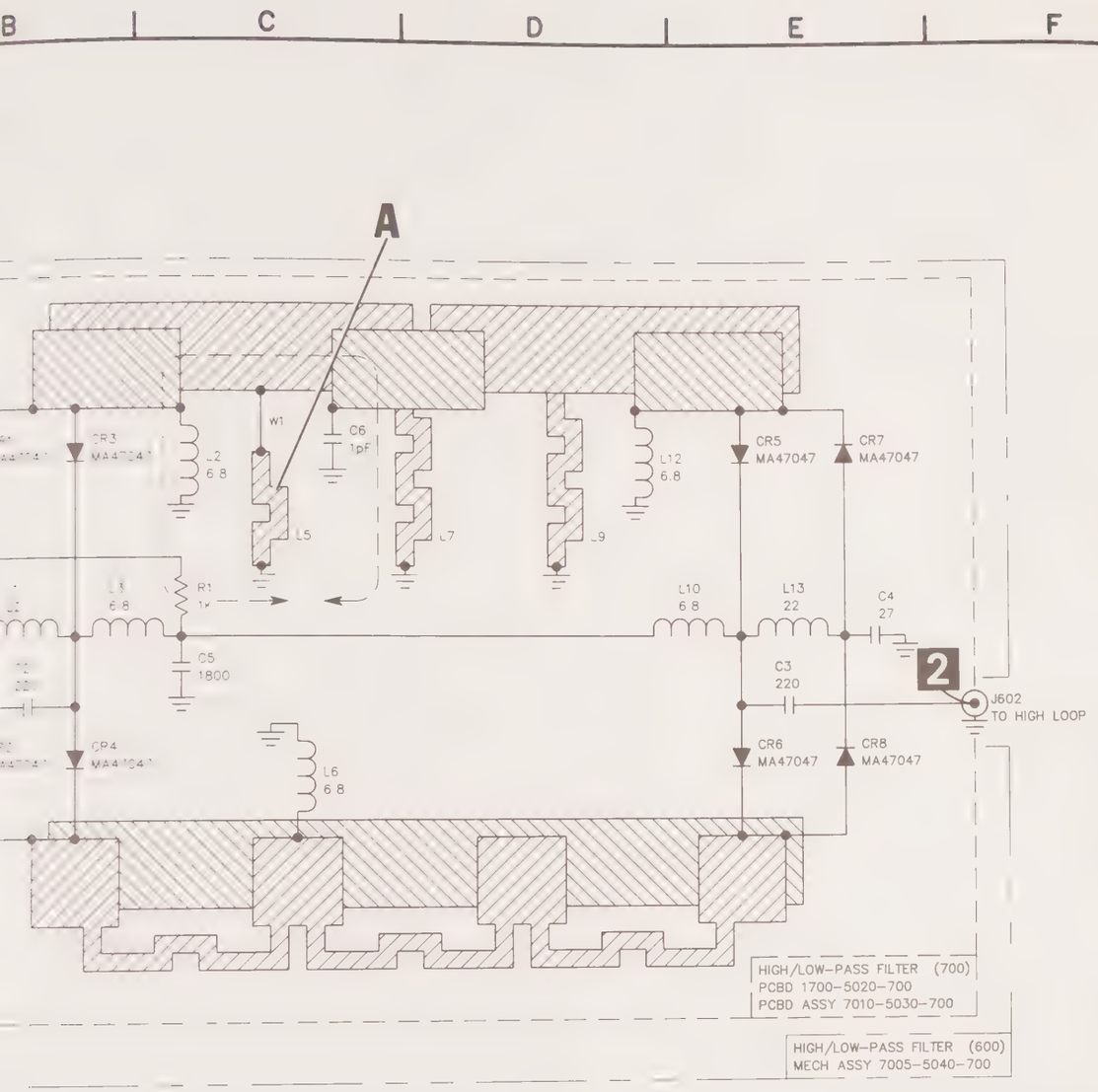


2



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S/A SET AT 150.2 MHz IN RECEIVE MODE WITH NO INPUT SIGNAL.





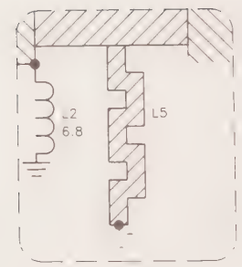
HIGH/LOW-PASS FILTER SCHEMATIC
(0000-5010-700-D)

NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

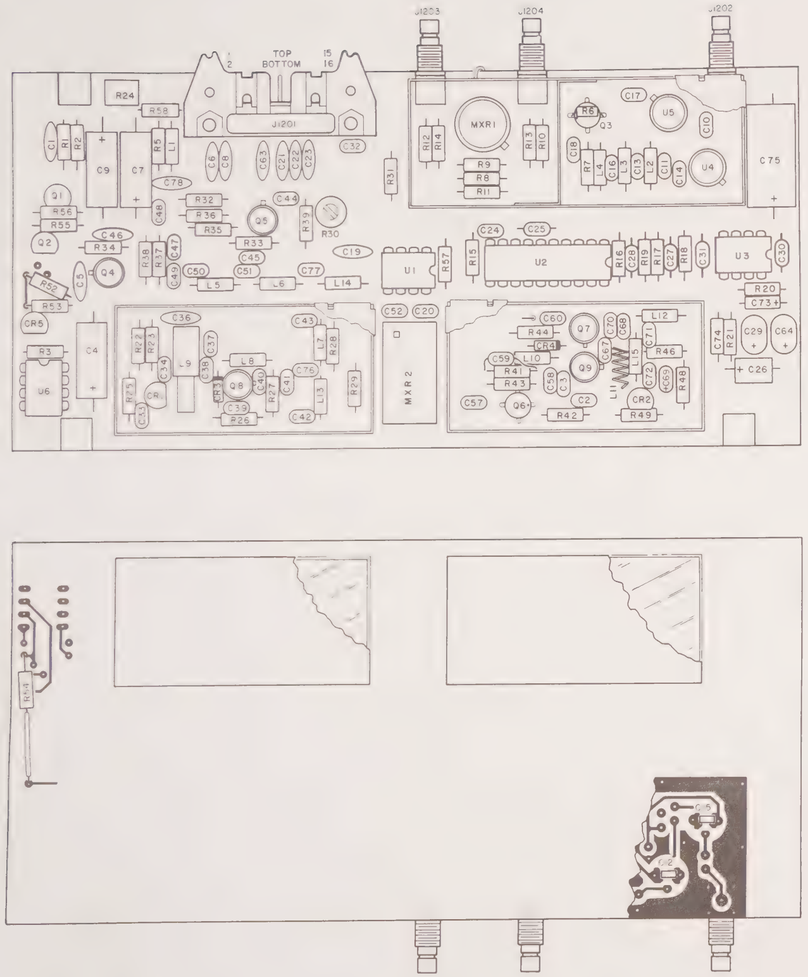
   A. MECH - 600 (I.E., L1 IS L601)
   B. PCB - 700 (I.E., C1 IS C701).

2. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS; ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.



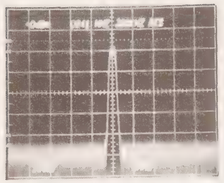
DETAIL **A**

Figure 6-28 High/Low-Pass Filter Assembly
(0000-5010-700-D)

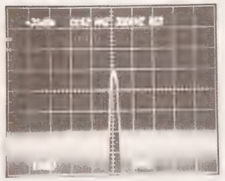


DUPLEX PC BOARD ASSY
(7010-5131-00-G8)

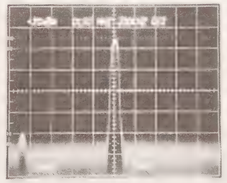
1



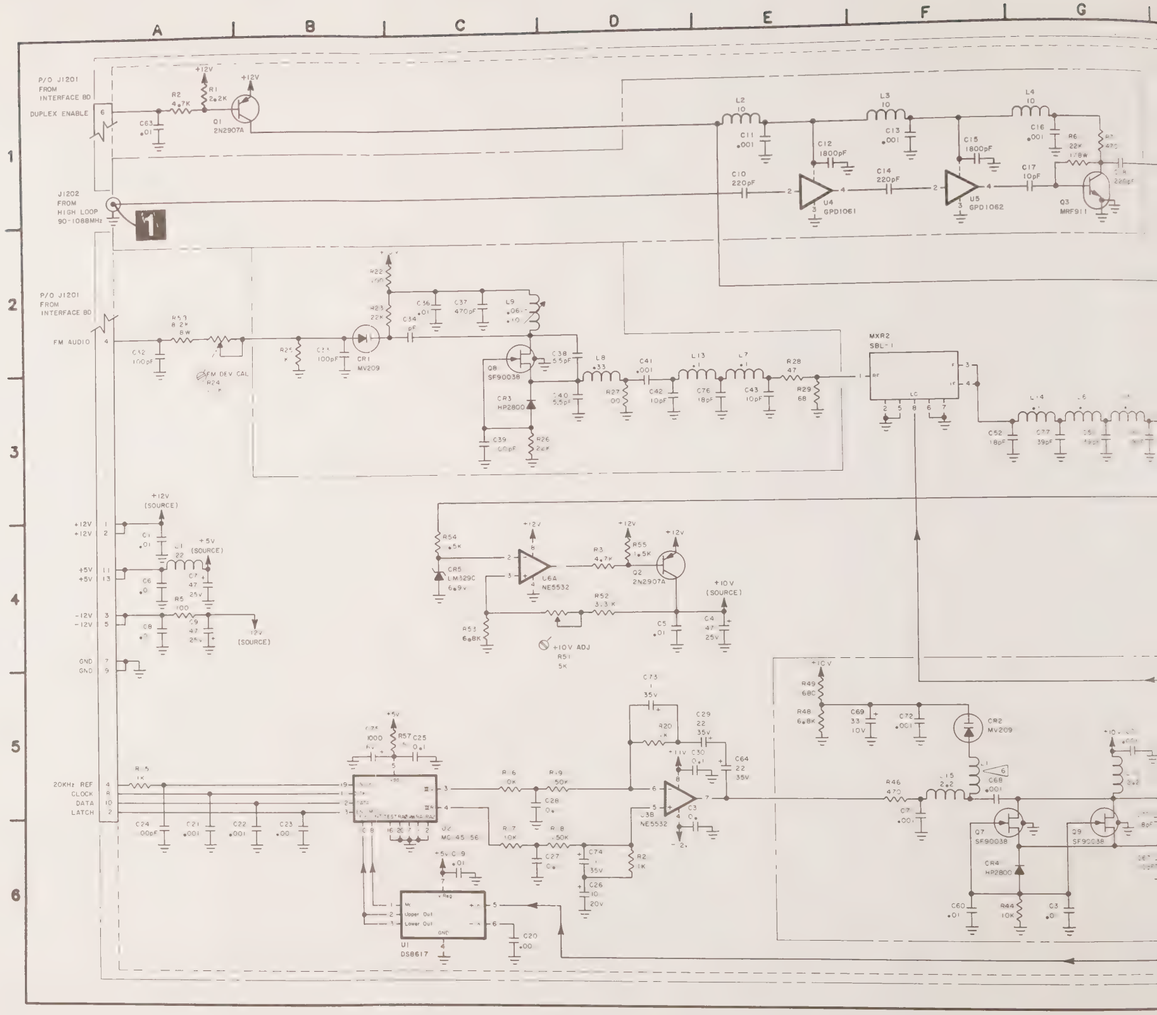
2

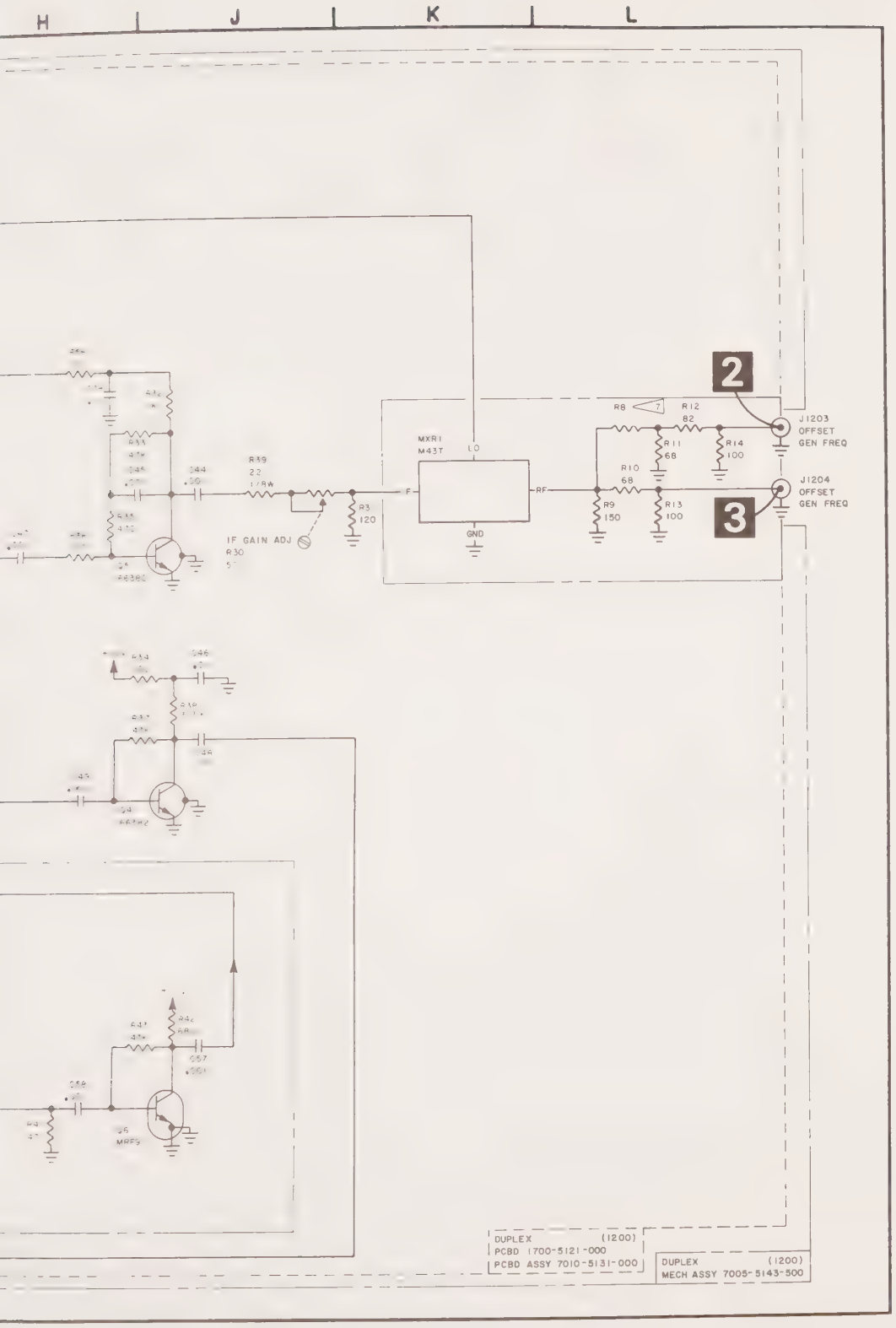


3



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200A SET AT 150.2 MHz WITH +2 MHz OFFSET IN DUPLEX MODE.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 1200 (I.E., R1 IS R1201).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

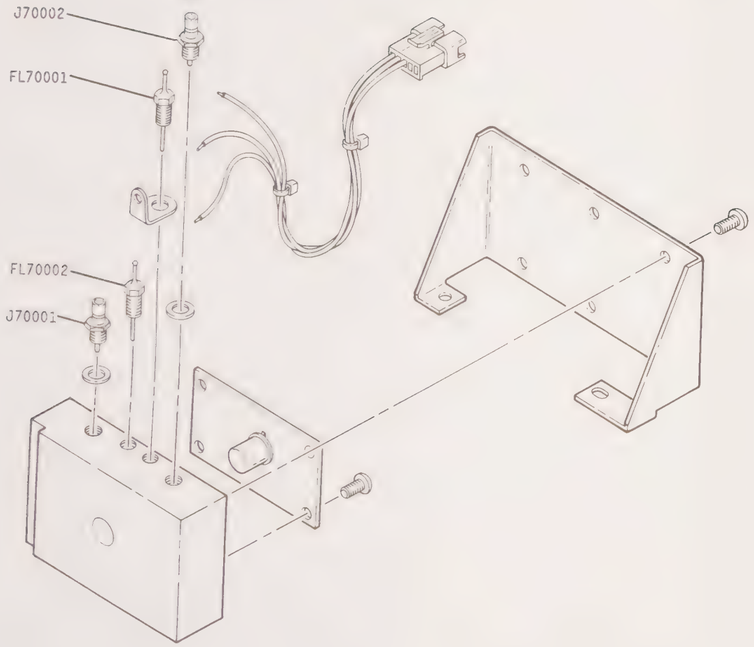
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4, 5. NOT USED.

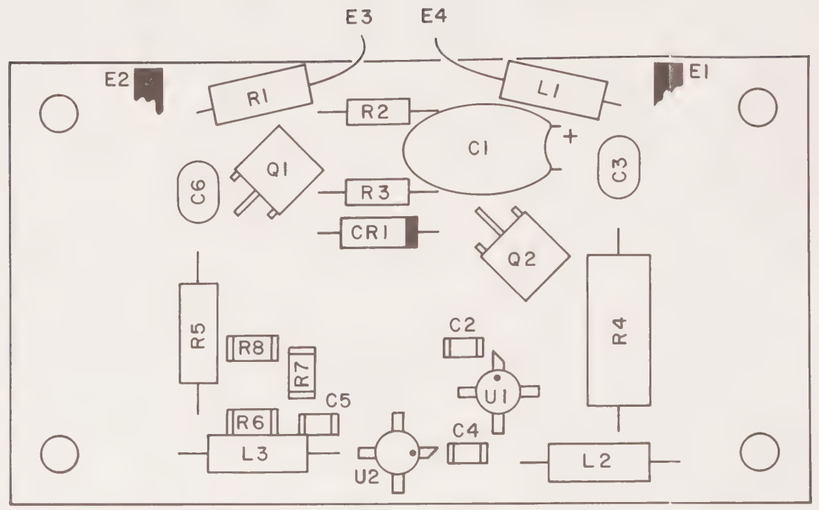
6. L1211 IS FORMED BY 2.4" LENGTH, 24 GA. WIRE, WRAPPED 4 TURNS.

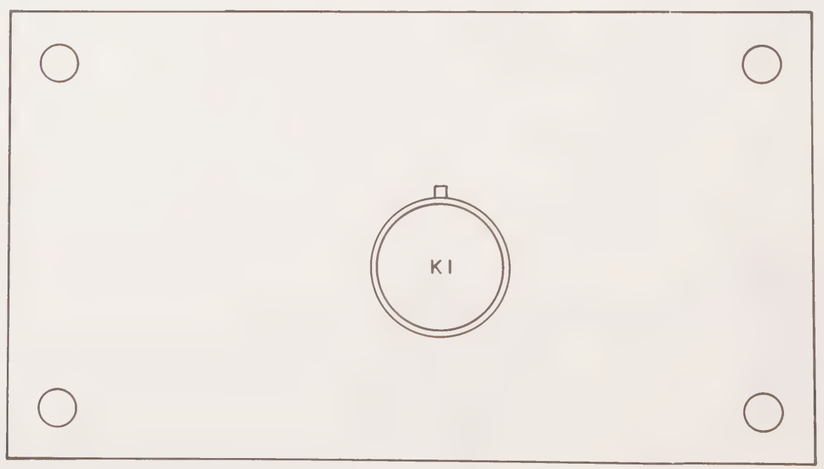
7. R1208 IS SELECTED AT TEST (S.A.T.):
RANGE: 820Ω TO 2.7KΩ
NOMINAL: 1.8KΩ

Figure 6-29 Duplex PC Board Assembly (FM/AM-1200A) (0000-5111-000-H)

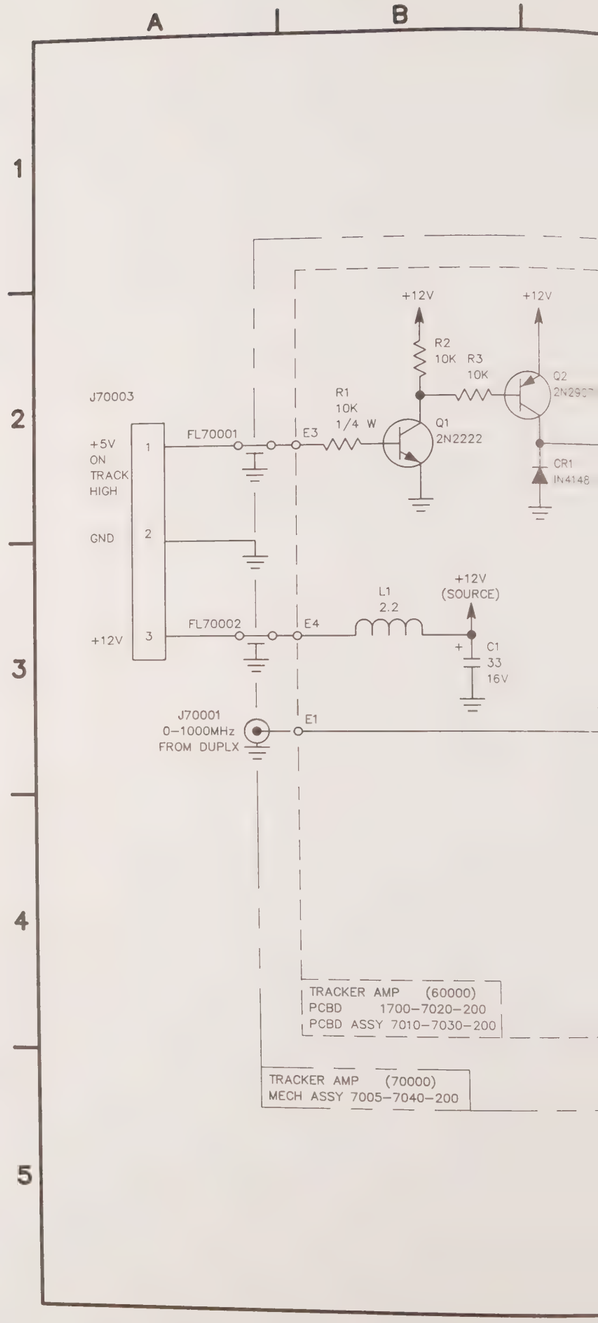


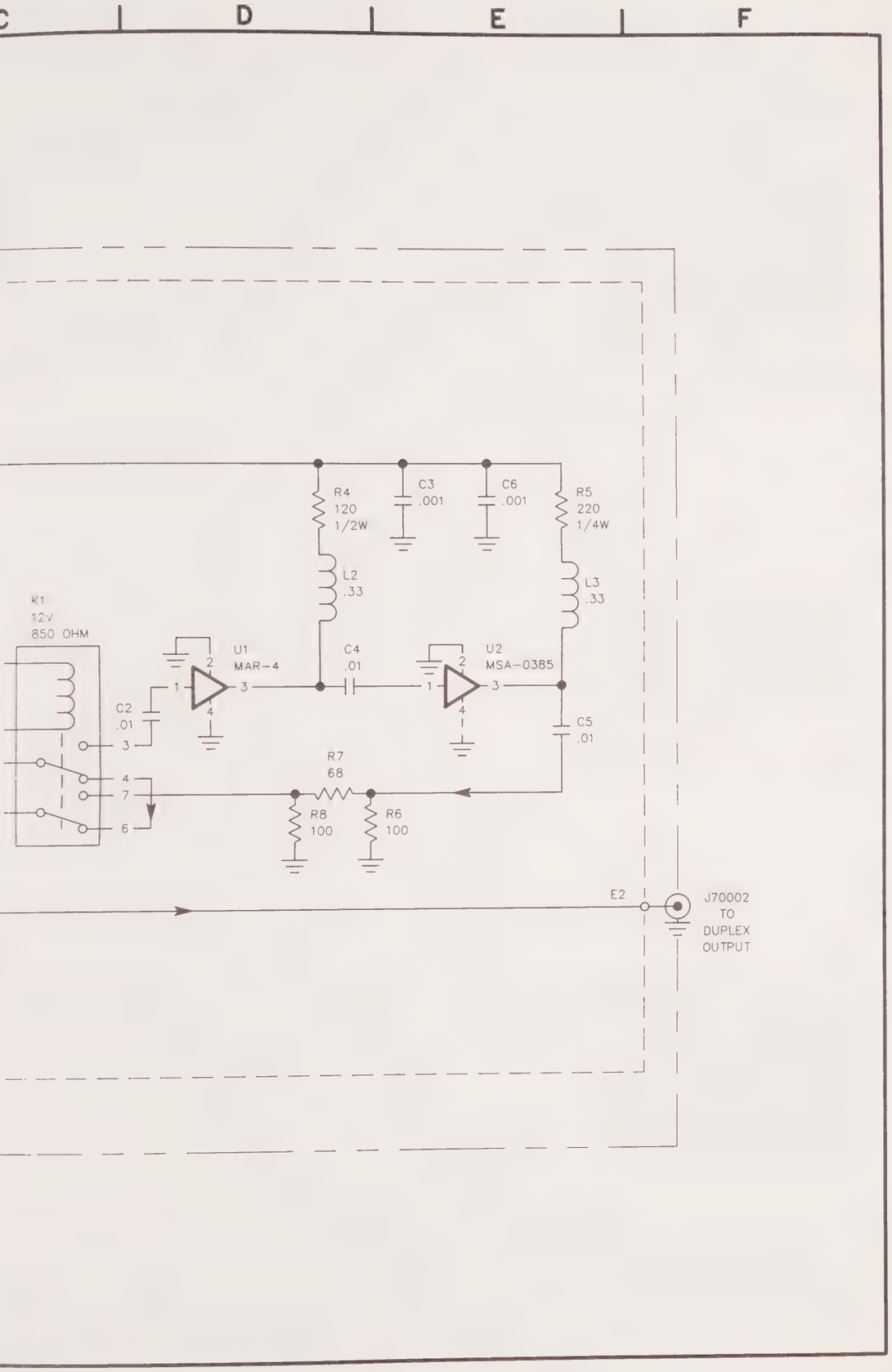
TRACKER AMP ASSY
(7005-7040-200-B)





TRACKER AMP PC BOARD ASSY
(7010-7030-200-B2)





NOTES:

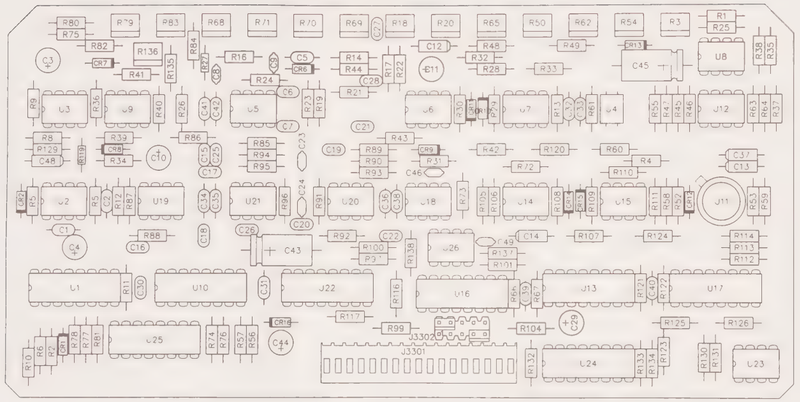
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. ASS'Y - 70000 (I.E., R1 IS R70001).
   B. PCB - 60000 (I.E., R1 IS 60001).

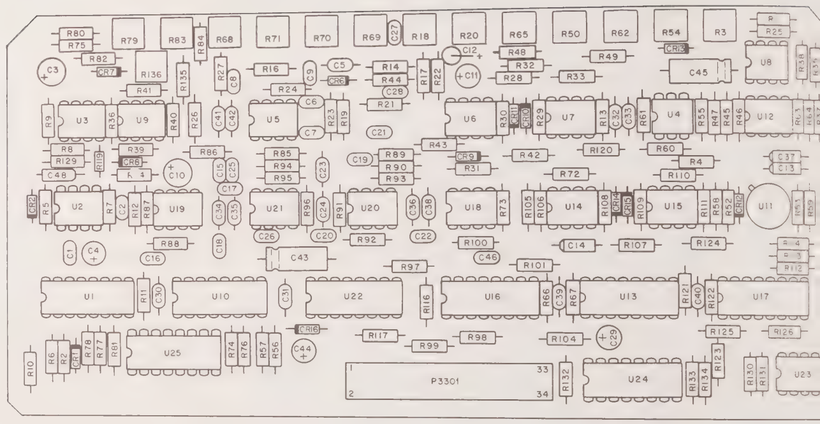
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-30 Tracking Amplifier Assembly (7010-7030-200-B2)



RECEIVE AUDIO PC BOARD ASSY (FM/AM-1200S)
(7010-7730-200-B1)

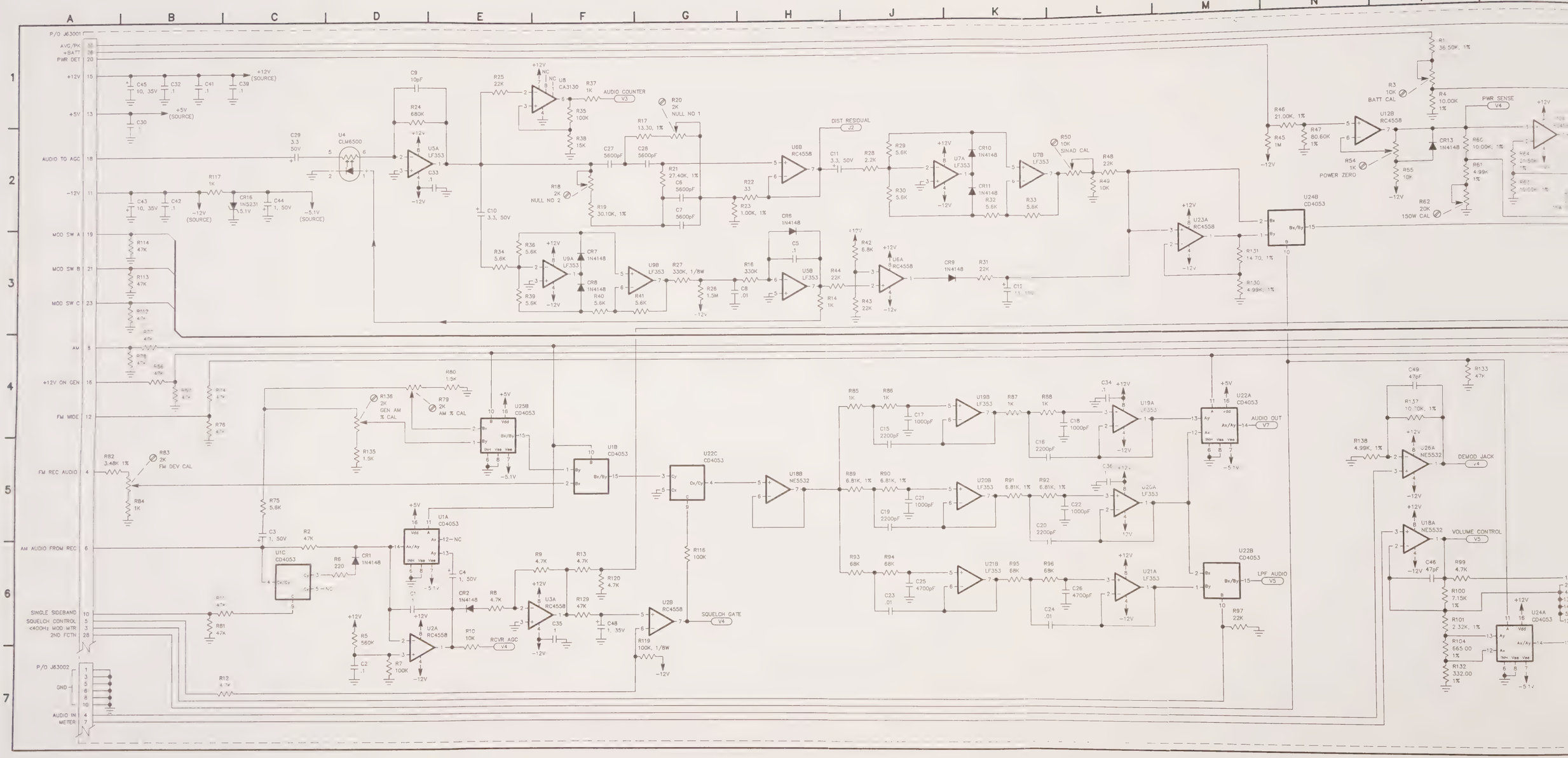


RECEIVE AUDIO PC BOARD ASSY (FM/AM-1200A)
(7010-5233-301-E8)

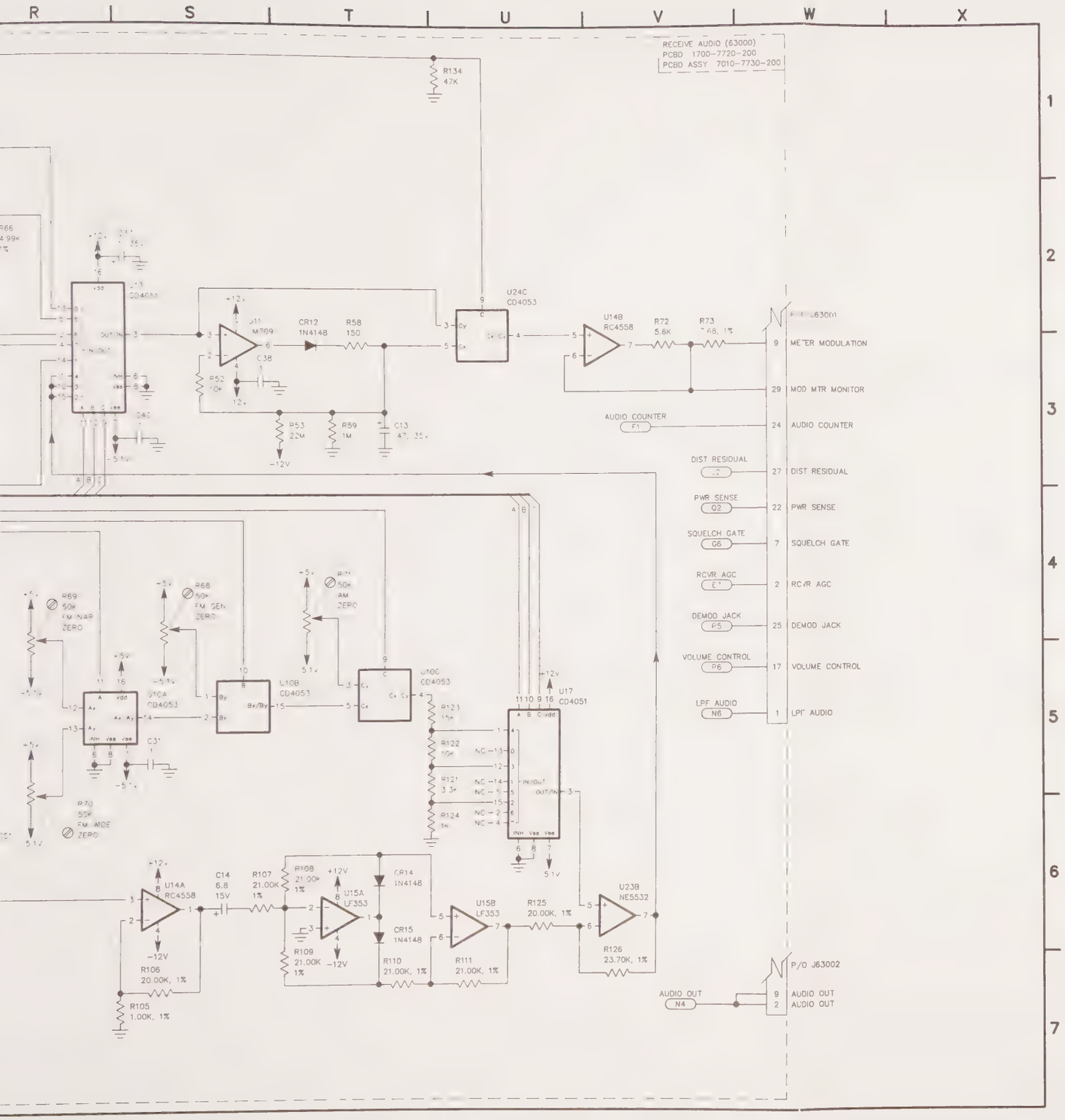
METER SELECT CODING													
J3301		S3704 MODULATION METER CONTROL POSITION											
		kHz/%X10				BATT TEST	SIG	DIST	SINAD	WP		WA	
PIN #	IDENTIFIER	2	6	20	60					150	15	150	15
19	MOD MTR A	0	1	0	0	0	1	1	1	0	1	0	1
21	MOD MTR B	0	1	1	1	0	0	1	1	1	0	1	0
23	MOD MTR C	1	0	0	0	0	0	1	1	1	1	1	1
28	2ND FUNCT	0	0	0	1	0	0	1	0	0	0	0	0
30	AVG/PEAK	0	0	0	0	0	0	1	1	0	0	1	1
1 = +12 VDC 0 = 0 VDC													

J3301	REMARKS
PIN 3	+5 VDC WHEN FUNCTION GENERATOR IS SET ON ANY TONE BELOW 409.6 Hz
PIN 8	+12 VDC ON SSB AND ALL AM MODES
PIN 12	+12 VDC ON FM WIDE ONLY

Figure 6-31 Receive Audio PC Board Assembly (0000-7710-200-C) (Sheet 1 of 3)



RECEIVE AUDIO SCHEMATIC (FM/AM-1200S) (0000-7710-200-C)



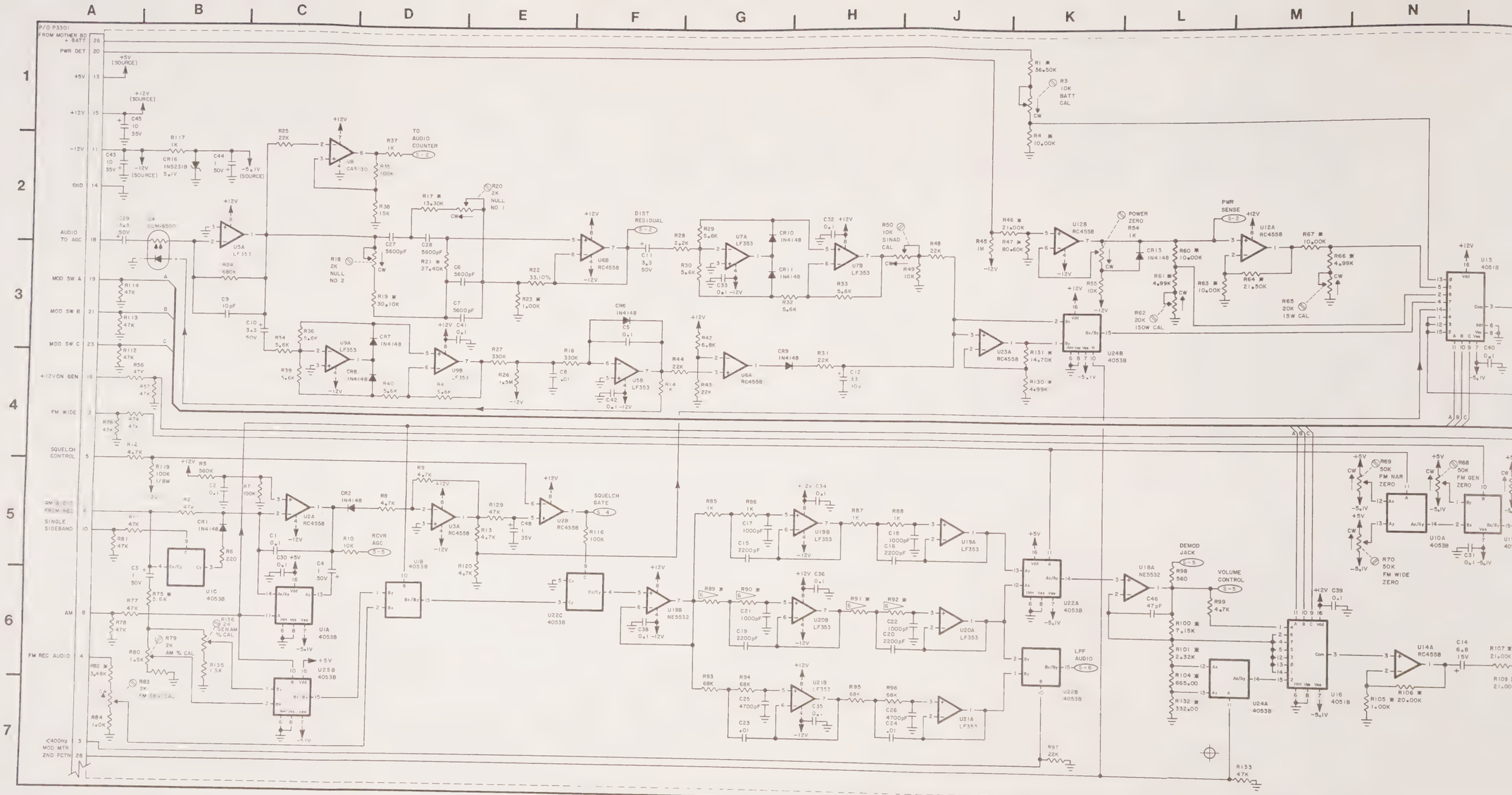
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 63000 (I.E., R1 IS R63001).

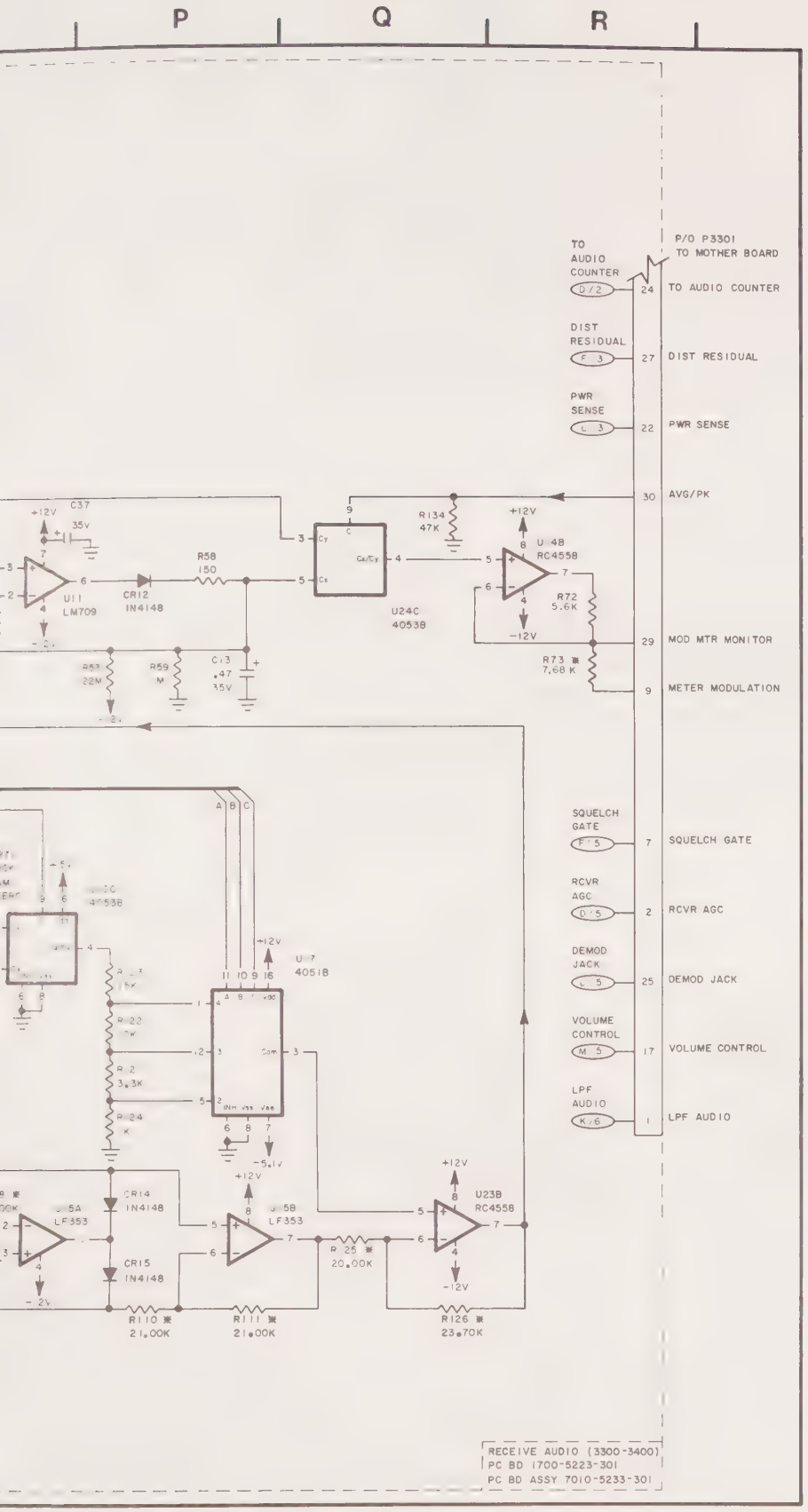
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-31 Receive Audio PC Board Assembly (0000-7710-200-C) (Sheet 2 of 3)



RECEIVE AUDIO SCHEMATIC (FM/AM-1200A) (0000-5213-301-E5)



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3300 AND 3400 (I.E., R1 IS R3301. R101 IS R3401).

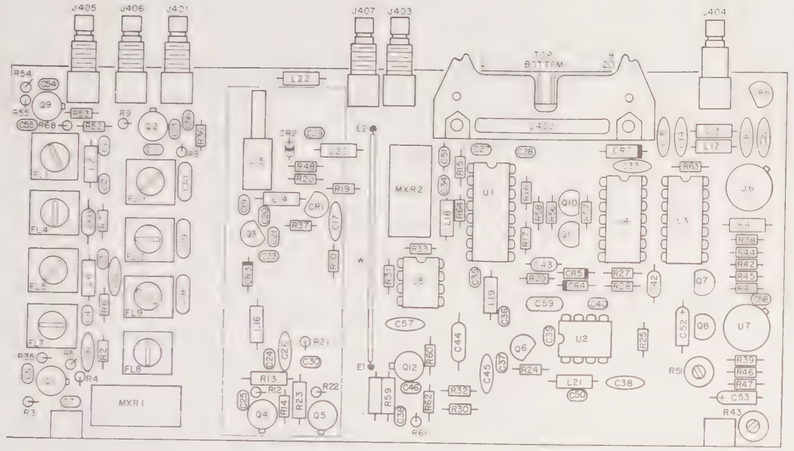
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

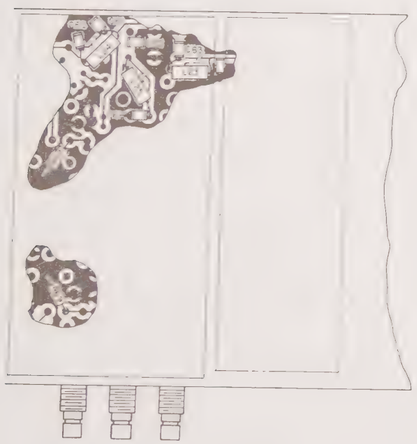
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

4,5. NOT USED.

6. R3389 THRU R3392 ARE 11.5KΩ

Figure 6-31 Receive Audio PC Board Assembly (0000-7710-200-C) (Sheet 3 of 3)



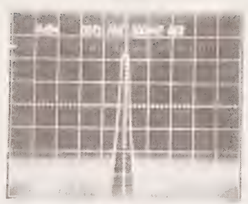


ANALYZER RF PC BOARD ASSY
(7010-5130-401-A9)

1

REC MODE

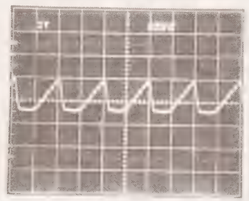
1



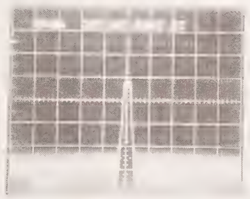
GEN MODE

2

3

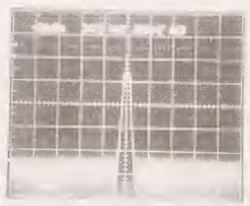


4



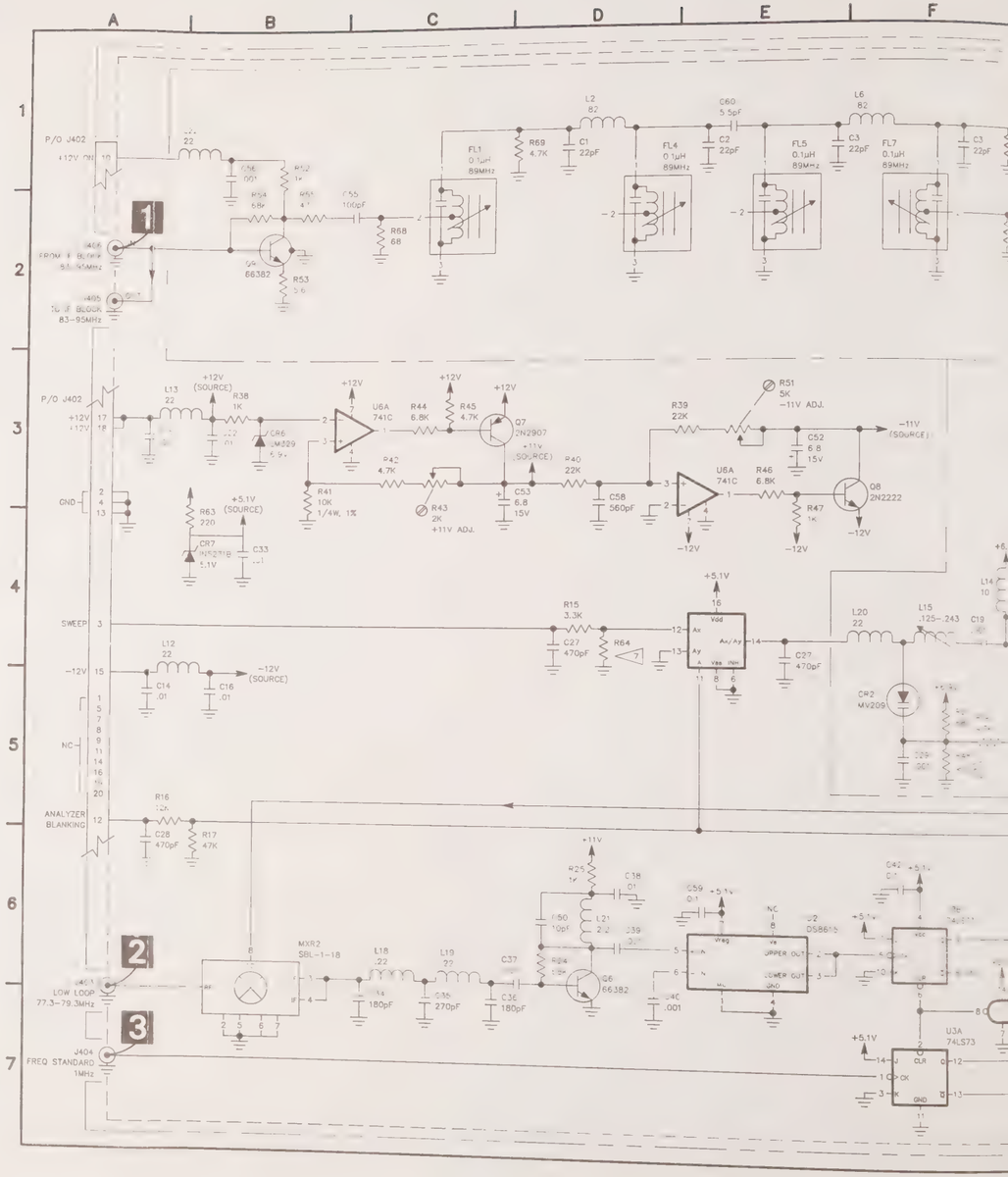
GEN MODE

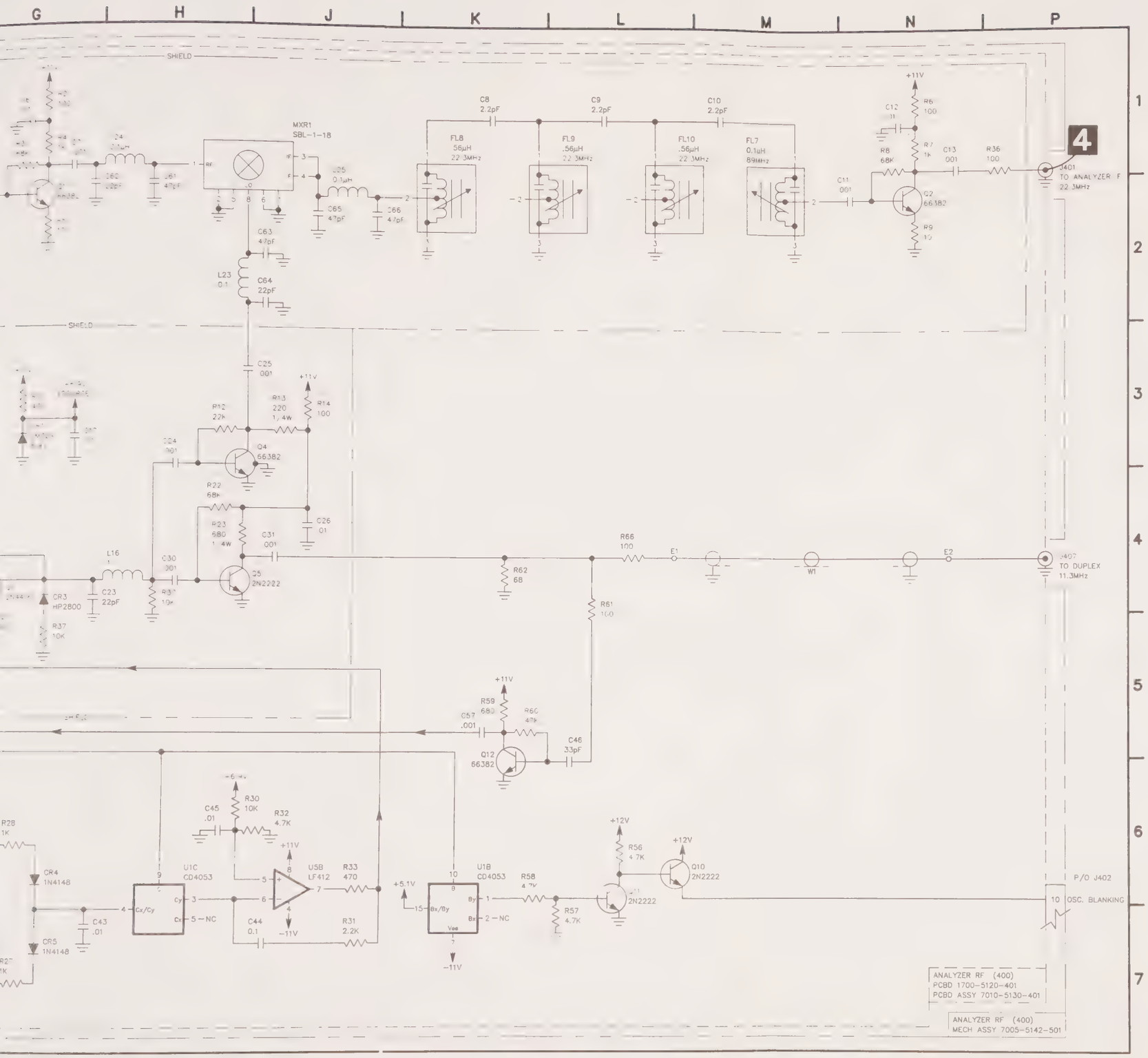
4



REC MODE

NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X10 PROBE, UNLESS OTHERWISE NOTED.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 400 (I.E., R1 IS R401).

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

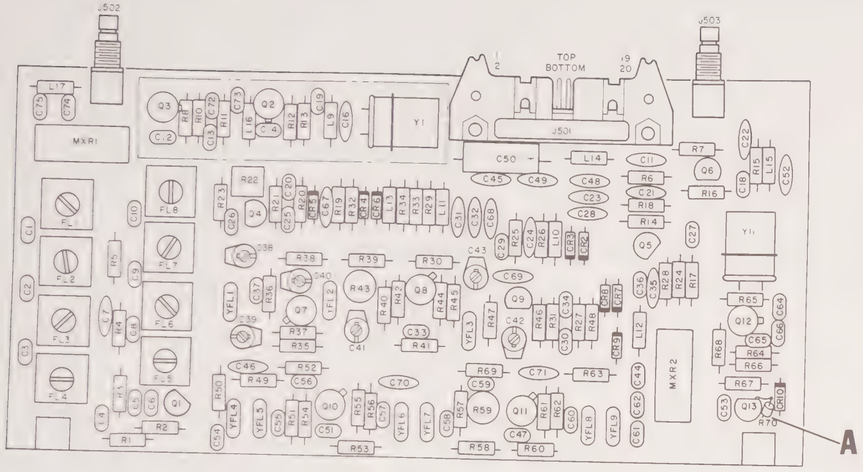
4,5. NOT USED.

6. R448 IS SELECTED AT TEST (S.A.T):
RANGE: 820KΩ TO 2.2KΩ
NOMINAL: 1.8KΩ

7. R464 IS SELECTED AT TEST (S.A.T):
RANGE: 1.0KΩ TO 2.2KΩ
NOMINAL: 1.2KΩ

HORIZONTAL SWEEP SELECTOR POSITION	PIN #		
	5	7	9
1 kHz/DIV	1	0	0
2 kHz/DIV	1	0	0
5 kHz/DIV	0	1	0
10 kHz/DIV	0	1	0
20 kHz/DIV	0	1	0
50 kHz/DIV	0	0	1
.1 MHz/DIV	0	0	1
.2 MHz/DIV	0	0	1
.5 MHz/DIV	0	0	1
1 MHz/DIV	0	0	1
1 = +12 VDC		0 = 0 VDC	

Figure 6-32 Analyzer RF PC Board Assembly (0000-5110-401-A4) (FM/AM-1200S ONLY)



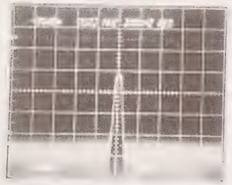
ANALYZER IF PC BOARD ASSEMBLY (7010-5130-500-ES)

DETAIL **A**

1

REC MODE

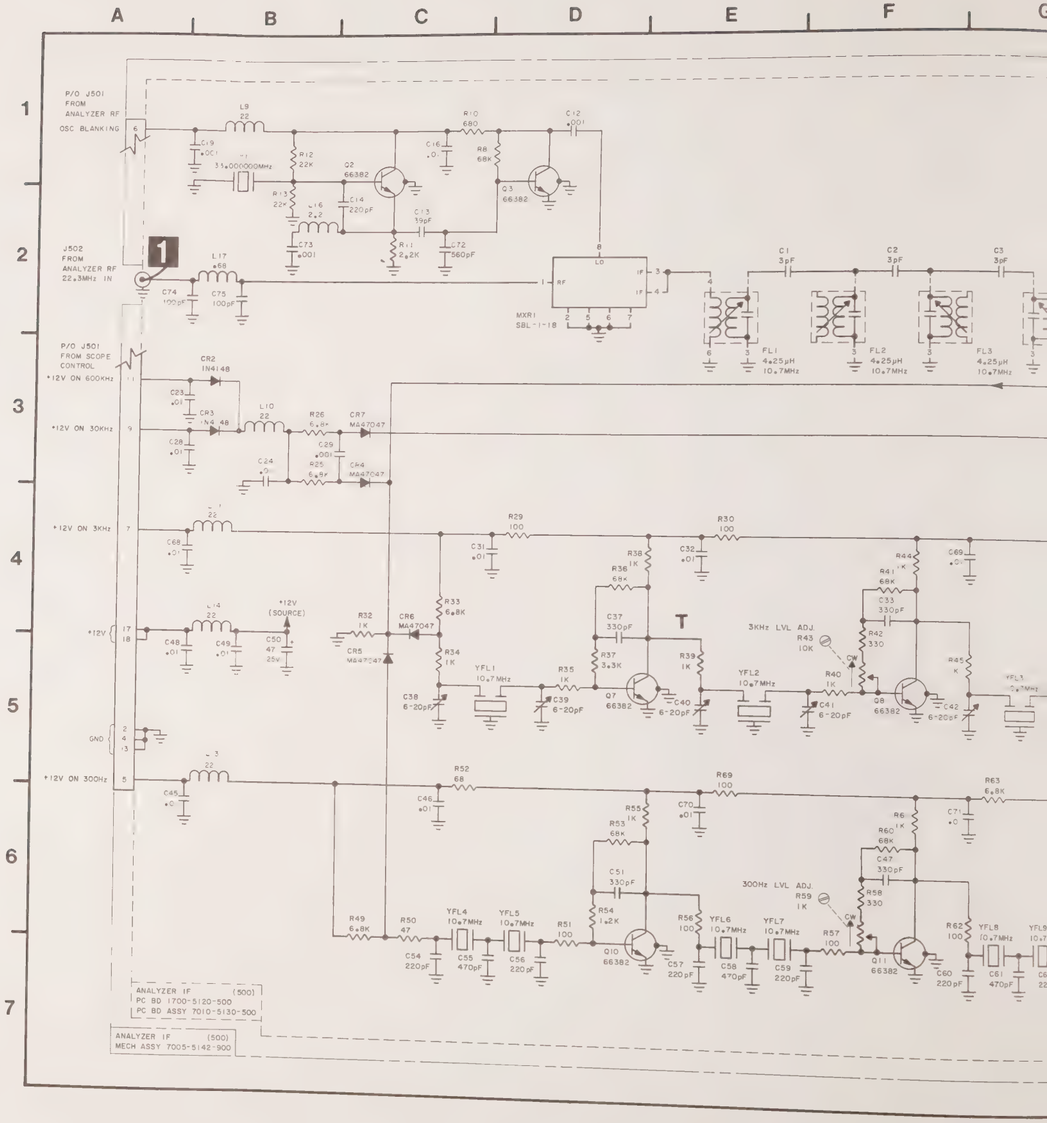
1

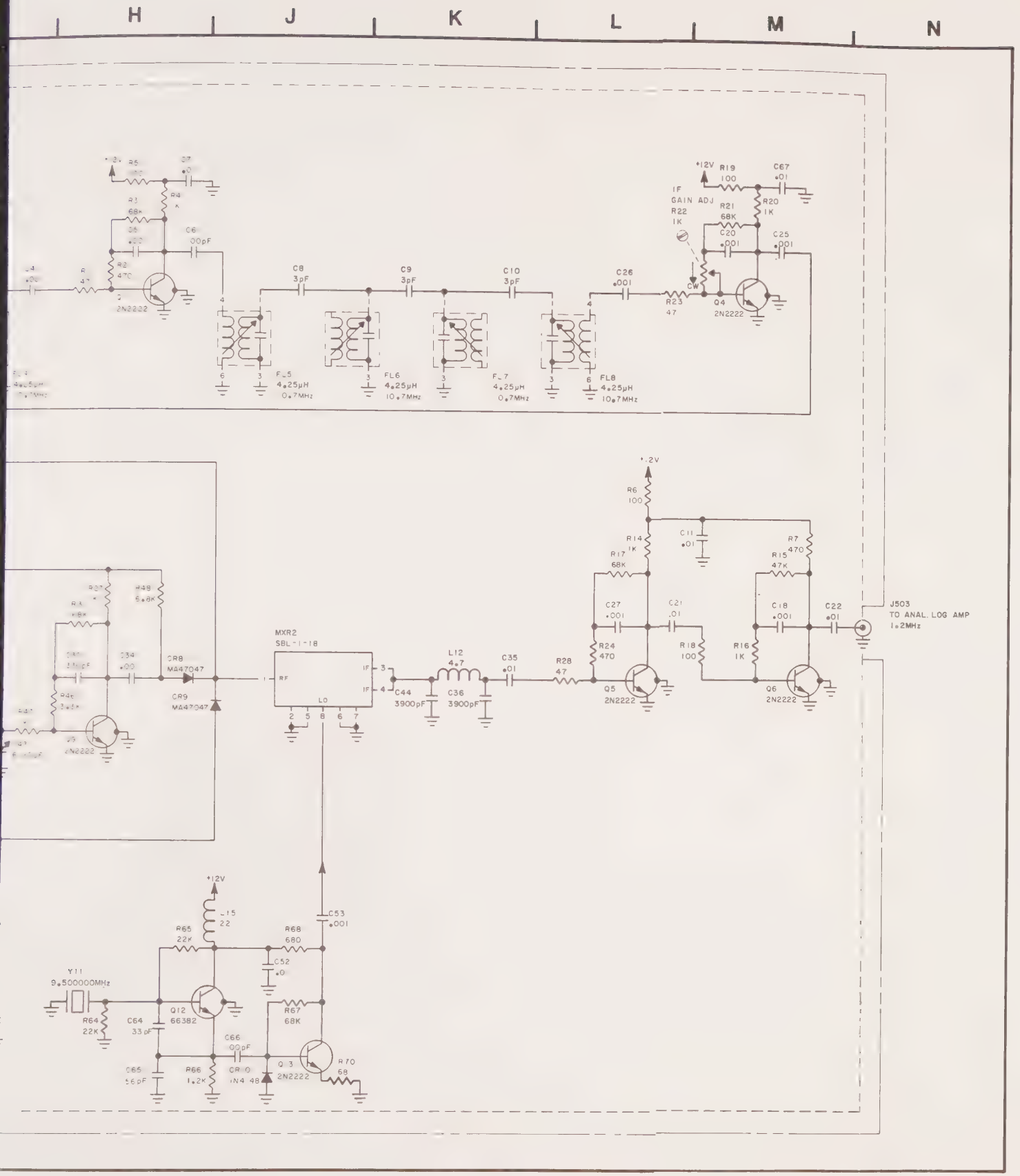


GEN MODE

NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200S SET AT 150.2 MHz AND NO INPUT SIGNAL IN RECEIVE MODE USING AN X10 PROBE, UNLESS OTHERWISE NOTED.

HORIZONTAL SWEEP SELECTOR POSITION	PIN #		
	5	7	9
1 kHz/DIV	1	0	0
2 kHz/DIV	1	0	0
5 kHz/DIV	0	1	0
10 kHz/DIV	0	1	0
20 kHz/DIV	0	1	0
50 kHz/DIV	0	0	1
.1 MHz/DIV	0	0	1
.2 MHz/DIV	0	0	1
.5 MHz/DIV	0	0	1
1 MHz/DIV	0	0	1
1 = +12 VDC 0 = 0 VDC			





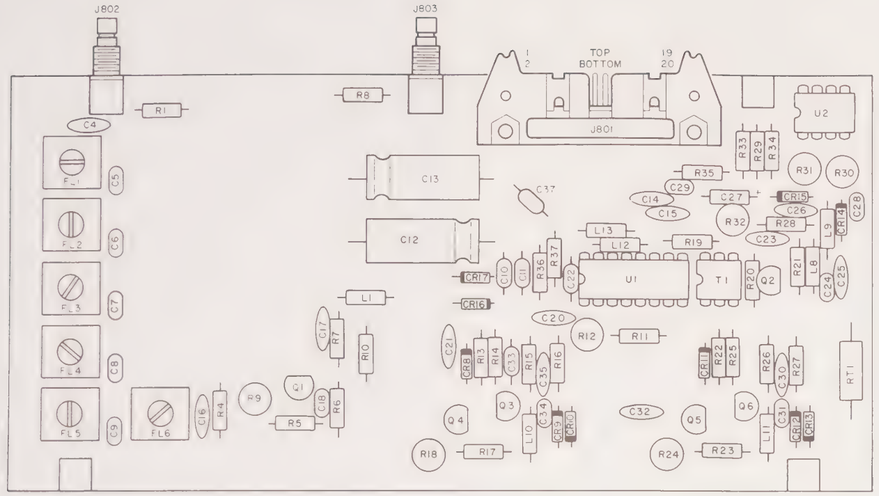
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 500 (I.E., R1 IS R501).

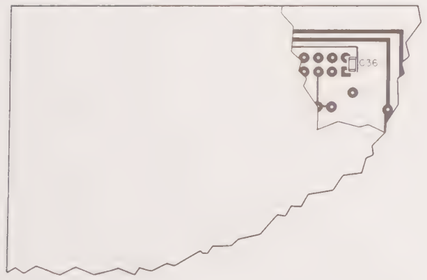
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-33 Analyzer IF PC Board Assembly (0000-5110-500-E3)
(FM/AM-1200S ONLY)

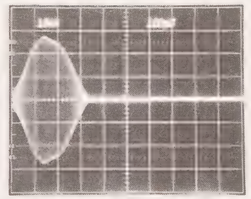


ANALYZER LOG AMP PC BOARD ASSY
(7010-5130-600-C)

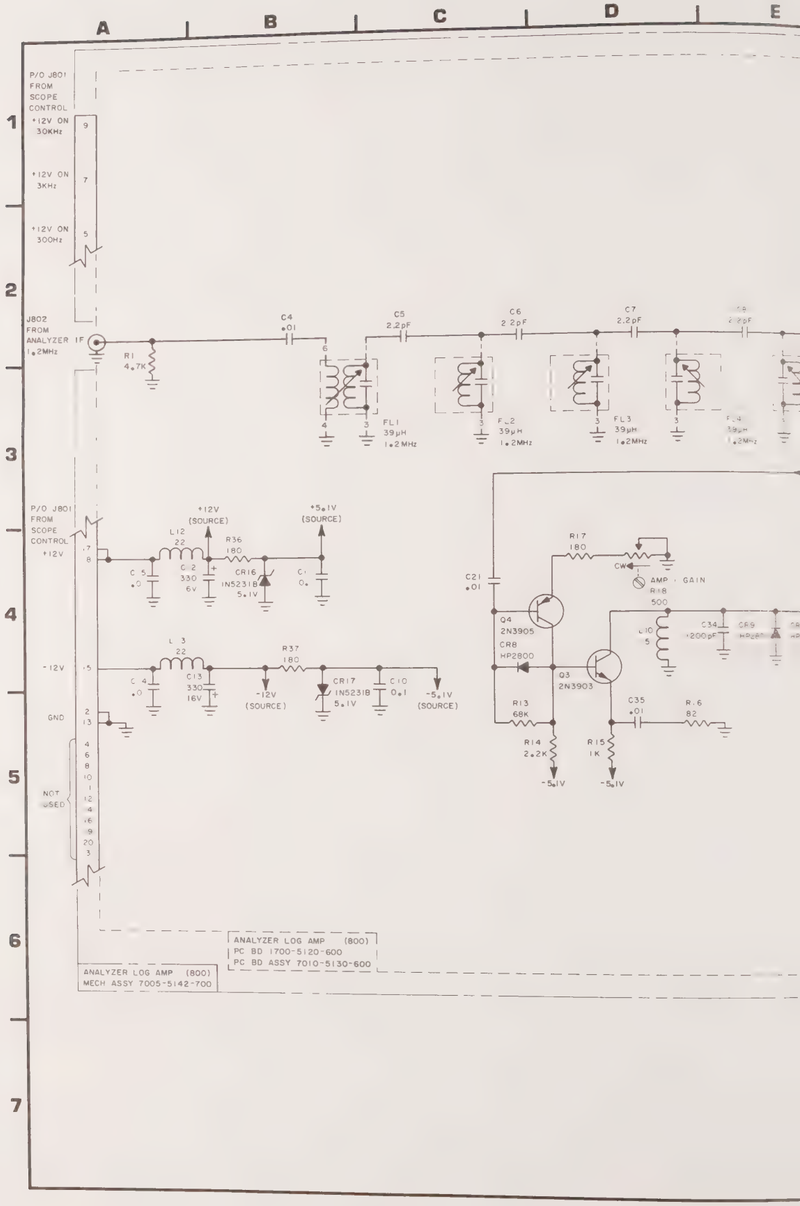


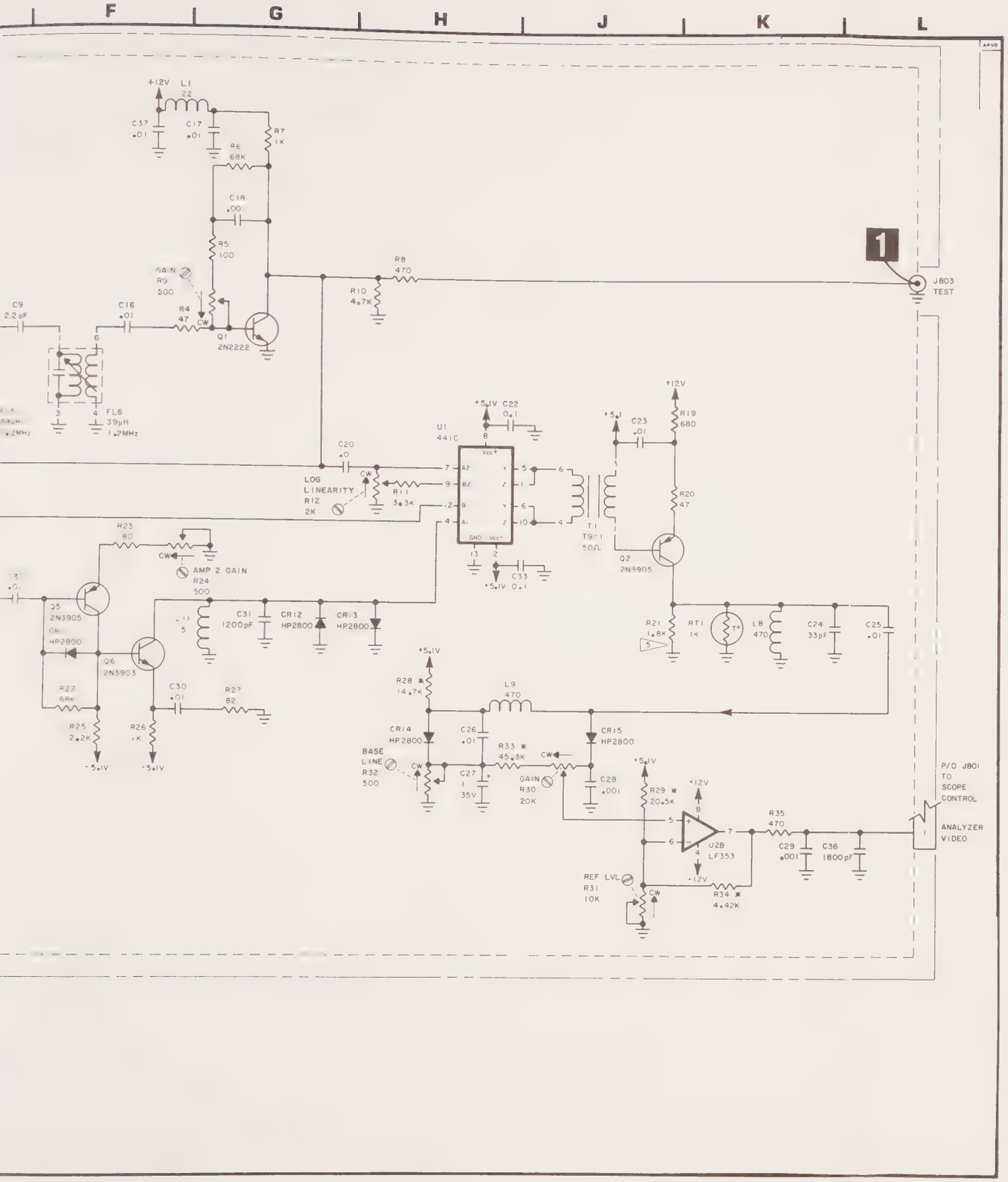
HORIZONTAL SWEEP SELECTOR POSITION	PIN #		
	5	7	9
1 kHz/DIV	1	0	0
2 kHz/DIV	1	0	0
5 kHz/DIV	0	1	0
10 kHz/DIV	0	1	0
20 kHz/DIV	0	1	0
50 kHz/DIV	0	0	1
.1 MHz/DIV	0	0	1
.2 MHz/DIV	0	0	1
.5 MHz/DIV	0	0	1
1 MHz/DIV	0	0	1
1 = +12 VDC		0 = 0 VDC	

1



NOTE: MEASUREMENT WAS TAKEN WITH AN INPUT AT THE ANTENNA OF 150 MHz @ -50 dBm USING AN X10 PROBE. FM/AM-1200S SETTING IS 1 MHz/DIV.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 800 (I.E., R1 IS R801).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

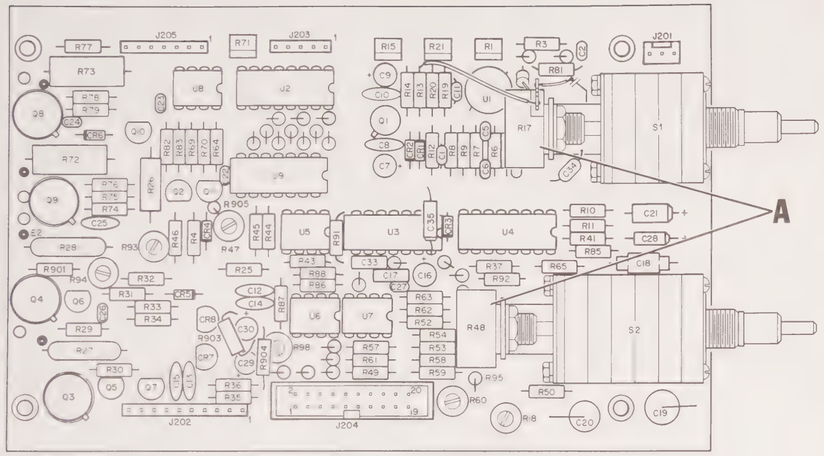
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE SPECIFIED.

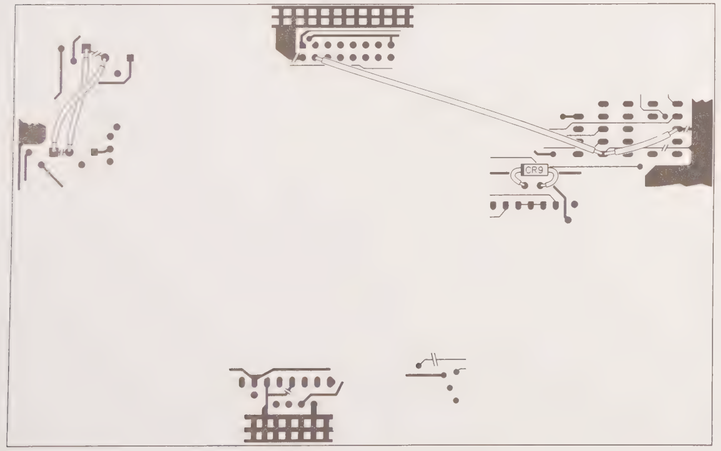
4. NOT USED.

5. R821 IS SELECTED AT TEST (S.A.T.):
   RANGE: 1.0KΩ TO 3.3KΩ
   NOMINAL: 1.8KΩ

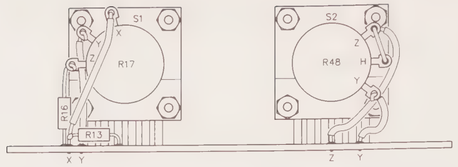
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-34 Analyzer Log Amp PC Board Assembly (0000-5110-600-C) (FM/AM-1200S ONLY)

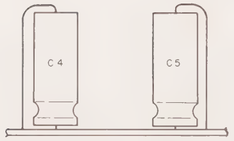




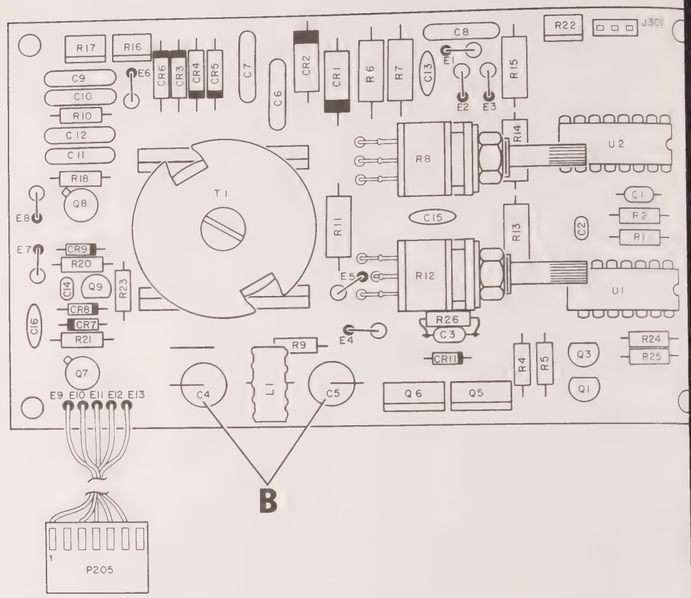
SCOPE CONTROL PC BOARD ASSY (7010-5130-200-J3)



DETAIL **A**

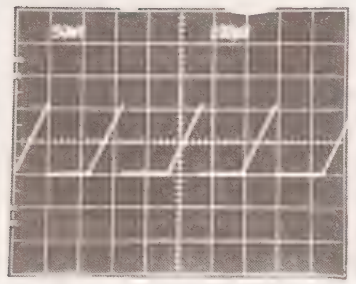


DETAIL **B**

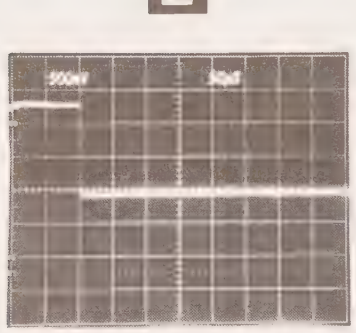


SCOPE POWER SUPPLY PC BOARD ASSY
(7010-5130-300-G)

1



2

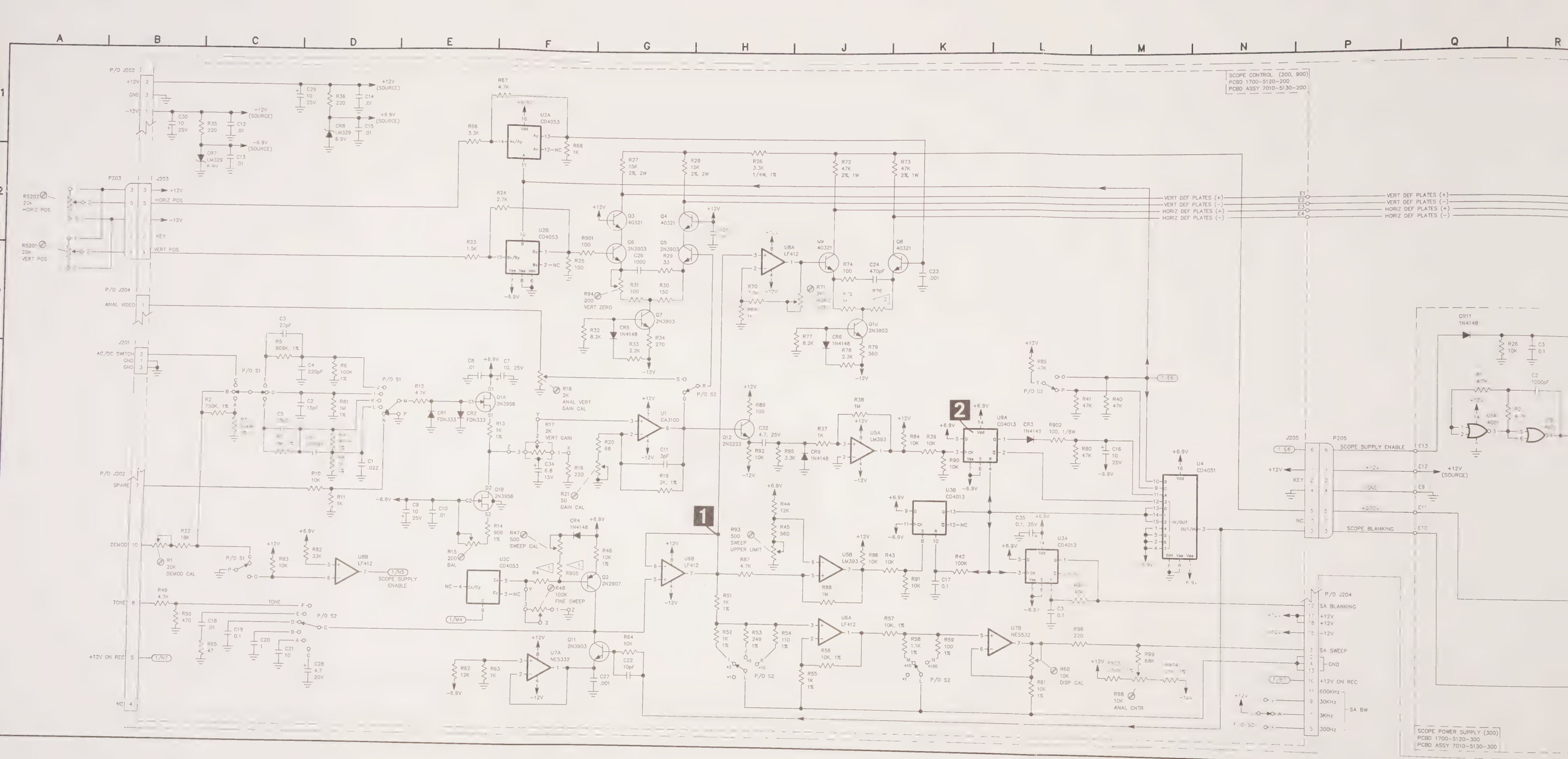


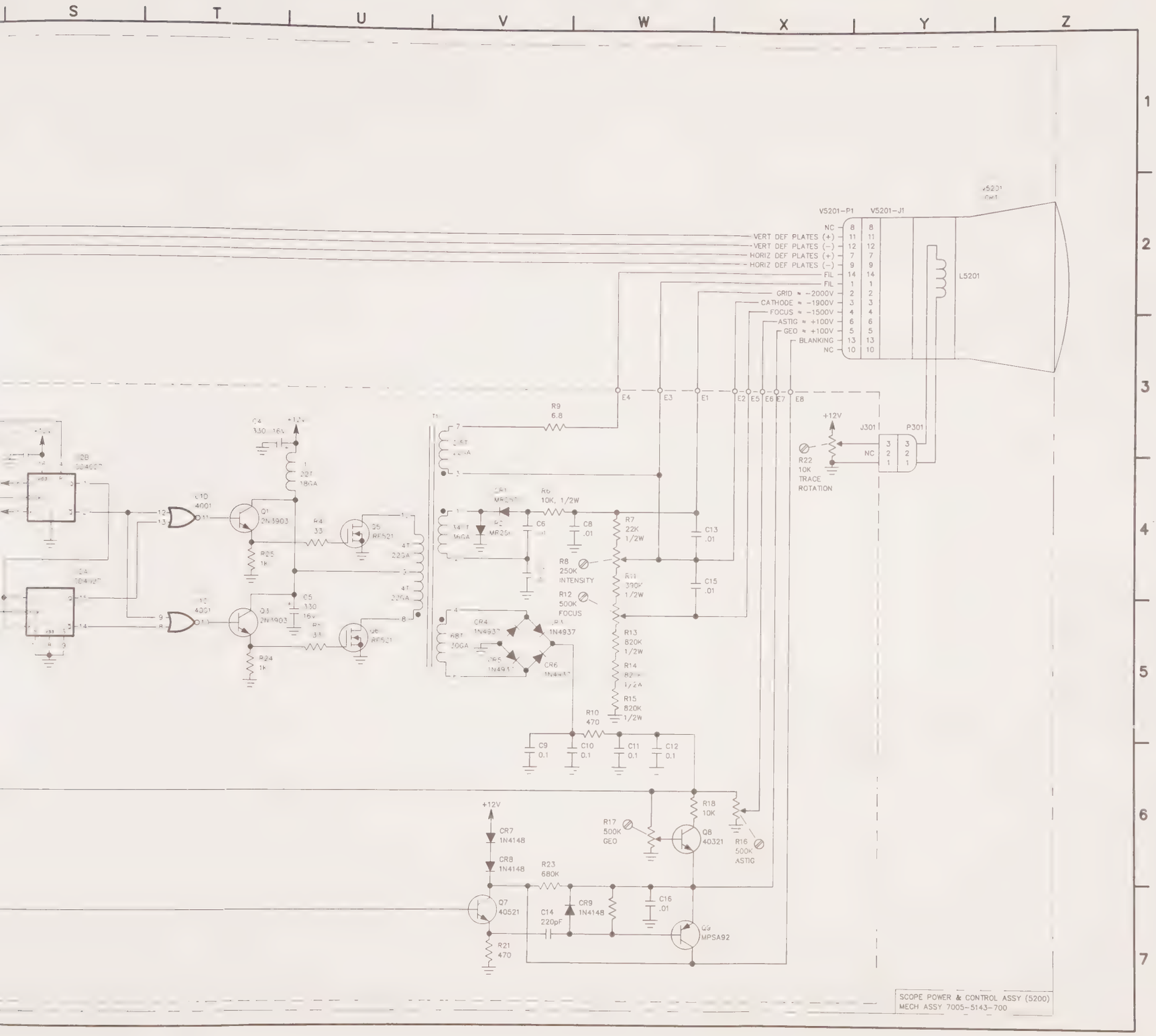
NOTE: ALL MEASUREMENTS WERE TAKEN WITH NO INPUT SIGNAL PRESENT. FM/AM-1200S SETTINGS: .01 ms/DIV, SQUELCH FULLY cw.

VERTICAL ATTENUATOR SELECTOR CONTROL (S201) TRUTH TABLE				
VERTICAL ATTENUATOR SELECTOR POSITION		PINS SHORTED		
		SECTION 1	SECTION 2	SECTION 3
kHz/$X10	OFF			P-O
	.5	D-B	M-I	
	.2	D-A	M-I	
	5	B-E		M-J
	20	E-A		M-J
V/DIV	10	F-C	M-L	P-G
	1	F-C	M-K	P-G
	.1	C-E		M-J P-G
.01		D-C	M-I	P-G
RESID				M-N P-G

HORIZONTAL SWEEP SELECTOR CONTROL (S202) TRUTH TABLE						
HORIZONTAL SWEEP SELECTOR POSITION		PINS SHORTED				
		SECTION 1	SECTION 2	SECTION 3	SECTION 4*	SECTION 5
TONE		C-F		T-P, R-Q		
mS/DIV	10		C-A	T-O, R-Q		
	1		C-B	T-O, R-Q		
	.1		C-D	T-O, R-Q		
	.01	C-E		T-O, R-Q		
MHz/DIV	1	C-G		R-S		U-V
	.5	C-G, L-I		R-S		U-V
	.2	C-G		R-S	L-J	U-V
	.1	C-G		R-S	L-K	U-V
kHz/DIV	50	C-G, L-I		R-S	L-M	U-V
	20	C-G		R-S	L-J, L-M	U-W
	10	C-G		R-S	L-K, L-M	U-W
	5	C-G, L-I		R-S	L-N	U-W
	2		C-A	R-S	L-J, L-N	U-X
	1		C-A	R-S	L-K, L-N	U-X
* - SECTION 4 CONTAINS TWO "L" PINS WHICH ARE TIED TO GROUND						

Figure 6-35 Scope Control & Power Supply Assembly (FM/AM-1200
(Sheet 1 of 2) (0000-5110-200-J2/0000-5110-300-G)


SCOPE CONTROL (200, 900)
PCBD 1700-5120-200
PCBD ASSY 7010-5130-200
SCOPE POWER SUPPLY (300)
PCBD 1700-5120-300
PCBD ASSY 7010-5130-300
VERT DEF PLATES (+)
VERT DEF PLATES (-)
HORIZ DEF PLATES (+)
HORIZ DEF PLATES (-)
SCOPE SUPPLY ENABLE
SCOPE BLANKING
SA BLANKING
SA SWEEP
SA BW
HORIZ POS
VERT POS
KEY
ANAL VIDEO
AC/DC SWITCH
SPARE
DEMOD
TONE
+12V ON REC
VERT ZERO
ANAL VERT GAIN CAL
VERT GAIN
GAIN CAL
SWEEP CAL
SWEEP UPPER LIMIT
BAL
FINE SWEEP
DEMOD CAL
DISP CAL
ANAL CNTR
1
2



NOTES:

1. R204 AND R905 ARE SELECTED AT TEST (S.A.T.):
   RANGE: 1.24KΩ TO 1.94KΩ
   NOMINAL: 1.5KΩ, 1% TOLERANCE

2. R276 IS SELECTED AT TEST (S.A.T.):
   RANGE: 800Ω TO 1.2KΩ
   NOMINAL: 1KΩ

3. THRU SER. NO. 6955: R224 WAS 27K, R267 WAS 10K.

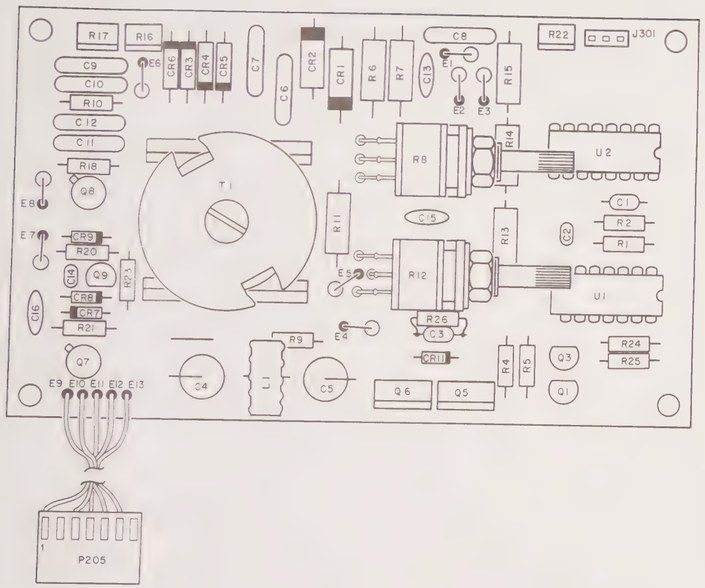
4. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 7005-5941-600: 5200 (I.E., R1 IS R5201).
   B. 7010-5931-600: 200, 900 (I.E., R1 IS R201, R101 IS R901).
   C. 7010-5130-300: 300 (I.E., R1 IS R301).

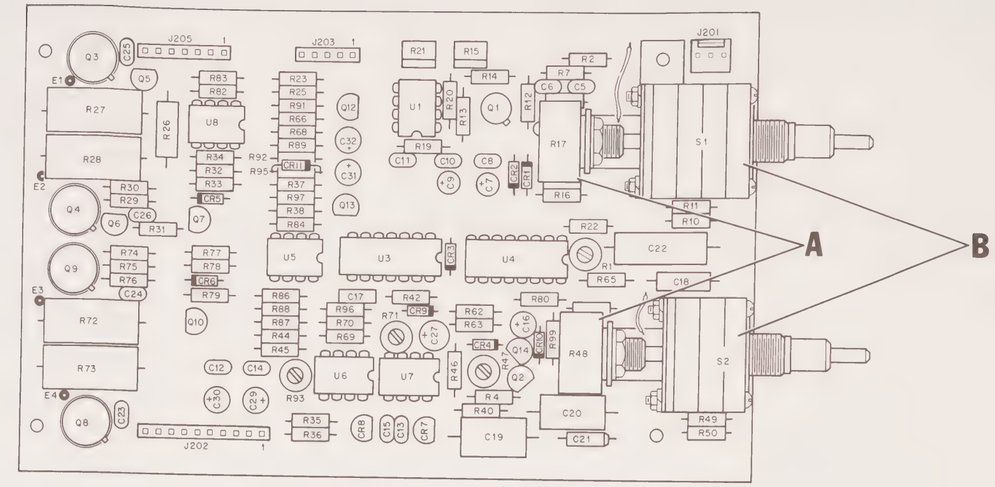
5. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

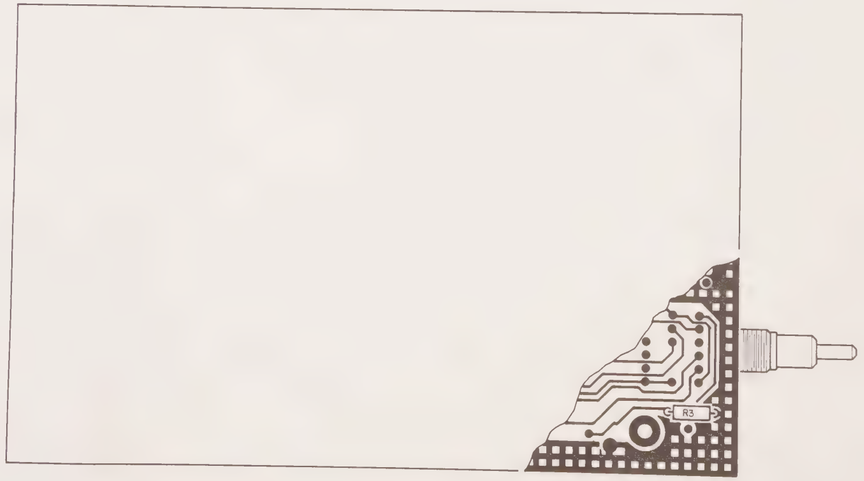
6. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-35 Scope Control & Power Supply Assembly (FM/AM-1200S) (Sheet 2 of 2) (0000-5110-200-J2/0000-5110-300-G)

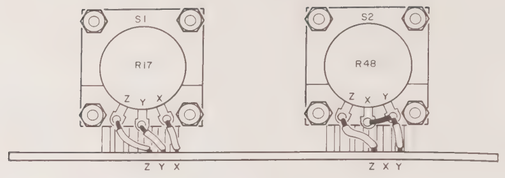


SCOPE CONTROL PC BOARD ASSY (FM/AM-1200A)
(7010-5130-300-G)

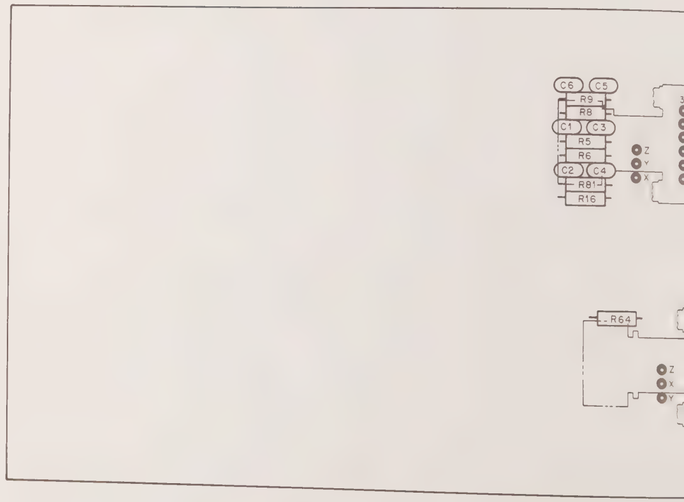




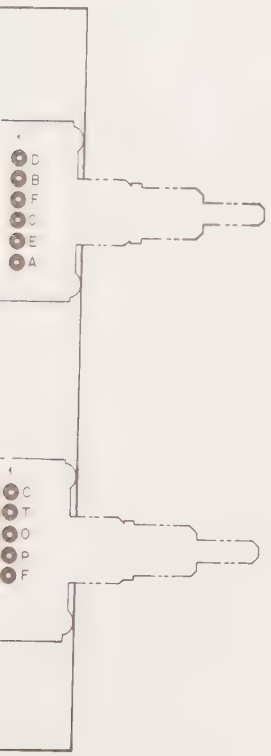
SCOPE POWER SUPPLY PC BOARD ASSY (FM/AM-1200A)
(7010-5530-200-F7)



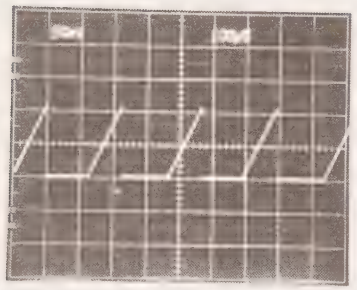
DETAIL **A**



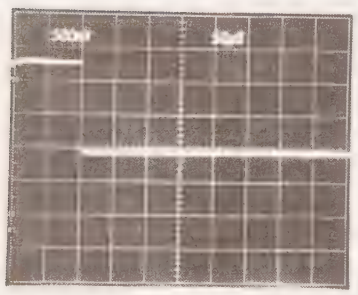
DETAIL **B**



1



2

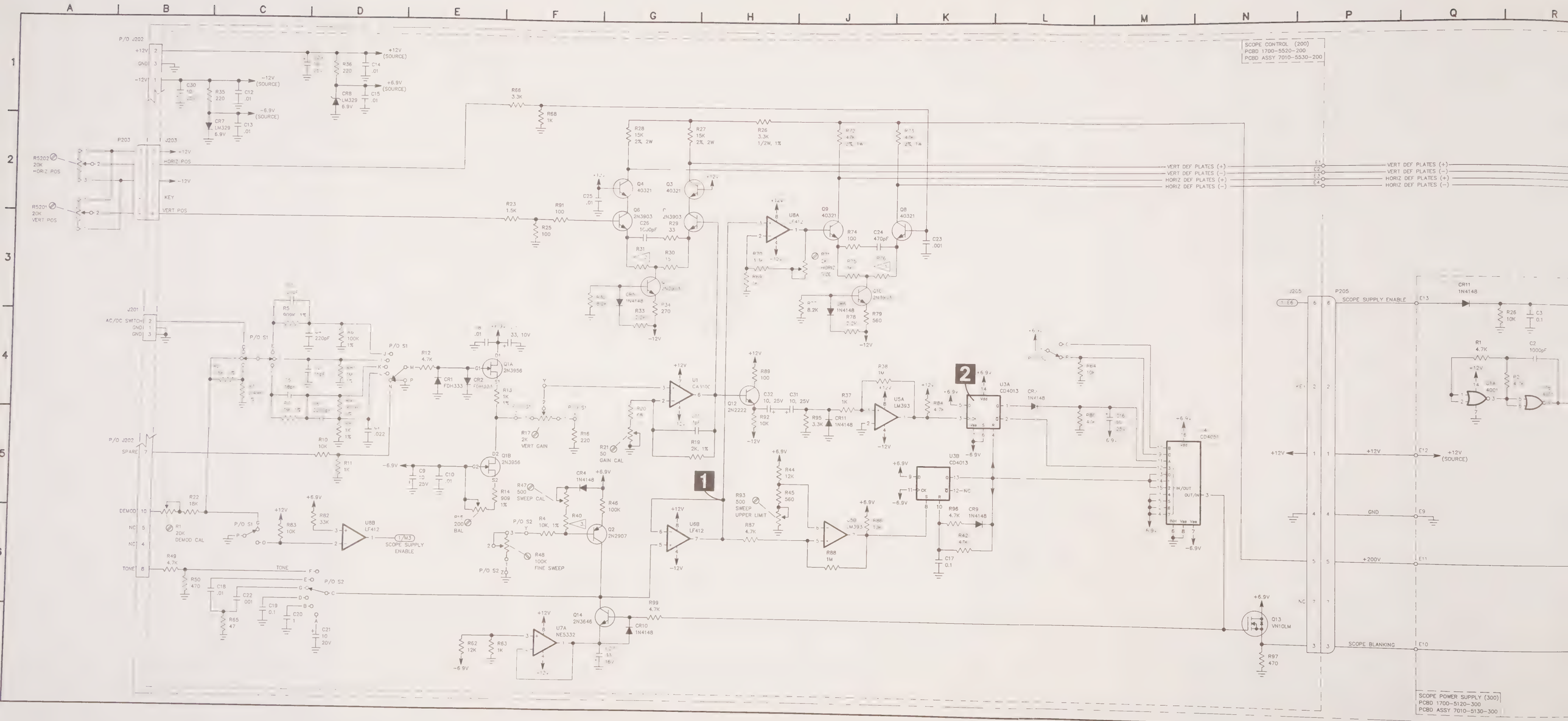


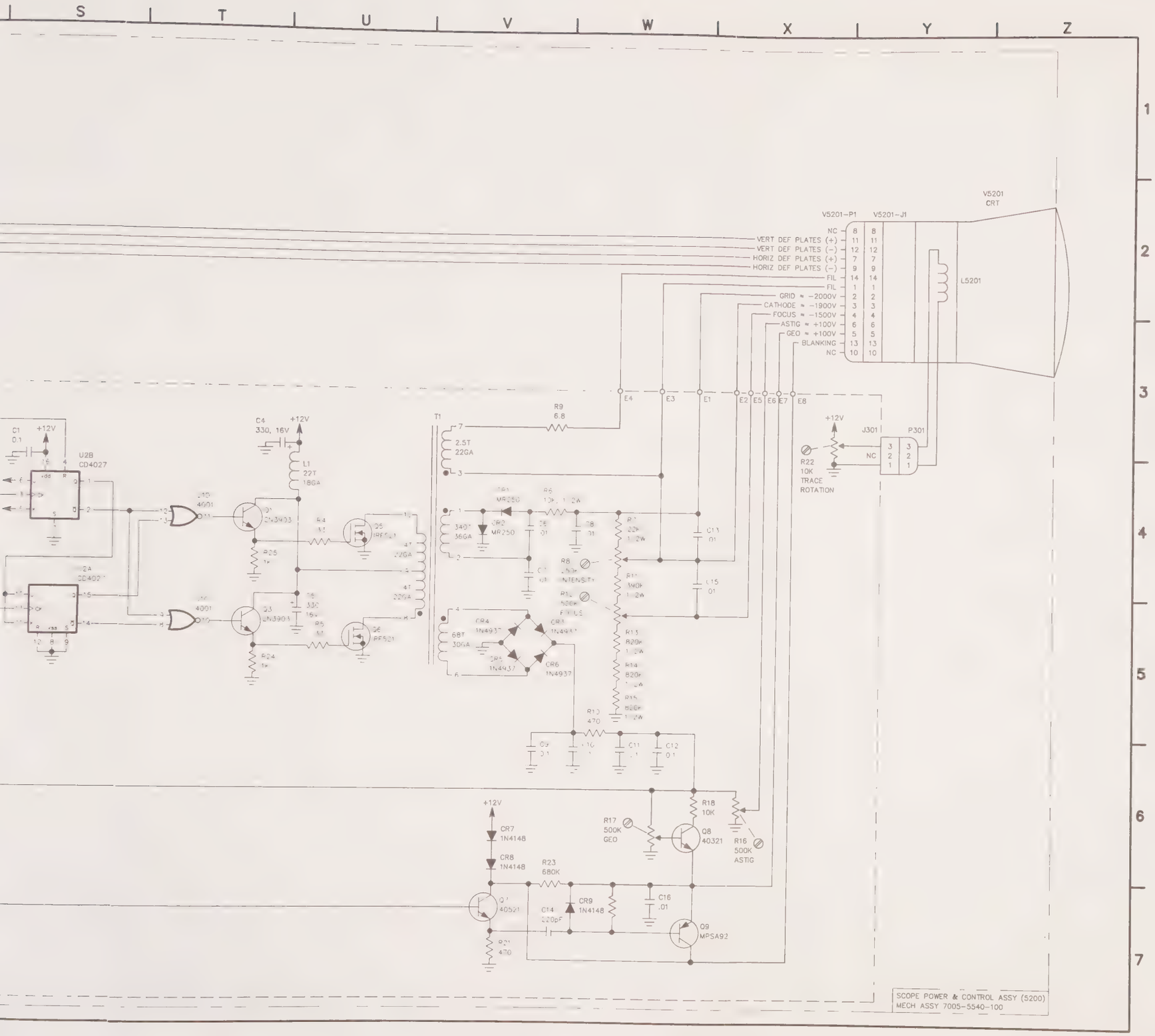
NOTE: ALL MEASUREMENTS WERE TAKEN WITH NO SIGNAL PRESENT. FM/AM-1200A SETTINGS: 10 µS/DIV, SQUELCH FULLY CW.

VERTICAL ATTENUATOR SELECTOR CONTROL (S201) TRUTH TABLE				
VERTICAL ATTENUATOR SELECTOR POSITION		PINS SHORTED		
		SECTION 1	SECTION 2	SECTION 3
kHz/⅀X10	OFF			P-O
	.5	D-B	M-I	
	.2	D-A	M-I	
	5	B-E		M-J
	20	E-A		M-J
V/DIV	10	F-C	M-L	P-G
	1	F-C	M-K	P-G
	.1	C-E		M-J P-G
.01		D-C	M-I	P-G
RESID				M-N P-G

HORIZONTAL SWEEP SELECTOR CONTROL (S202) TRUTH TABLE			
HORIZONTAL SWEEP SELECTOR POSITION		PINS SHORTED	
		SECTION 1	SECTION 2
TONE		C-F, T-P	
mS/DIV	10	T-O	C-A
	1	T-O	C-B
µS/DIV	100	T-O	C-D
	10	T-O	C-E
	1	T-O	C-G

Figure 6-36 Scope Control & Power Supply Assembly (FM/AM-1200A) (Sheet 1 of 2) (0000-5110-300-G/0000-5510-200-F4)


SCOPE CONTROL (200)
PCBD 1700-5520-200
PCBD ASSY 7010-5530-200
SCOPE POWER SUPPLY (300)
PCBD 1700-5120-300
PCBD ASSY 7010-5130-300
VERT DEF PLATES (+)
VERT DEF PLATES (-)
HORIZ DEF PLATES (+)
HORIZ DEF PLATES (-)
SCOPE SUPPLY ENABLE
SCOPE BLANKING
+12V
GND
+200V
+12V (SOURCE)
P/O J202
P203
J203
J201
AC/DC SWITCH
SPARE
DEMOD
TONE
HORIZ POS
KEY
VERT POS
VERT GAIN
GAIN CAL
SWEEP CAL
FINE SWEEP
SWEEP UPPER LIMIT
DEMOD CAL
BAL
1
2



NOTES:

1. R276 IS SELECTED AT TEST (S.A.T.):
   RANGE: 560Ω TO 1.2KΩ
   NOMINAL: 560Ω

2. R231 IS SELECTED AT TEST (S.A.T.):
   RANGE: 42Ω TO 200Ω
   NOMINAL: 150Ω

3. R240 IS SELECTED AT TEST (S.A.T.):
   RANGE: 1.24KΩ TO 1.91KΩ
   NOMINAL: 1.5KΩ

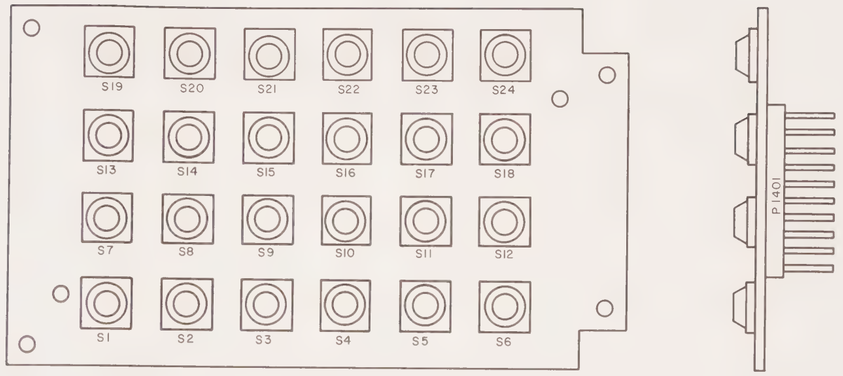
4. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 7005-5941-600: 5200 (I.E., L1 IS L5201).
   B. 7010-59351-600: 200, 900 (I.E., R1 IS R201, R101 IS R901).
   C. 7010-5930-300: 300 (E.I., R1 IS R301).

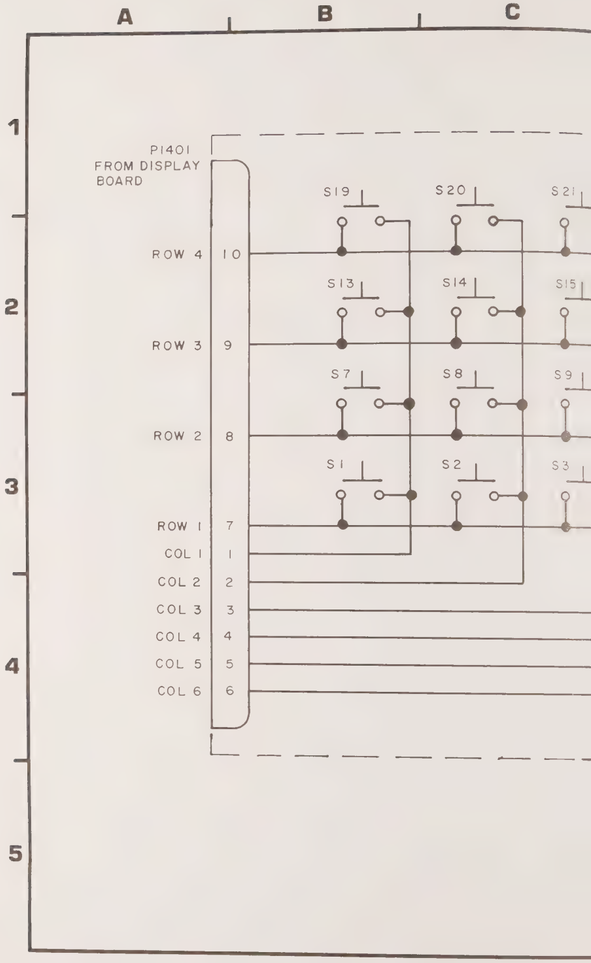
5. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

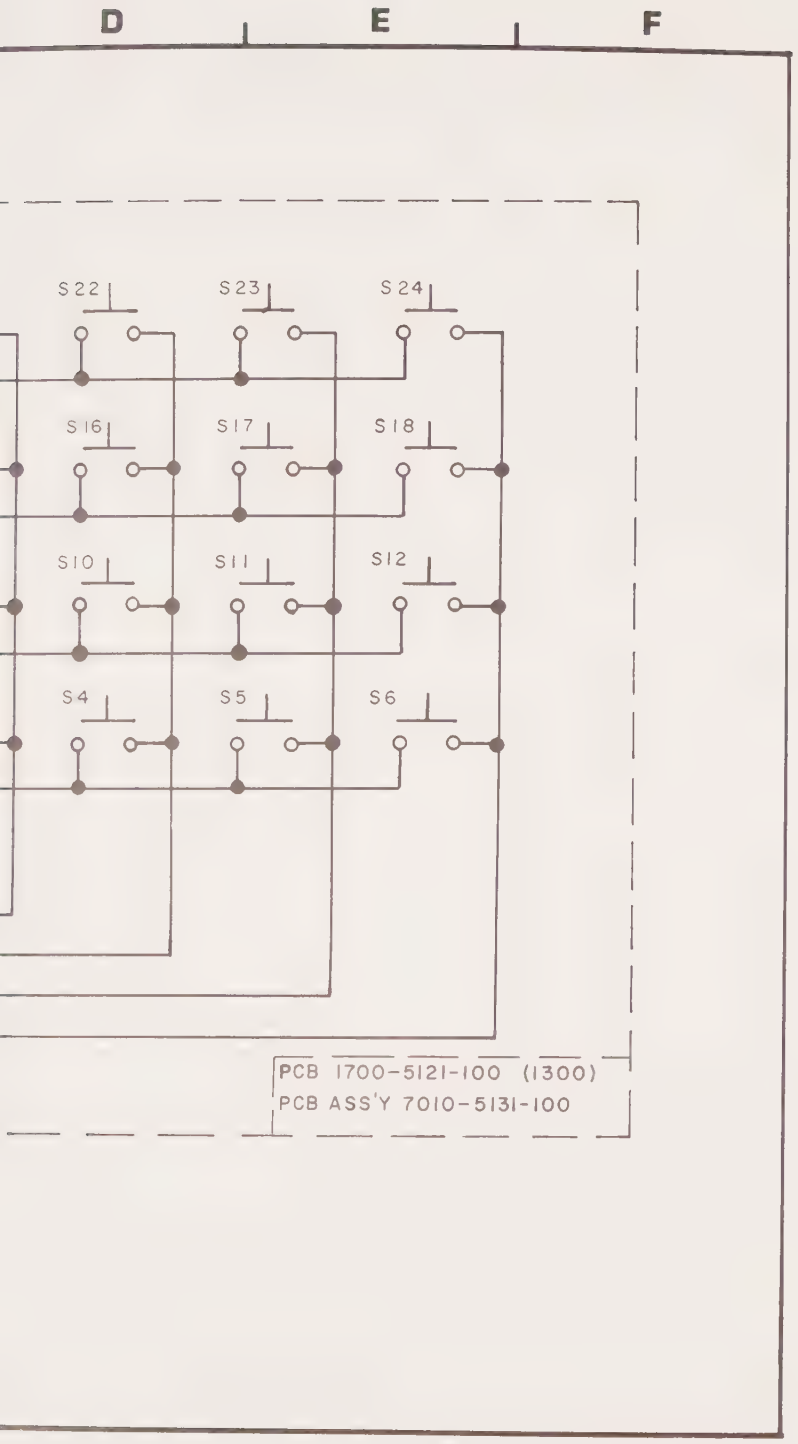
6. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-36 Scope Control & Power Supply Assembly (FM/AM-1200A) (Sheet 2 of 2) (0000-5110-300-G/0000-5510-200-F4)



KEYBOARD PC BOARD ASSY
(7010-5131-100-B)

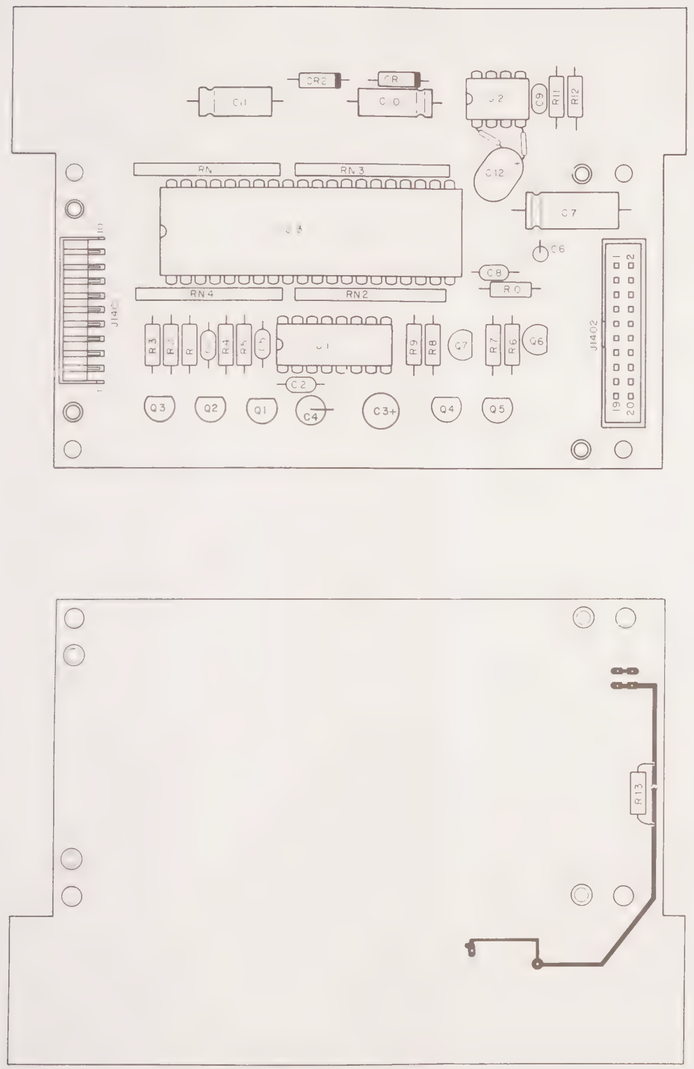




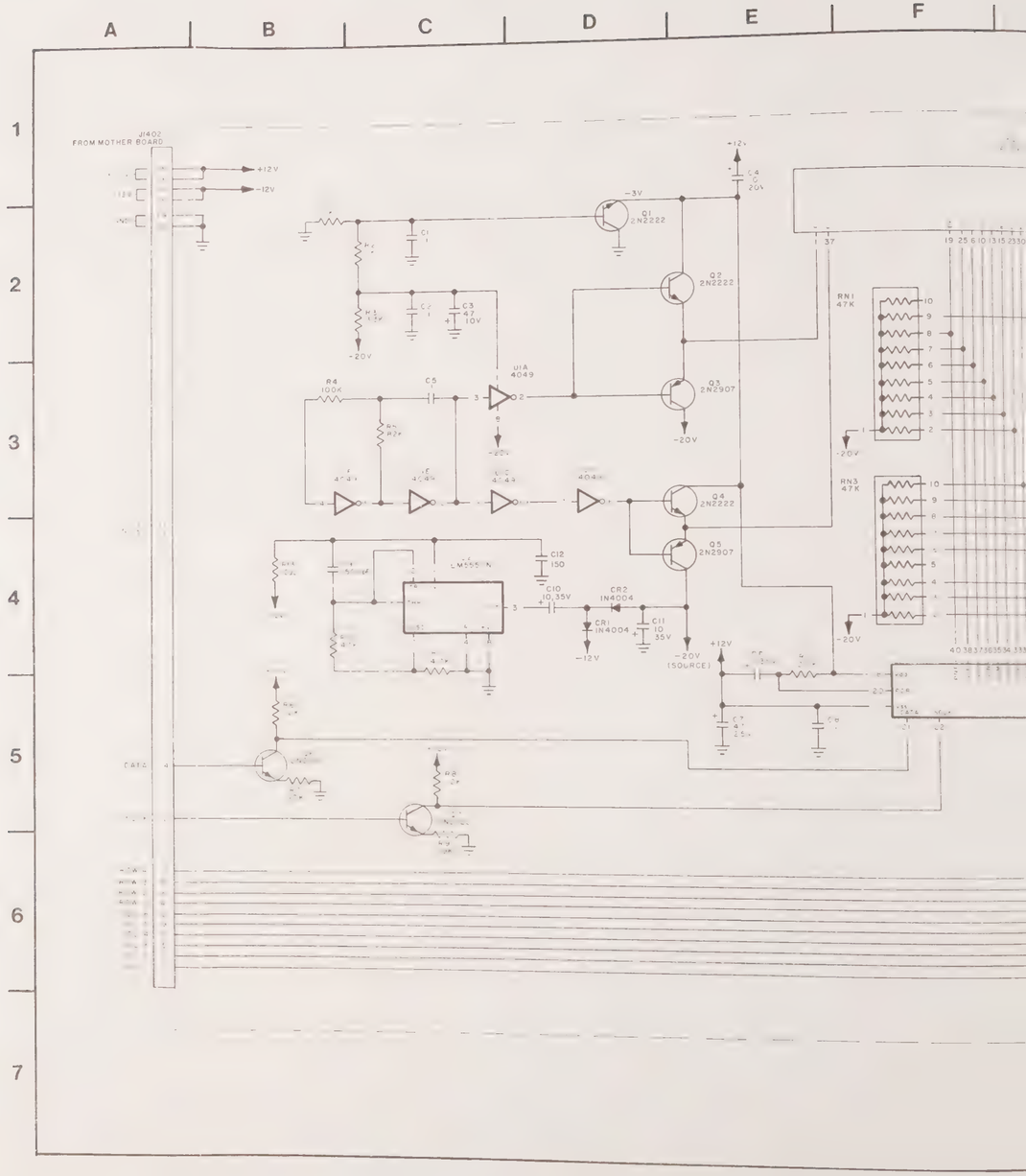
NOTES:

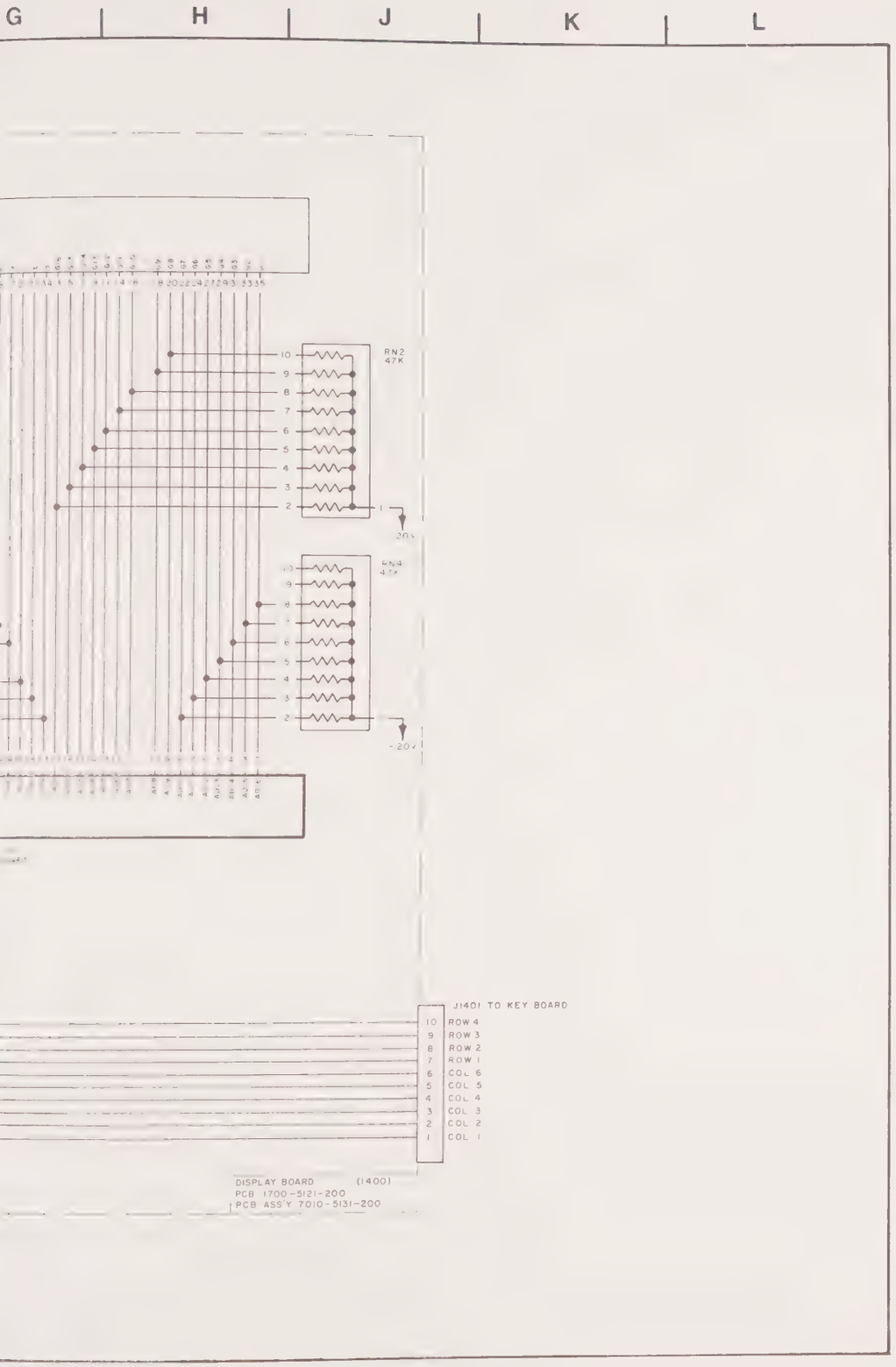
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 1300 (I.E., R1 IS R1301).

Figure 6-37 Keyboard Assembly (0000-5110-100-B)



DISPLAY PC BOARD ASSY
(7010-5131-200-D8)





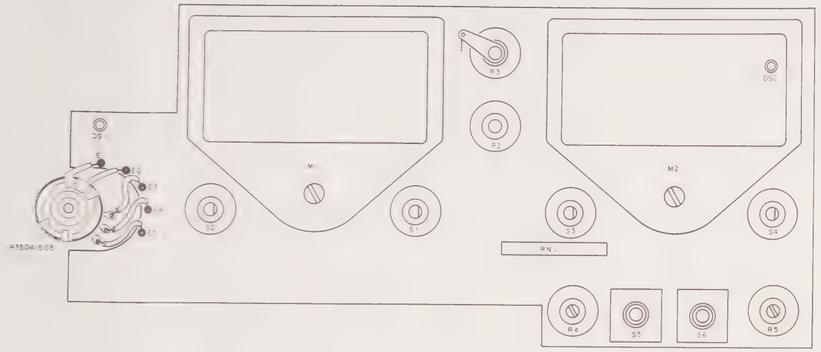
NOTES:

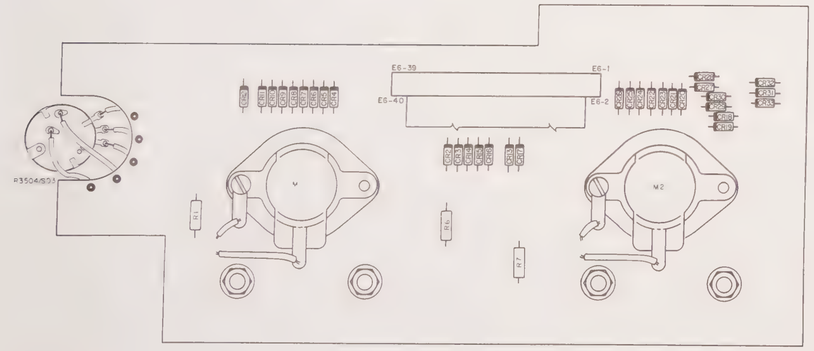
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 1400 (I.E., R1 IS R1401).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-38 Display PC Board Assembly (0000-5111-200-E3)





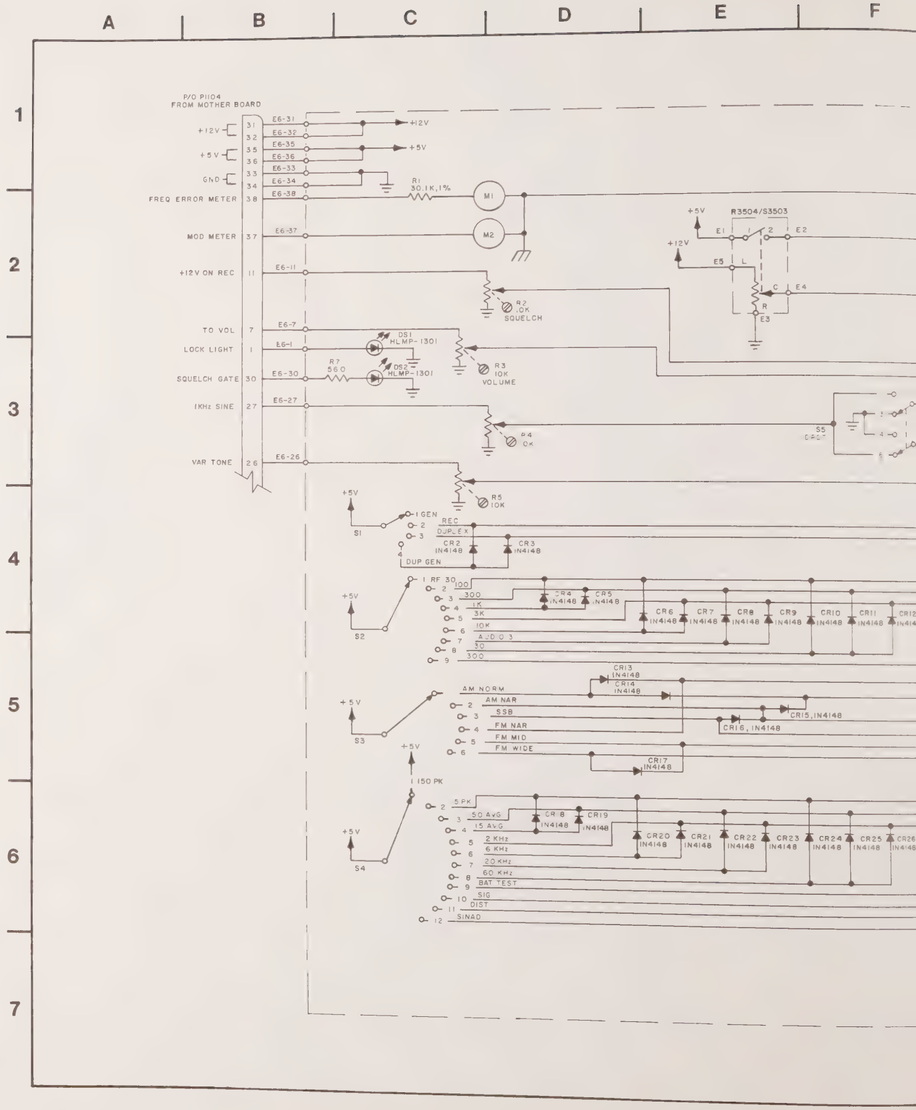
FUNCTION SWITCH PC BOARD ASSY
(7010-5530-700-C5)

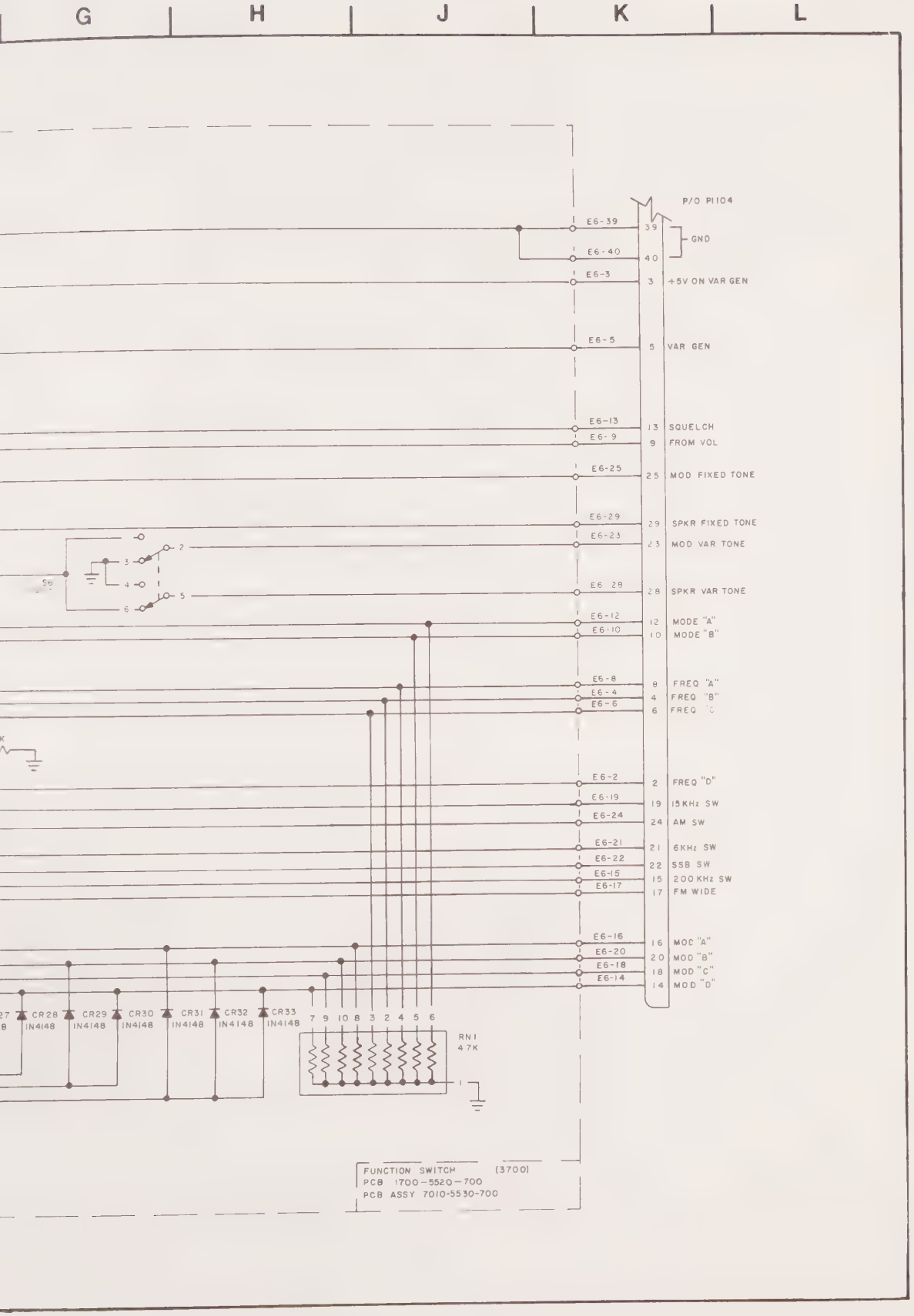
S3701 MODE SELECTOR CONTROL		
POSITION	CONTROL LINES	
	MODE A	MODE B
GEN	0	0
REC	1	0
DUP	0	1
DUP/GEN	1	1
1 = +5 VDC	0 = 0 VDC	

S3703 MODULATION SELECT CONTROL						
POSITION	CONTROL LINES					
	AM	SSB	FM WIDE	6K	15K	200K
AM NORM	1	0	0	0	1	0
AM NAR	1	0	0	1	0	0
SSB	1	1	0	1	0	0
FM NAR	0	0	0	0	1	0
FM MID	0	0	0	0	0	1
FM WIDE	1	0	1	0	0	1
1 = +12 VDC			0 = 0 VDC			

S3702 FREQ ERROR METER RANGE SELECTOR CONTROL				
POSITION	CONTROL LINES			
RF	FREQ MTR A	FREQ MTR B	FREQ MTR C	FREQ MTR D
30	0	0	0	0
100	1	0	0	0
300	0	1	0	0
1K	1	1	0	0
3K	0	0	1	0
10K	1	0	1	0
AUDIO				
3	0	1	1	0
30	1	1	1	0
300	0	0	0	1
1 = +5 VDC			0 = 0 VDC	

S3704 MODULATION METER CONTROL				
POSITION	CONTROL LINES			
	MOD MTR A	MOD MTR B	MOD MTR C	MOD MTR D
WP 150	0	0	0	0
WP 15	1	0	0	0
WA 150	0	1	0	0
WA 15	1	1	0	0
2 kHz/$X10	0	0	1	0
6 kHz/$X10	1	0	1	0
20 kHz/$X10	0	1	1	0
60 kHz/$X10	1	1	1	0
BATT	0	0	0	1
SIG	1	0	0	1
DIST	0	1	0	1
SINAD	1	1	0	1
1 = +5 VDC			0 = 0 VDC	





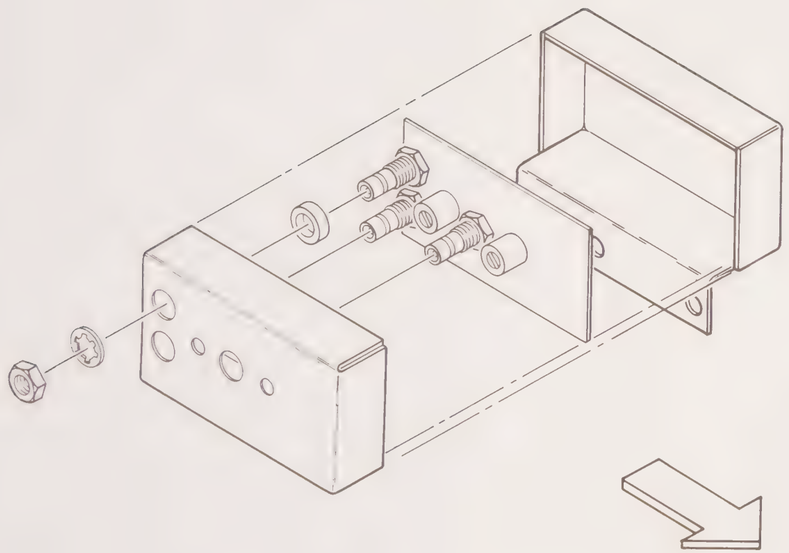
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3700 (I.E., R1 IS R3701).

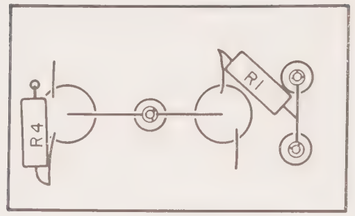
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

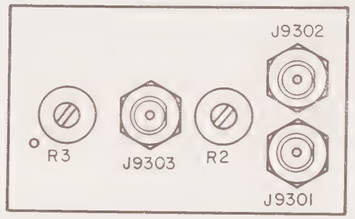
Figure 6-39 Function Switch PC Board Assembly (0000-5510-700-C)



MIXER NULL ASSY (7005-5144-700-B)

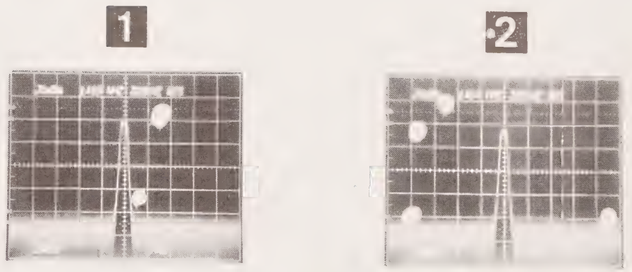


BOTTOM

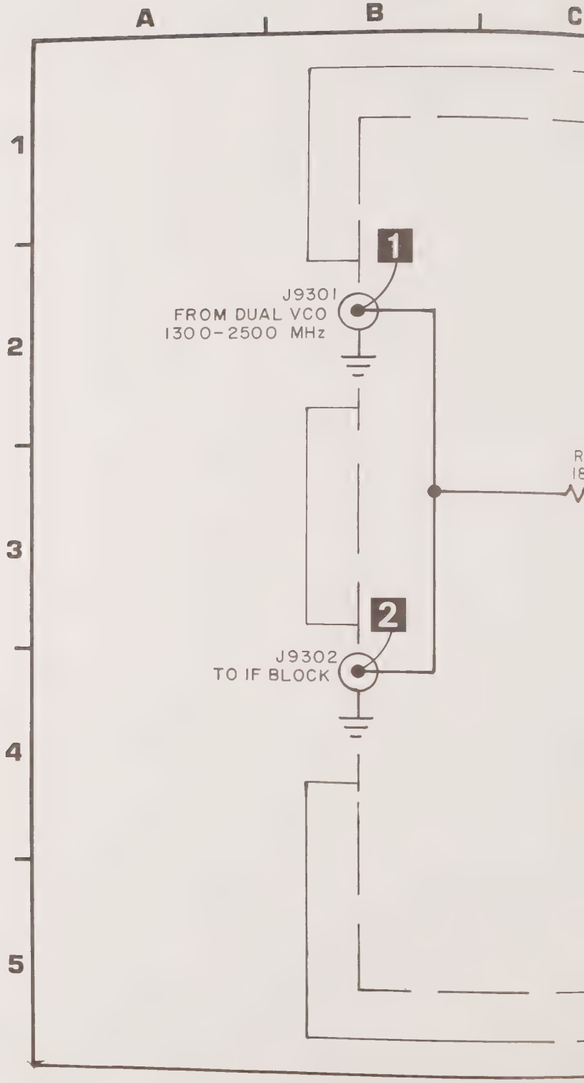


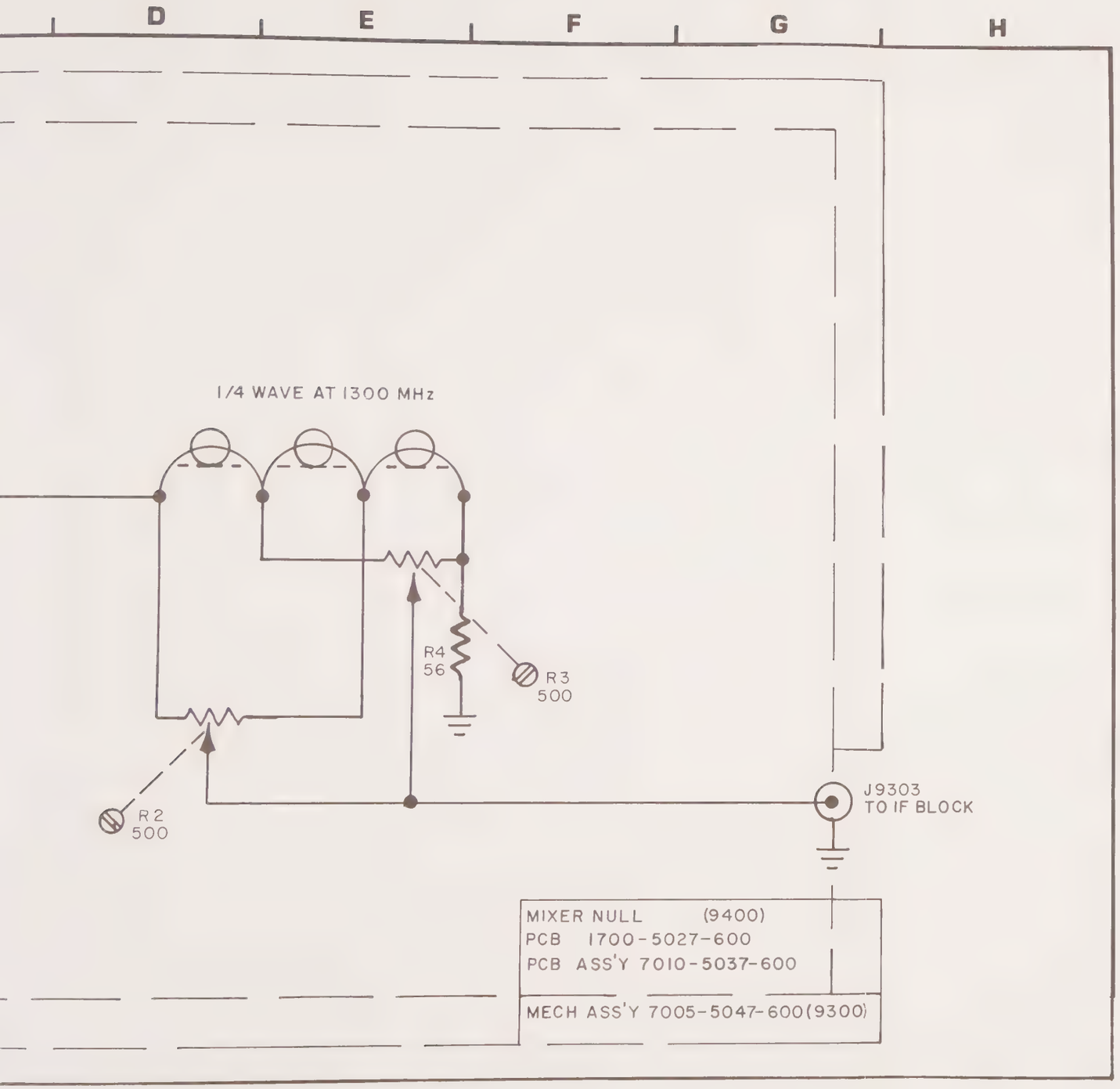
TOP

MIXER NULL PC BOARD ASSY
(7010-5037-600-A5)



NOTE: ALL MEASUREMENTS WERE TAKEN IN GEN MODE WITH FM/AM-1200S/A AT 150.2 MHz.





NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING SERIES:

   A. MECH ASSY (7005-5047-600): 9300 (I.E., R1 IS R9301).

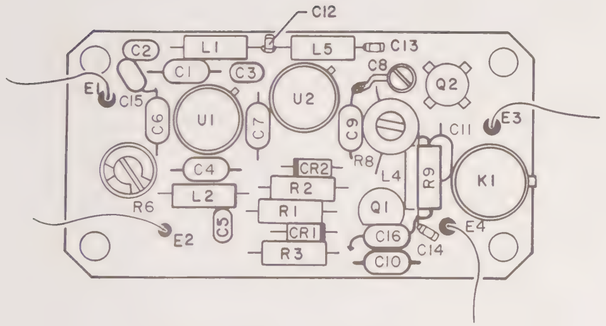
   B. PCB ASSY (7010-5037-600): 9400 (I.E., R1 IS R9401).

2. CRITICAL LENGTH OF CONDUCTOR: 1/4 τ AT 1300 MHz.

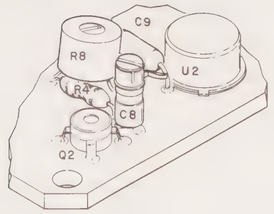
3. ALL RESISTORS ARE 1/8 W, ±5% TOLERANCE.

4. ALL RESISTANCE IS EXPRESSED IN OHMS, UNLESS OTHERWISE NOTED.

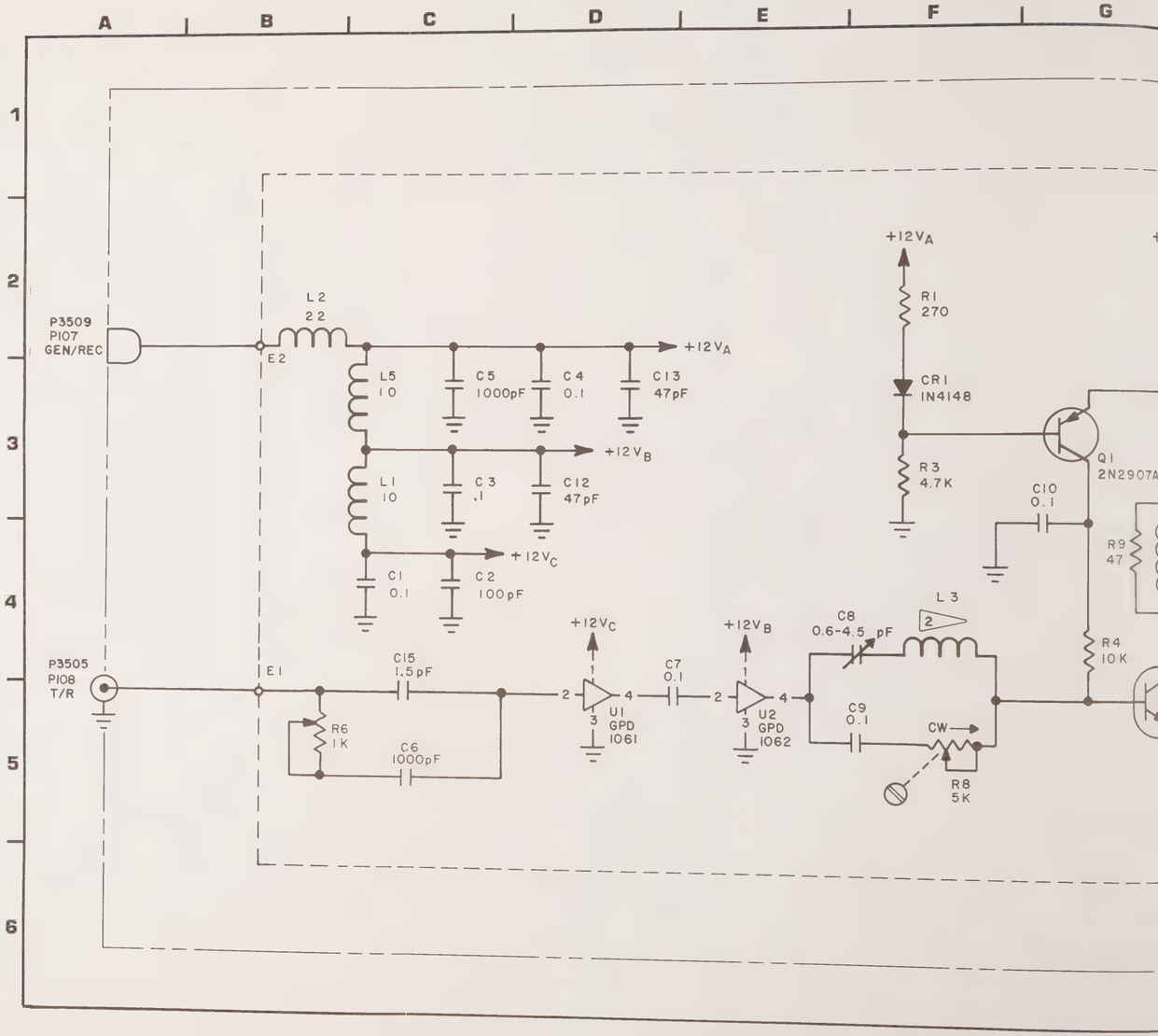
Figure 6-40 Mixer Null Assembly (0000-5016-600-C1)

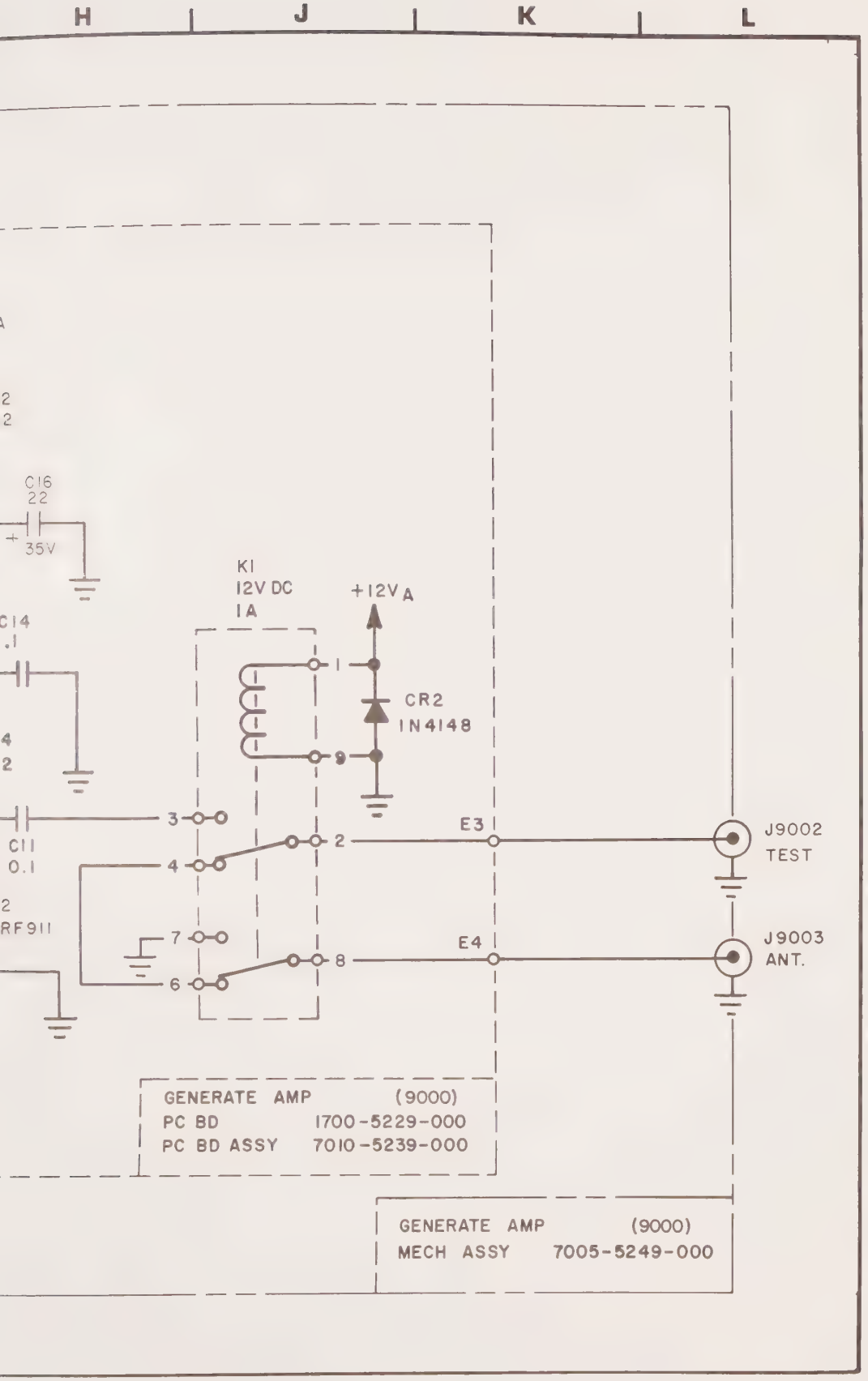


GENERATE AMP PC BOARD ASSY
(7010-5239-000-A4)



DETAIL **A**





NOTES:

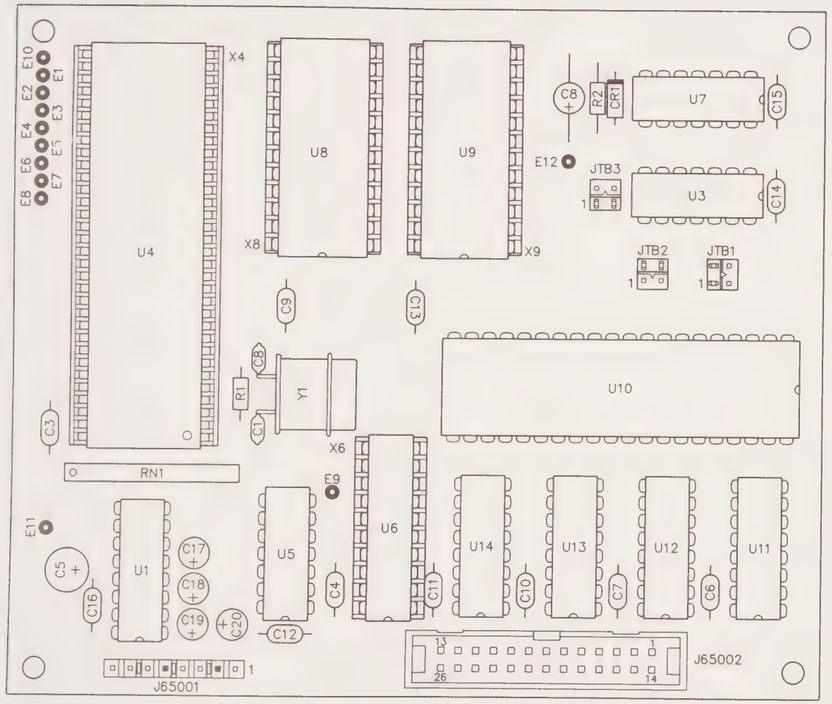
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 9000 (I.E., R1 IS R9001).

2. L9003 IS FORMED FROM LEAD OF C9008 CUT TO 0.2" LENGTH.

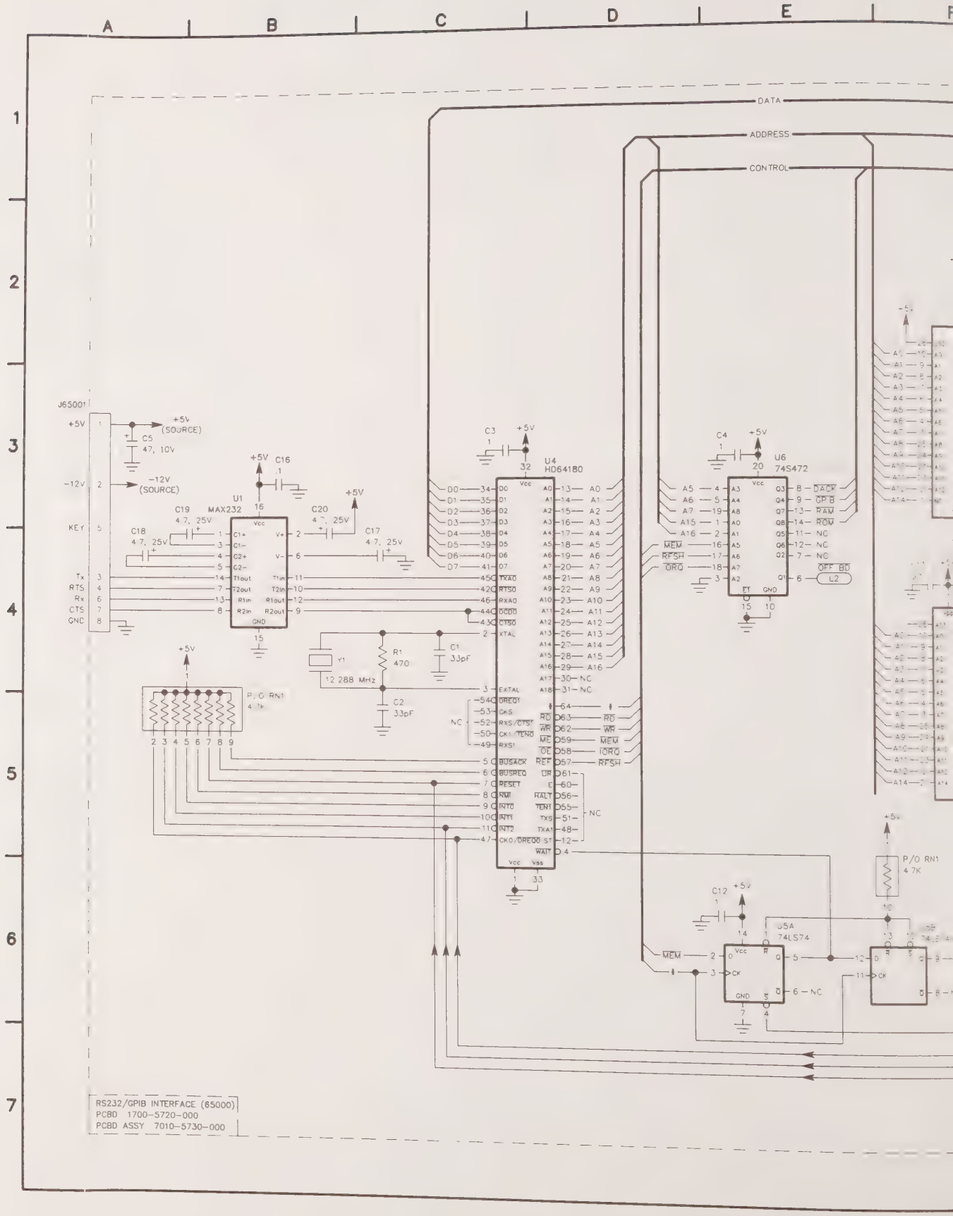
3. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

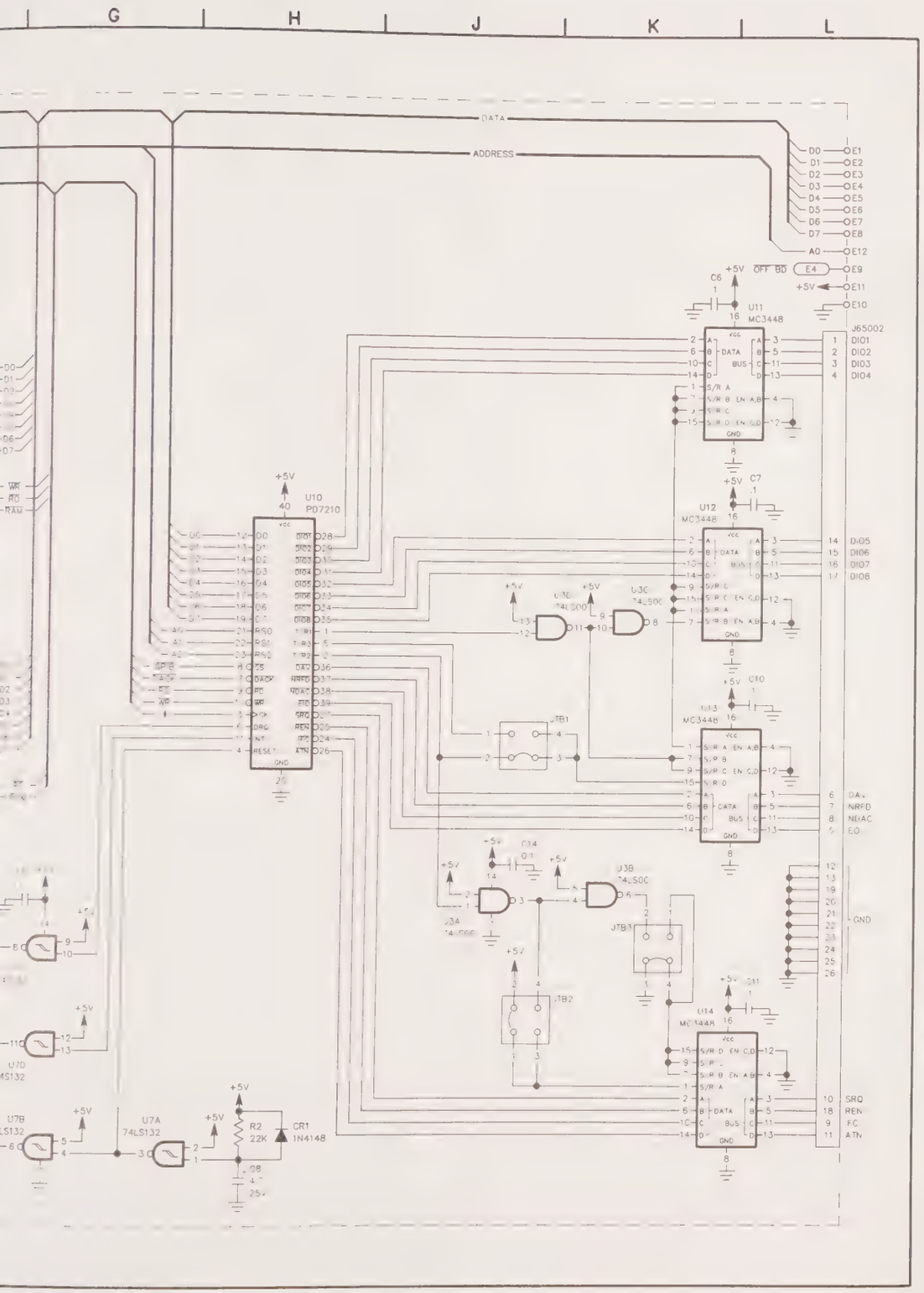
4. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS AND ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS, UNLESS OTHERWISE NOTED.

Figure 6-41 Generate Amplifier Assembly (0000-5219-000-B3)



RS-232C/GPIB INTERFACE PC BOARD ASSY
(7010-5730-000-C3)





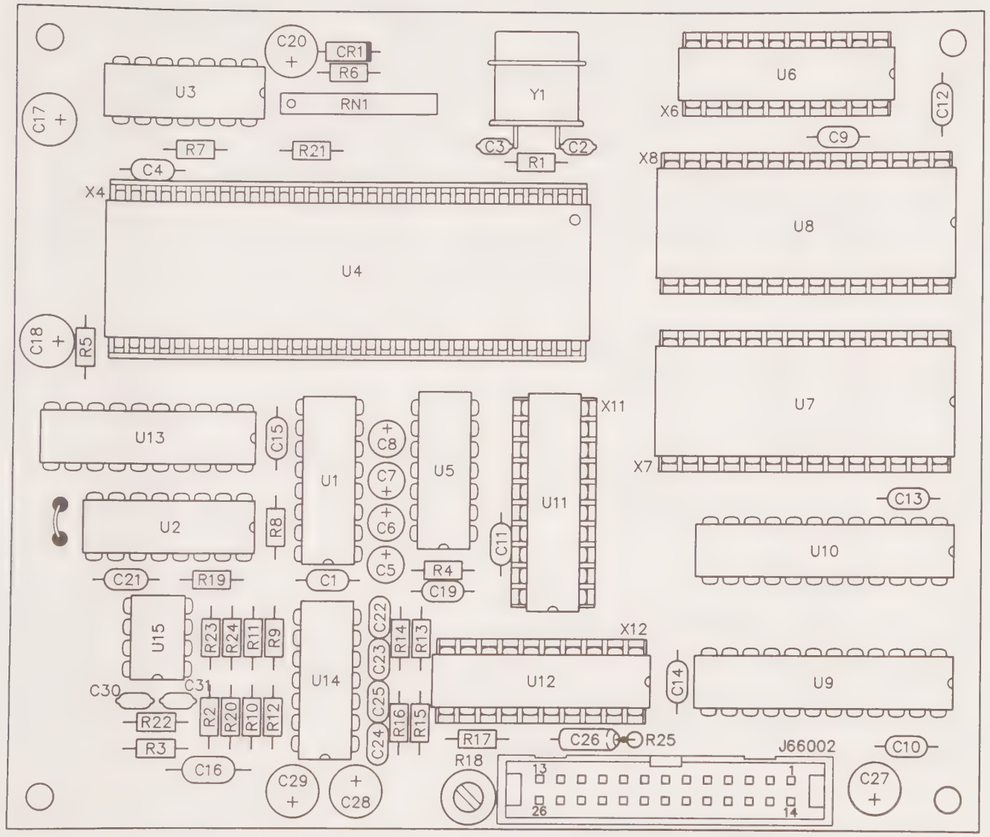
NOTES:

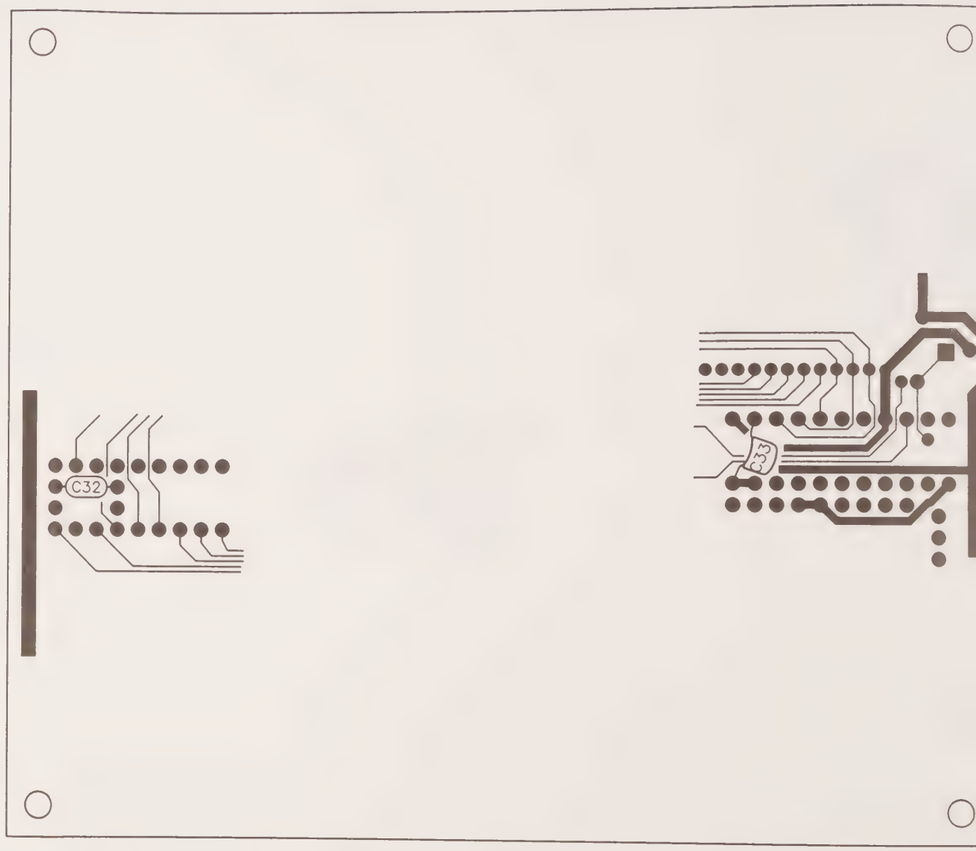
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 65000 (I.E., R1 IS R65001).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

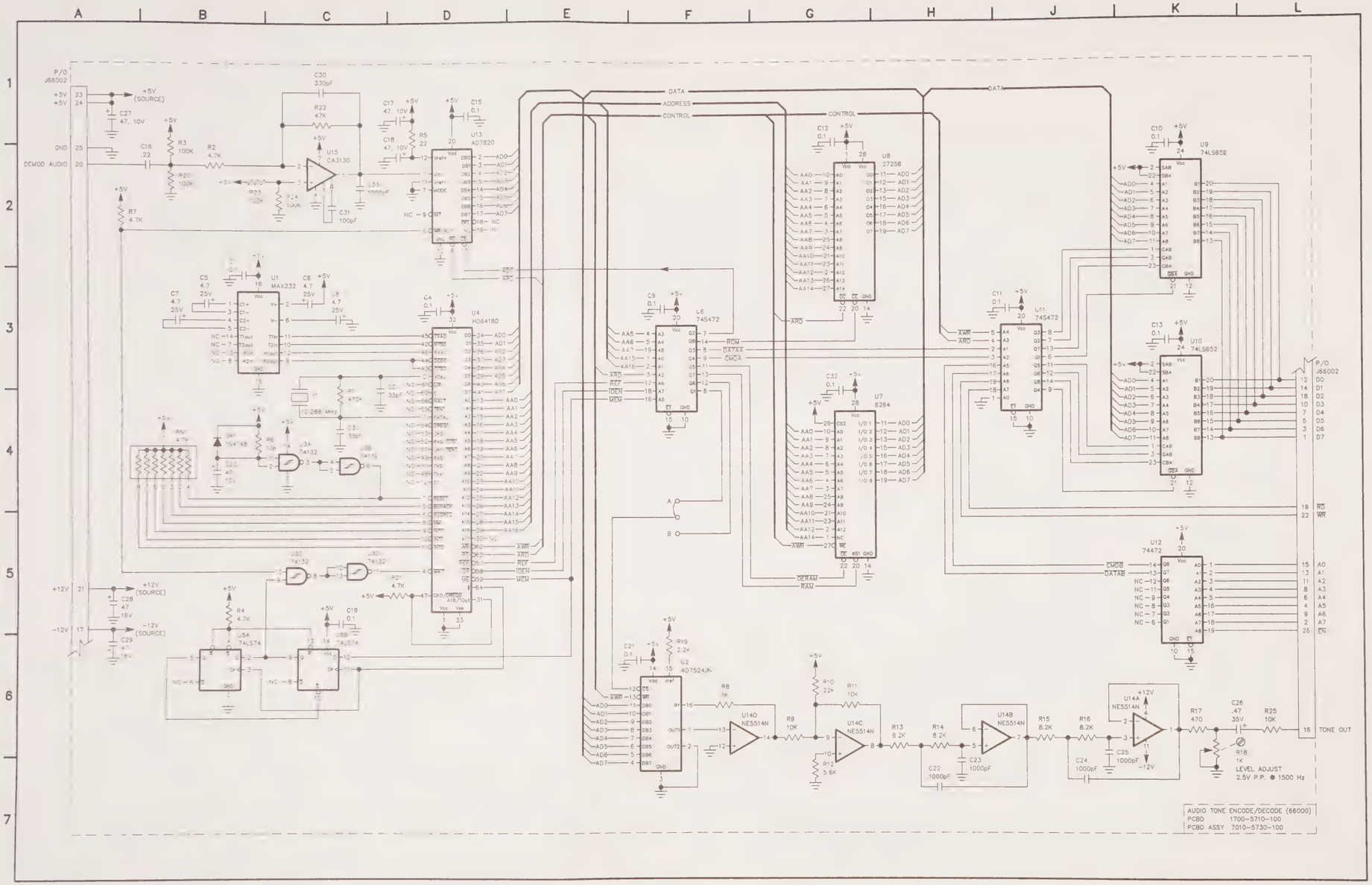
3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

Figure 6-42 RS-232C/GPIB Interface PC Board Assembly (Option) (0000-5710-000-C2)





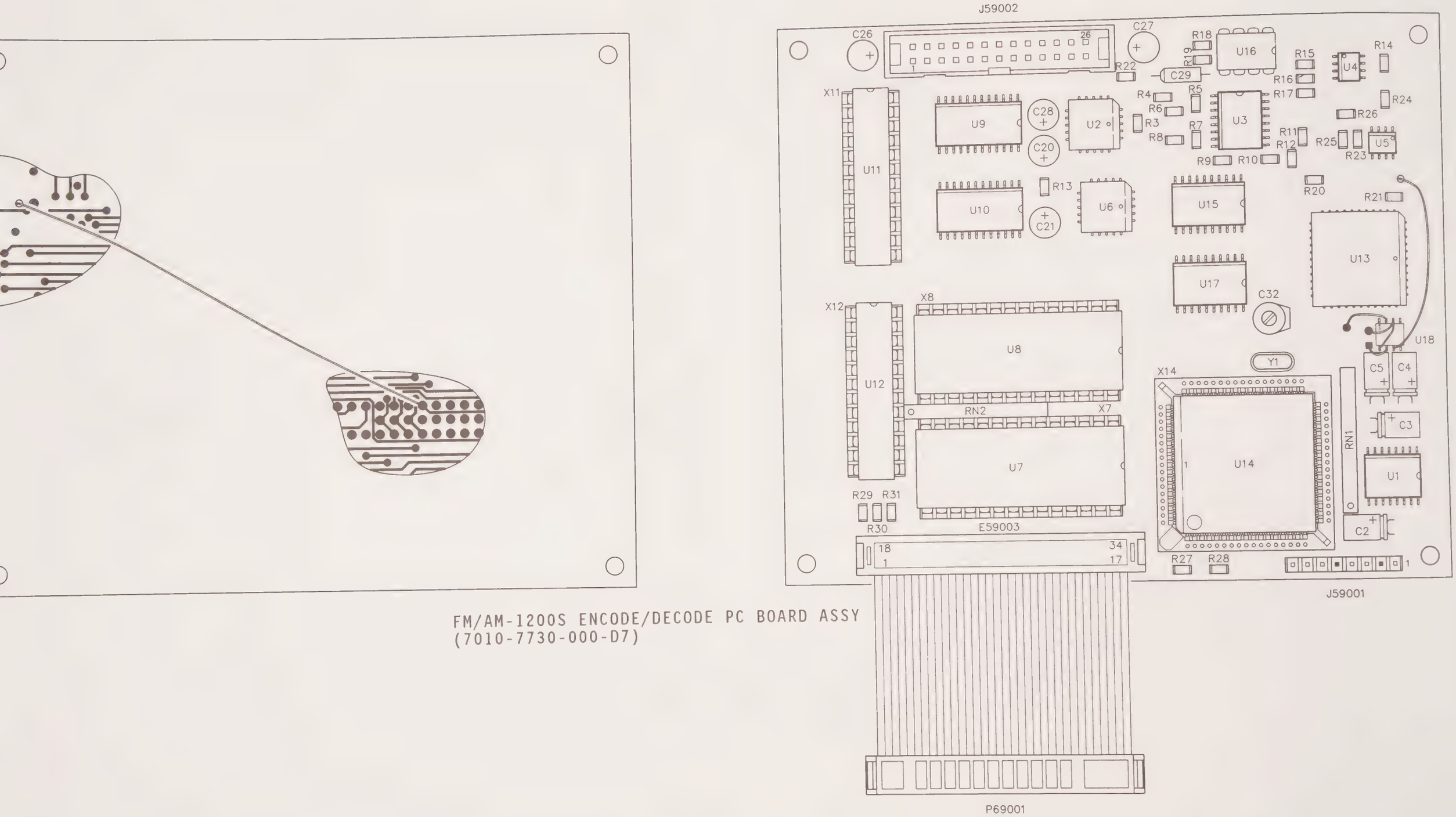
AUDIO ENCODE/DECODE PC BOARD ASSY
(7010-5730-100-C7)



NOTES:

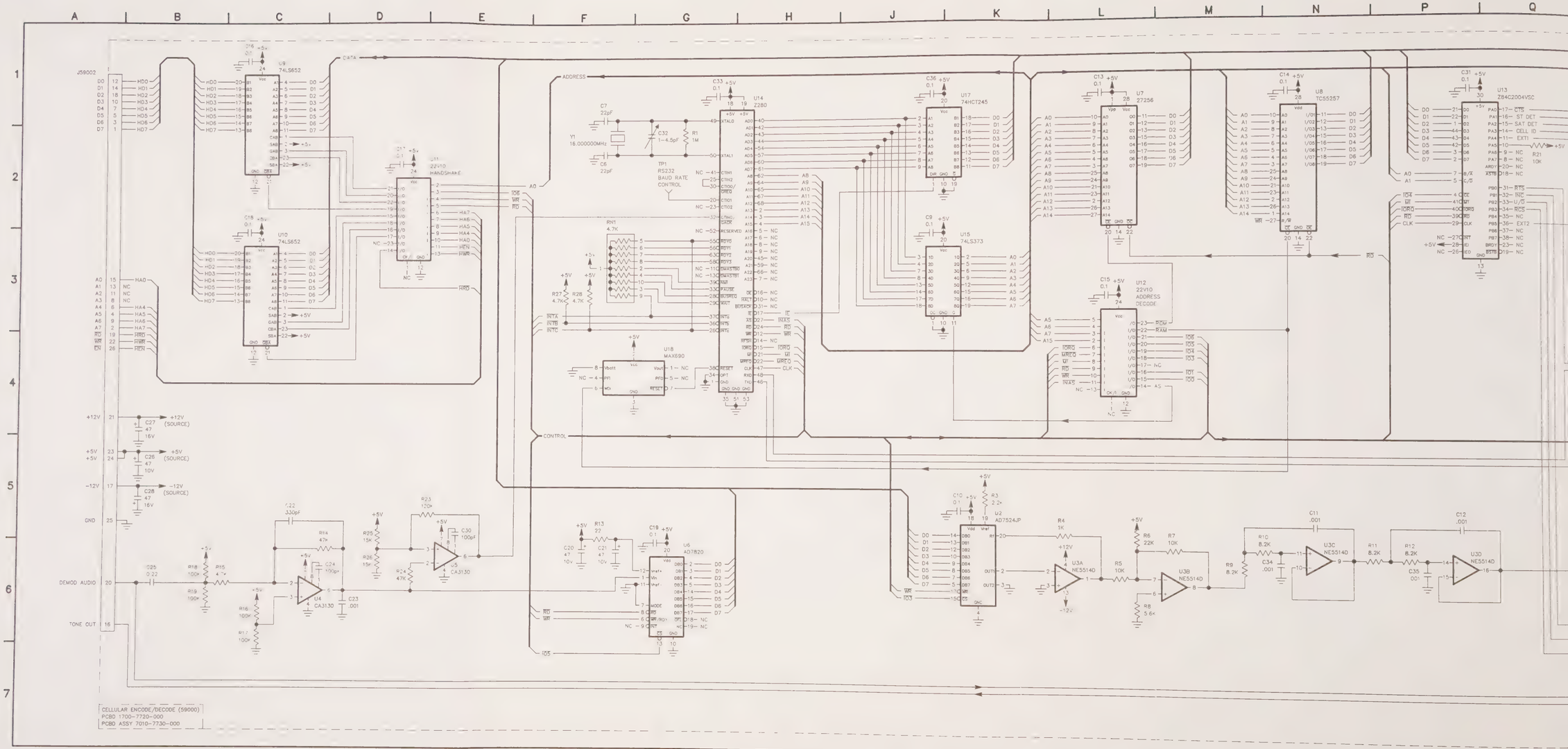
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 66000 (I.E., R1 IS R66001).
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS; AND ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

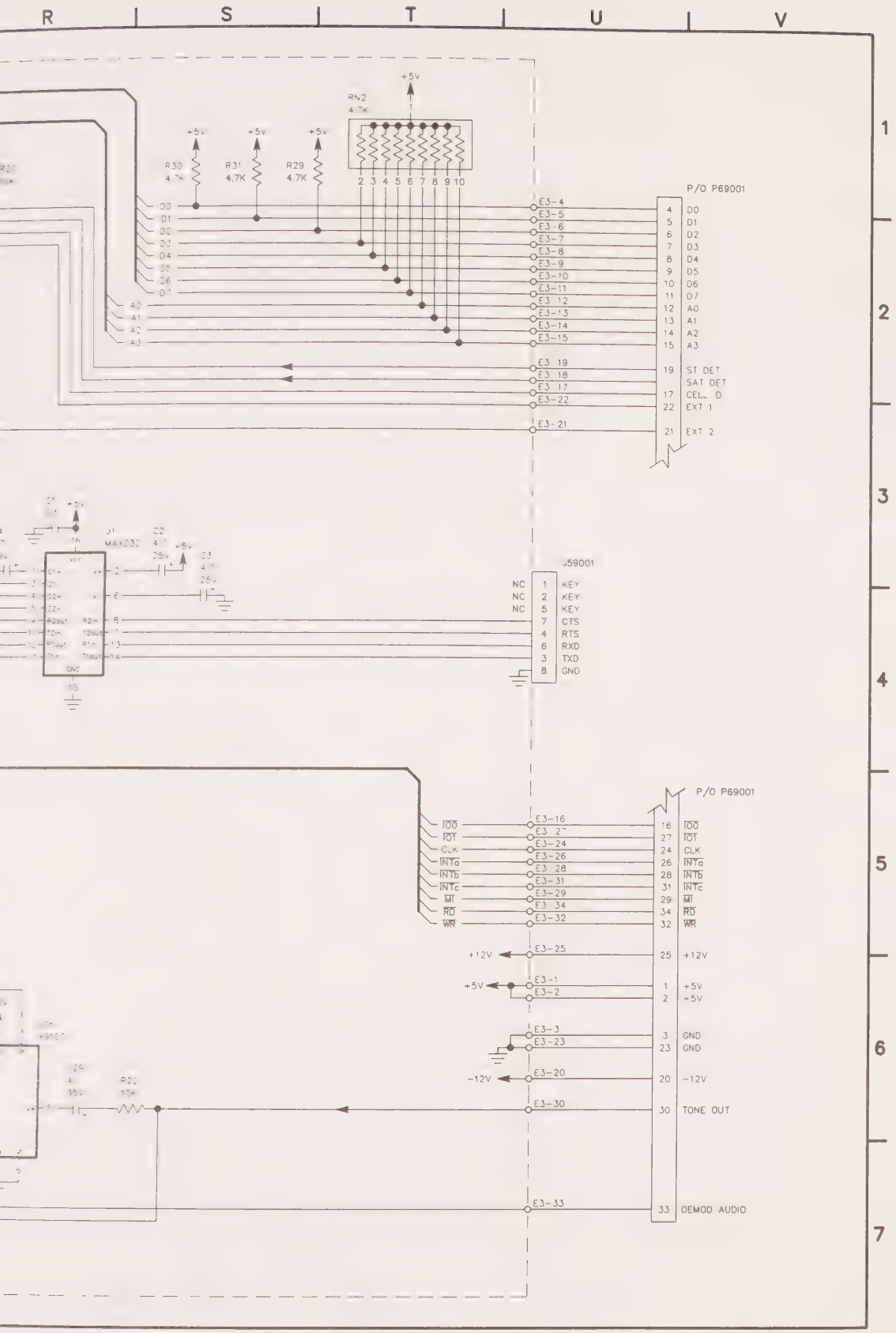
Figure 6-43 Audio Encode/Decode PC Board Assembly (Option) (0000-5710-000-C3)



FM/AM-1200S ENCODE/DECODE PC BOARD ASSY
(7010-7730-000-D7)

Figure 6-44 FM/AM-1200S Encode/Decode PC Board Assembly (Option) (Sheet 1 of 2) (0000-7710-000-D3)


CELLULAR ENCODE/DECODE (59000)
PCB0 1700-7720-000
PCB0 ASSY 7010-7730-000



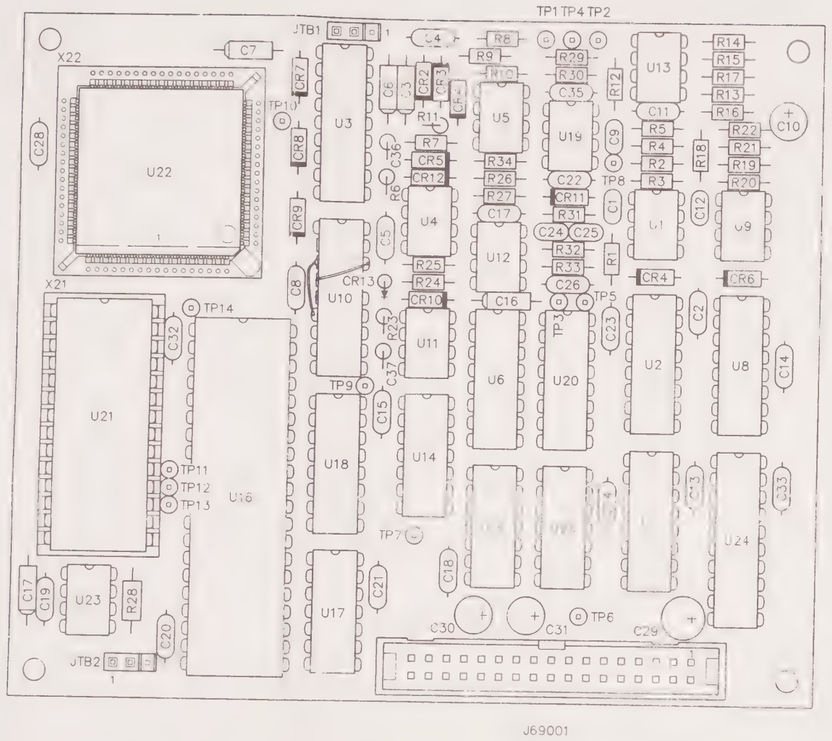
NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 59000 (I.E., R1 IS R59001).

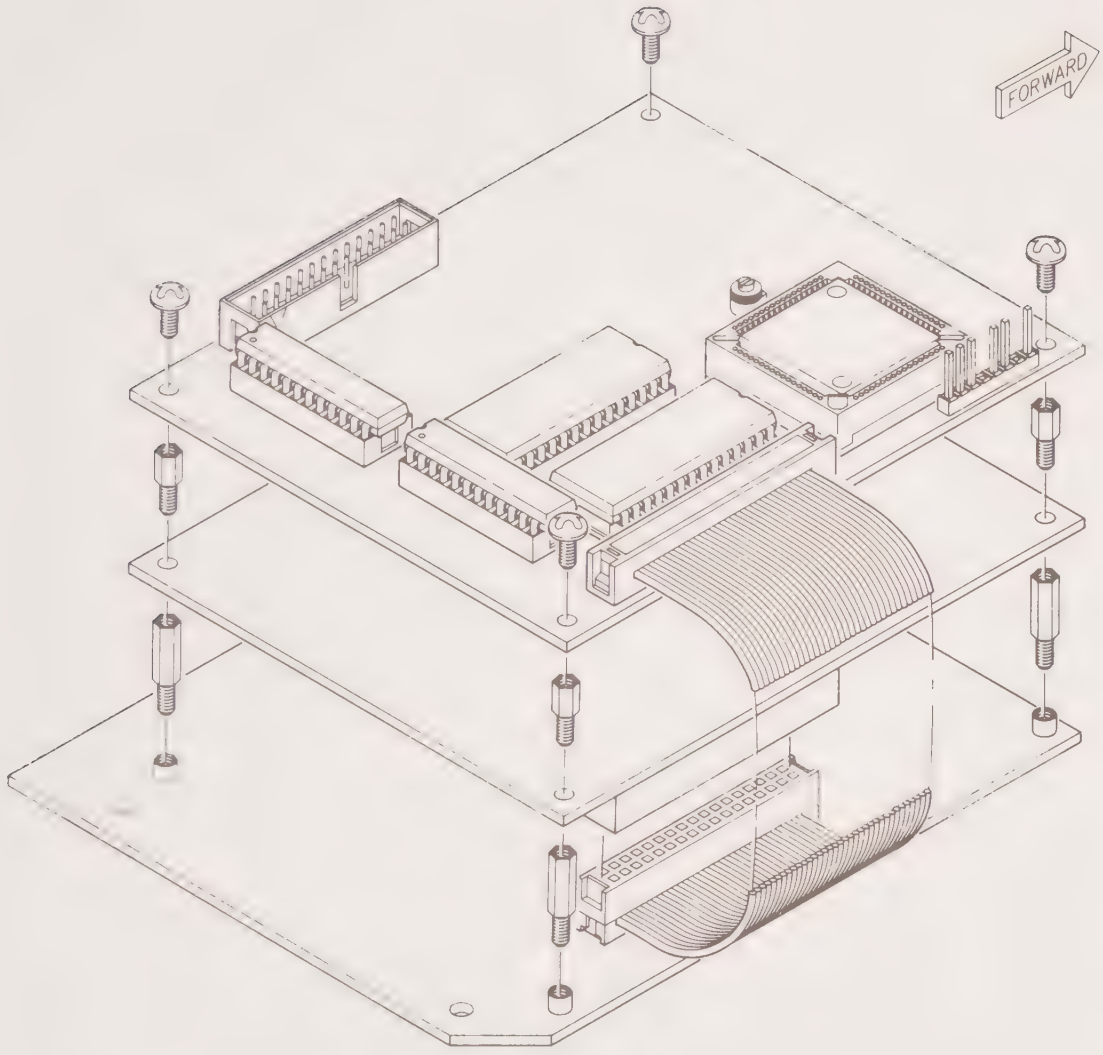
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; AND ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

Figure 6-44 FM/AM-1200S Encode/Decode PC Board Assembly (Option) (Sheet 2 of 2) (0000-7710-000-D3)

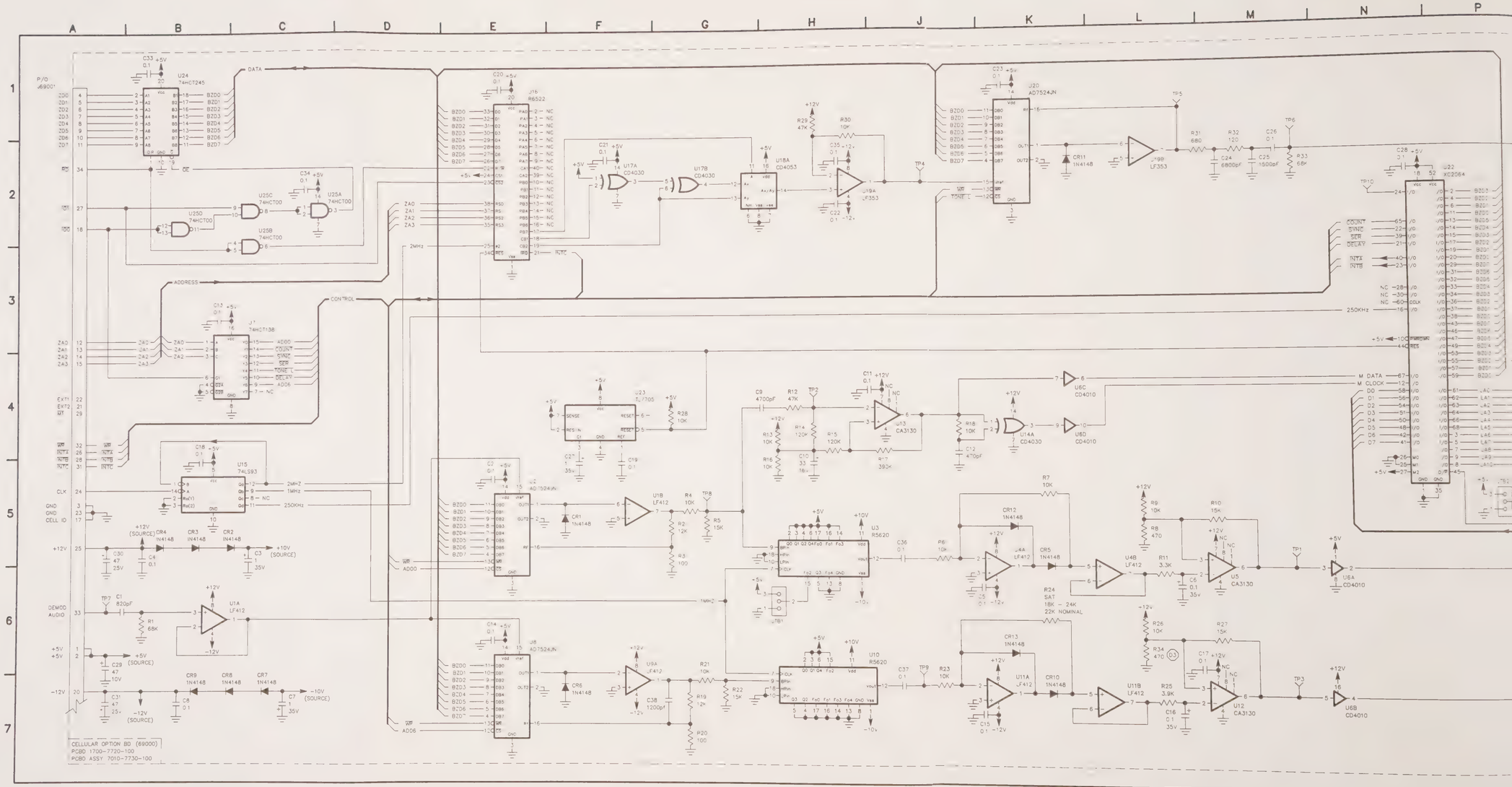


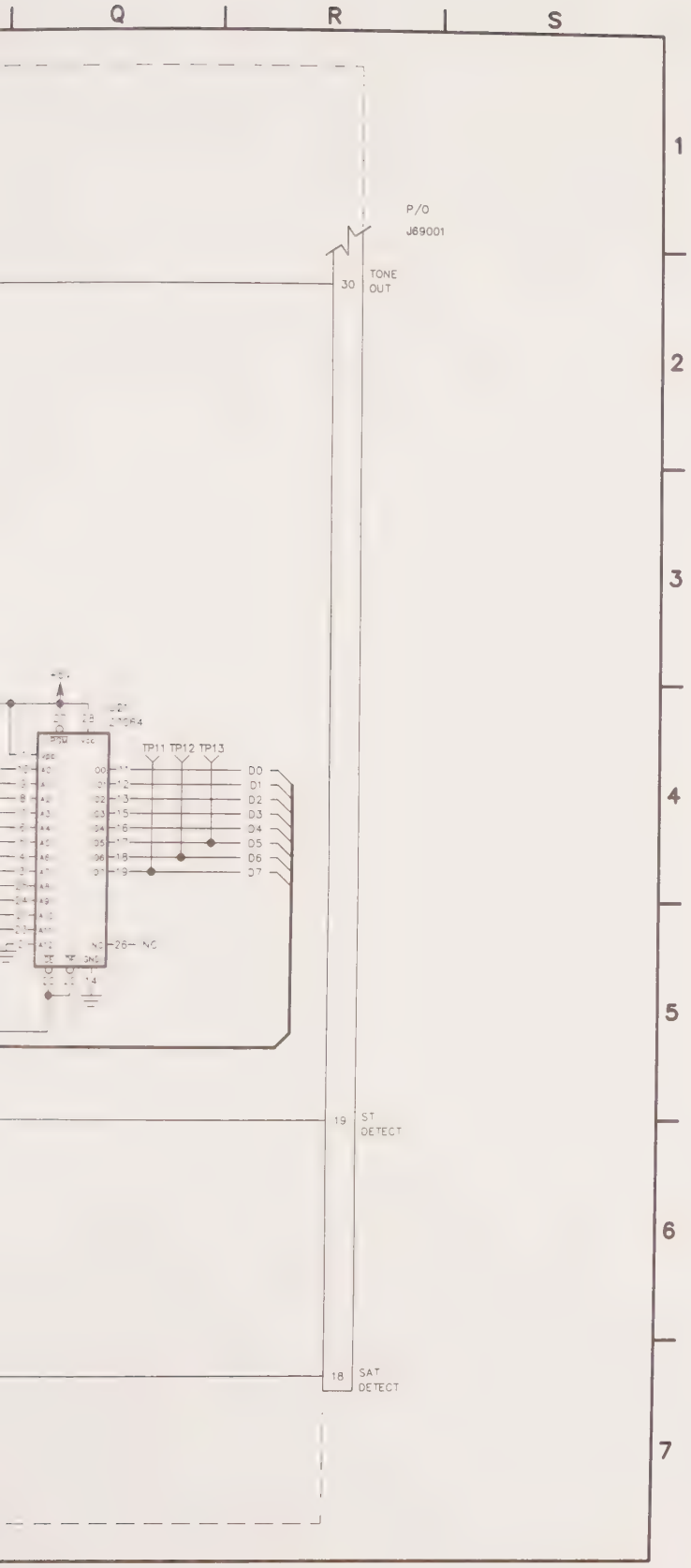
CELLULAR OPTION PC BOARD ASSY
(FM/AM-1200S) (7010-7730-100-D7)



CELLULAR OPTION ASSY (FM/AM-1200S)
(7005-7740-100-B)

Figure 6-45 FM/AM-1200S Cellular PC Board Assembly (Option) (Sheet 1 of 2) (0000-7710-100-D5)


CELLULAR OPTION BD (69000)
PCBD 1700-7720-100
PCBD ASSY 7010-7730-100



NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 69000 (I.E., R1 IS R69001).

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE, UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS; ALL CAPACITANCE IS EXPRESSED IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

Figure 6-45 FM/AM-1200S Cellular PC Board Assembly (Option) (Sheet 2 of 2) (0000-7710-100-D5)

APPENDICES

APPENDIX A - FM/AM-1200S/A SPECIFICATIONS

A-1 RF SIGNAL GENERATOR

Frequency Range:	250 kHz to 999.9999 MHz in 100 Hz increments.
Frequency Accuracy:	(See Master Oscillator)
Residual FM:	<100 Hz RMS peak (300 Hz to 3 kHz Bandwidth)
Harmonics:	2nd Harmonic ≤-30 dBc 3rd Harmonic ≤-45 dBc
Non-Harmonics & Spurious: (at offset from selected frequency)	±10 kHz to ±1.5 MHz: ≤-30 dBc in band, ±1.5 MHz to band end: ≤-55 dBc (IF Image -35 dBc)
RF Output Power: (At T/R Connector)	-127 dBm to -20 dBm (10 dB steps with 11 dB range vernier) into 50Ω.
RF Output Accuracy:	±2.5 dB
Variable Generate:	When in the "locked" position, the generator is phase-locked to the master oscillator. When switched from the "locked" position, the generator may be varied ±10 kHz.
Internal Modulation:	
Deviation Range:	0 to 50 kHz (with 1 kHz tone).
% AM Range:	0 to 90% (with 1 kHz tone).
External Modulation:	
Frequency Response:	FM: 2 Hz to 30 kHz (DC when in variable generate). AM: 10 Hz to 10 kHz (30% maximum modulation above 5 kHz).
Modulation Sensitivity: (at 1 kHz sine)	FM: 0.1 VRMS/kHz (-0 to +30%) AM: 0.01 VRMS/% (-0 to +30%)
Distortion: (at 1 kHz sine)	FM: <1%: to 20 kHz deviation AM: <10% to 60% modulation
Input Impedance:	10 KΩ nominal.

A-2 DUPLEX GENERATOR

Frequency Range: ±49.99 MHz from receive frequency in 10 kHz steps.

Frequency Resolution: 2.5 kHz

Frequency Accuracy: (See Master Oscillator)

Output Level:

Duplex Port: -60 dBm (±10 dB) fixed level into 50 Ohm (FM/AM-1200A)

Duplex High: (FM/AM-1200S) -15 dBm (±10 dB) ±49.99 MHz from receive frequency.

Duplex Low: (FM/AM-1200S) -25 dBm (±5 dB) below Duplex High in the same frequency.

Input Protection: 0.25 WATT (maximum without damage)

Transmission Port: -80 dBm (±10 dB) fixed level
-85 dBm (±10 dB) fixed level

A-3 RECEIVE/MONITOR

Frequency Range: 100 kHz to 999.9999 MHz in 100 Hz increments.

Sensitivity: 2 µV typical (1 MHz to 1000 MHz, FM narrow).

Selectivity (at 3 dB):

MODE	RECEIVER BANDWIDTH	AUDIO BANDWIDTH
FM WIDE	200 kHz	80 kHz
FM MID	200 kHz	8 kHz
FM NAR	15 kHz	8 kHz
SSB	6 kHz	8 kHz
AM NAR	6 kHz	8 kHz
AM NORM	15 kHz	8 kHz

Adjacent Channel Rejection:

RECEIVER BANDWIDTH	GREATER THAN 40 dB DOWN
200 kHz	±300 kHz
15 kHz	±27 kHz
6 kHz	±12 kHz

Demodulation Output:

Impedance: 600 Ohms

Output Level:	(Into an open circuit): FM: 60 mVRMS/1 kHz (nominal) AM: 5 mVRMS/% (nominal)
Receiver Antenna:	
Input Protection:	0.25 WATT (maximum without damage)

A-4 POWER METER

Range:	0 to 15 WATTS and 0 to 150 WATTS peak or average responding.
Accuracy:	1 to 600 MHz (±7% of reading, ±3% of full scale). 600 to 1000 MHz (±20% of reading ±3% of full scale).
Input Power:	50 WATTS continuous >50 to 150 WATTS, one minute "ON", five minutes "OFF".

A-5 FREQUENCY ERROR METER

RF Accuracy:	±Master Oscillator ±3% of full scale
RF Ranges:	±10 kHz, ±3 kHz, ±1 kHz, ±300 Hz, ±100 Hz, ±30 Hz full scale
Audio Counter:	
Frequency Range:	10 Hz to 12 kHz
Accuracy:	±0.01%, ±3% of full scale
Ranges:	±300 Hz, ±30 Hz, ±3 Hz full scale

A-6 MODULATION METER

FM Deviation:	
Accuracy:	±5% of reading. ±3% of full scale for a 1 kHz tone.
Ranges:	2 kHz, 6 kHz, 20 kHz, 60 kHz full scale.
AM% Modulation:	
Accuracy:	±5% of reading. ±3% of full scale for a 1 kHz tone.
Ranges:	60%, 200% full scale.

A-7 SINAD DISTORTION METER

Sinad:	±3 to 20 dB at 1 kHz.
Accuracy:	±1 dB at 12 dB SINAD.
Input Level:	0.25 VRMS to 2 VRMS (10 VRMS maximum SINAD).
Distortion Range:	0 to 20% at 1 kHz.
Accuracy:	±1% at 10% distortion
Input Level:	0.25 VRMS to 2 VRMS 10 VRMS maximum

Impedance: 10 KΩ nominal.

A-8 FUNCTION GENERATOR

Functions:	SINE, SQUARE, RAMP, TRIANGLE, DTMF, TONE SEQ and DCS.
Tone Accuracy:	
Fixed:	(Same as Master Oscillator)
Variable:	±0.01%
Tone Distortion:	(At 2.5 VRMS output)
Fixed:	≤0.5%
Variable (SINE):	≤2% (10 Hz to 100 Hz) ≤0.7% typical (100 Hz to 30 kHz).
Tone Output Level:	Variable to 2.5 VRMS minimum, either tone into 150 Ohm load.
Frequency Range (Variable):	10 Hz to 30 kHz in 0.1 Hz increments.

DTMF ENCODE:

Deviation:	3.5 kHz Fixed (±500 Hz)
Mark Time:	50 msec Minimum
Space Time:	50 msec Minimum
DTMF Decode (Optional):	See Digital Voltmeter

A-9 OSCILLOSCOPE

Display Size:	2 inches X $2\frac{1}{2}$ inches (5.1 X 6.4 cm).
Vertical Bandwidth:	DC to 1 MHz (at 3 dB Bandwidth)
External Vertical:	
Input Ranges:	10 mV, 100 mV, 1V, 10V per division.
Horizontal Sweep:	
Rate:	FM/AM-1200A - 10 msec, 1 msec, 100 µsec, 10 µsec per division. 1 µsec per division.
	FM/AM-1200S - 10 msec, 1 msec, 100 µsec, 10 µsec per division.

A-10 MASTER OSCILLATOR

Standard TCXO:

Accuracy:	0.2 PPM (0 to 50° C)
Aging:	0.5 PPM per year
Optional Oven Oscillator:	(Option 02)
Stability:	0.5 PPM (0 to 50° C)
Aging:	0.25 PPM per year

A-11 GENERATE AMPLIFIER (Optional)

Gain:	30 ±2 dB typical, 250 kHz to 1000 MHz
Test Set Output with Amplifier Installed:	Variable to +10 dBm, FM, CW Variable to +4 dBm, AM

A-12 DIGITAL VOLTMETER (Optional)

AC Volts:

Frequency Range:	45 Hz to 10 kHz
Voltage Range:	0 to 100. VRMS
Accuracy:	±10% ±2 Counts

DC Volts:

Voltage Range:	0 to ±100 VDC
Accuracy:	±10% ±2 Counts

DTMF Decode:

Deviation:	1 kHz Minimum
Mark Time:	50 msec Minimum
Space Time:	50 msec Minimum
Sensitivity:	20 dB FM Quieting

A-13 GENERAL CHARACTERISTICS

Temperature Range:	0 to 50° C

A-14 POWER REQUIREMENTS

Line:	105 - 130/210 - 260 VAC 50 - 400 Hz at 60 WATTS typical.
Ext. DC:	12 - 30 VDC nominal; 3.5 AMPS at 12V typical; 1.5 AMPS at 28V, typical.

A-15 SPECTRUM ANALYZER (FM/AM-1200S Only)

Log Scale: Within 2 dB linearity from -30 dBm to -90 dBm indication.

Dynamic Range: 70 dB (from display reading of -30 to -100 dBm).

Modes:

SCAN WIDTH	BANDWIDTH
1 MHz/DIV	30 kHz
100 kHz/DIV	30 kHz
200 kHz/DIV	30 kHz
100 kHz/DIV	30 kHz
50 kHz/DIV	30 kHz
20 kHz/DIV	3 kHz
10 kHz/DIV	3 kHz
5 kHz/DIV	3 kHz
2 kHz/DIV	300 Hz
1 kHz/DIV	300 Hz

A-16 TRACKING GENERATOR

Frequency Range: 1 MHz to 999.9999 MHz

Output Levels:
HIGH: -5 dBm (+3/-5 dB)
MID: -15 dBm (±7 dB)
LOW: -40 dBm (+5/-10 dB)

Flatness: ±1 dB over center 80% of displayed area.
±5 dB over remaining 20% of display.

Tracking Span: 10 kHz to 10 MHz as set by spectrum analyzer scan width.

Output Impedance: 50Ω nominal.

Spurious: Harmonic and Non-Harmonics are <5 dBc, typically 10 dBc.
Image (RF +180 MHz) Typically 0 dBc.

Dynamic Range: >70 dB

Tracking Adjustment Range: -200 Hz to 1.0 kHz minimum as compared to analyzer center.

APPENDIX B - TEST EQUIPMENT REQUIREMENTS

B-1 GENERAL

This appendix contains a list of test equipment suitable for performing all of the maintenance procedures contained in this manual. Any other equipment meeting the specifications listed in this appendix may be substituted in place of the recommended models. It should be noted that the equipment listed in this appendix may exceed the minimum required specifications for some of the procedures contained in this manual.

B-2 RECOMMENDED TEST EQUIPMENT

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Oscilloscope	Tektronix 465B	DC to 100 MHz 5 mV/Div vertical trace 2 ns/Div sweep rate Dual Trace
Spectrum Analyzer	Tektronix 7613 Frame Oscilloscope Tektronix 7L13/U Spectrum Analyzer	Variable Persistance Storage Frequency Range: 1 kHz to 2.5 GHz Resolution Bandwidth: 30 Hz to 3 MHz
Tracking Generator	Tektronix TM503 Frame Tektronix TR502 Tracking Generator	Three-wide Mainframe Frequency Range: 100 kHz to 1.8 GHz Output Level: 0 dBm, ±0.5 dB Power Range: 0 to -59 dBm in 10 and 1 dB steps
Frequency Counter	Fluke Model 7220A	Frequency Range: 5 Hz to 1300 MHz
Digital Multimeter	Fluke Model 8010A	3 1/2 digit, ±0.1% basic DC accuracy
Distortion Analyzer	Sound Technology Model 1700B	Frequency Range: 10 Hz to 110 kHz Accuracy: .002% distortion AC Voltage Accuracy: 2%

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Function Generator	Wavetek 182A	Frequency Range: .004 Hz to 4 MHz Functions: Sine, Triangle & Square
Signal Generator	Hewlett Packard 8640B	Frequency Range: 1 to 1000 MHz Resolution: 0.1 to 100 Hz Accuracy: 2×10^{-6} RF Output: +20 to -130 dBm
Modulation Meter	Boonton Model 82AD	Frequency Range: 10 MHz to 1.2 GHz Accuracy: FM: ±2% of reading from 30 Hz to 100 kHz AM: ±2% of reading from 10 Hz to 90% AM and 5% below 10% and 90%; from 30 Hz to 100 kHz Resolution: 0.1% of full scale for FM and AM
RF Power Source	MCL 15122 Main Frame 6048 Oscillator Module	Frequency Range: 50 to 200 MHz Power Range: 0 to 65 W
RF Power Meter with Power Detector	Boonton RF Microwatt-meter Model 42 BD	Frequency Range: 200 kHz to 18 GHz Power Range: 1.0 nW to 10 mW Accuracy: ±0.25% fs ±0.15 dB >10 nW
	Boonton Power Sensor Model 41-4A	Frequency Range: 200 kHz to 7 GHz Power Range: 1 nW to 10 mW Accuracy: ±0.3 dB >10 nW
Power Supply	B&K 1601	Regulation: 0.1% or 1 mV Ripple: 5 mV Voltage Range: 0-50 VDC @ 0-2A

APPENDIX C - USER I/O PORTS/CONNECTORS PIN-OUT TABLES

C-1 TABLE OF I/O PORTS

CONNECTOR NAME	CONNECTOR TYPE	SIGNAL INPUT/OUTPUT	SIGNAL TYPE
T/R (11)	BNC	Input/Output	RF
AUX PWR (12)	Banana Jack	Output	+12 VDC
DUPLEX Output (14)	BNC	Output	RF
EXT MOD/SINAD (15)	BNC	Input/Output	Audio
DEMOD (16)	BNC	Output	Audio
TONE OUT (17)	BNC	Output	Audio
MIC/ACC (19)	5 Pin Microphone Connector	Input/Output	See Pin-Out
SCOPE/DVM (20)	BNC	Input	DC to 1 MHz; AC of DC
ANT (34)	BNC	Input	RF
RS-232 (43)	25 Pin, Type D	Input/Output	See Pin-Out
GPIB Option 13 (43)	24 Pin, GPIB	Input/Output	See Pin-Out
AC Power (44)	EAC-301	Input	105-130/ 210-260 VAC
DC Power (45)	712A	Input	12-30 VDC
External Reference (46)	BNC	Input/Output	10 MHz RF

Table C-1 Table of I/O Ports

C-2 PIN-OUT TABLE FOR MIC/ACC CONNECTOR

PIN NO.	SIGNAL NAME	SIGNAL TYPE	INPUT/OUTPUT
1	+12 VDC	DC Voltage	1/8 AMP Fused Output
2	Chassis END		
3	Mic Key	Switched	GND for Generate
4	Mic Audio	Audio	Input
5	Tone Key	Switched	GND to Remove Variable To

Table C-2 MIC/ACC Connector Pin Assignments

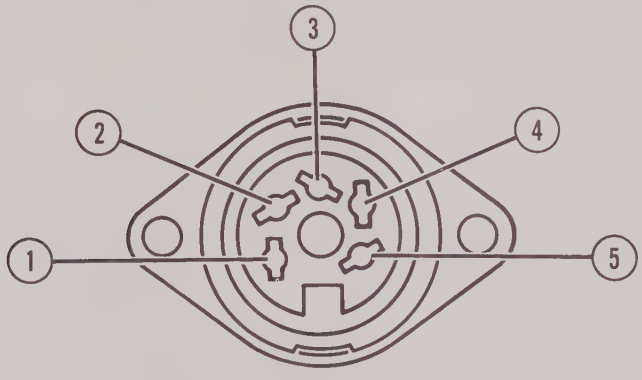


Figure C-1 MIC/ACC Connector Pin Identification
(Front View)

C-3 PIN-OUT TABLE FOR RS-232 CONNECTOR

The FM/AM-1200S/A is configured as Data Terminal Equipment (DTE)

Pin No.	Input/Output	Remarks
2 (RDX)	← Commands	
3 (TDX)	Info →	
4 (RTS)	→	If high, FM/AM-1200S/A can command If low, FM/AM-1200S/A busy.
5 (CTS)	←	If low, terminal not ready to receive. If not used, it must be tied high.
7 (Common Ground)		
1, 6, and 8 thru 25 not used		

Table C-3 RS-232 Connector Pin Assignments (Standard)

NOTE: A special cable (to be configured by the user) may be necessary to interface the RS-232 port to an external controller and/or printer.

FM/AM-1200S/A PROTOCOL

No Parity	Bit 8 Must Be Zero (Most Significant)
Must Be Half Duplex	1 Stop BIT (End of Character)
Must Be Upper Case	High Level = -12V
8 Data Bits Per Character	Low Level = +12V

Pin No.	Assignment
7	Common Ground
13	CTS
14	RDX
16	TDX
18	GND
19	RTS
1 thru 6, 8 thru 12, 15, 17, 20 thru 25	Not Used

Table C-4 RS-232 Connector Pin Assignments with Cellular Testing (Option 15) Installed

C-4 PIN-OUT TABLE FOR GPIB CONNECTOR (OPTION 13)

When the GPIB Option (Option 13) is installed, a 24-pin connector is available on the rear panel for connection to an external controller Pin-Outs are shown in Table C-5 below. The operator should ensure proper interface between the FM/AM-1200S/A and the external roller.

Once the proper external controller connection is made, the FM/AM-1200S/A can be initialized with the proper address by using the GPIB Menu.

Pin No.	Signal	Pin No.	Signal
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	Ground
7	NRFD	19	Ground
8	NDAC	20	Ground
9	IFC	21	Ground
10	SRQ	22	Ground
11	ATN	23	Ground
12	Ground	24	Ground

Table C-5 Pin-Out Table for GPIB Connector

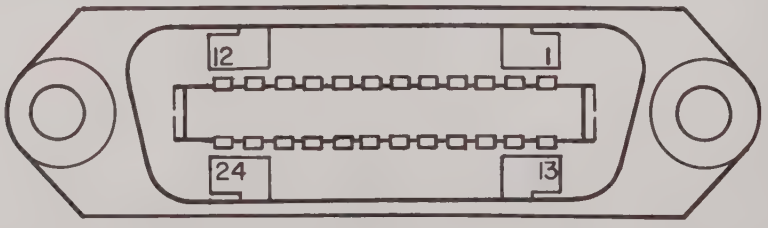


Figure C-2 GPIB Connector Pin Identification

APPENDIX D - SPECIAL ACCESSORY TEST EQUIPMENT

D-1 GENERAL

This appendix contains recommendations for constructing special equipment necessary for performing certain test procedures in this manual.

D-2 BATTERY LOAD SIMULATOR

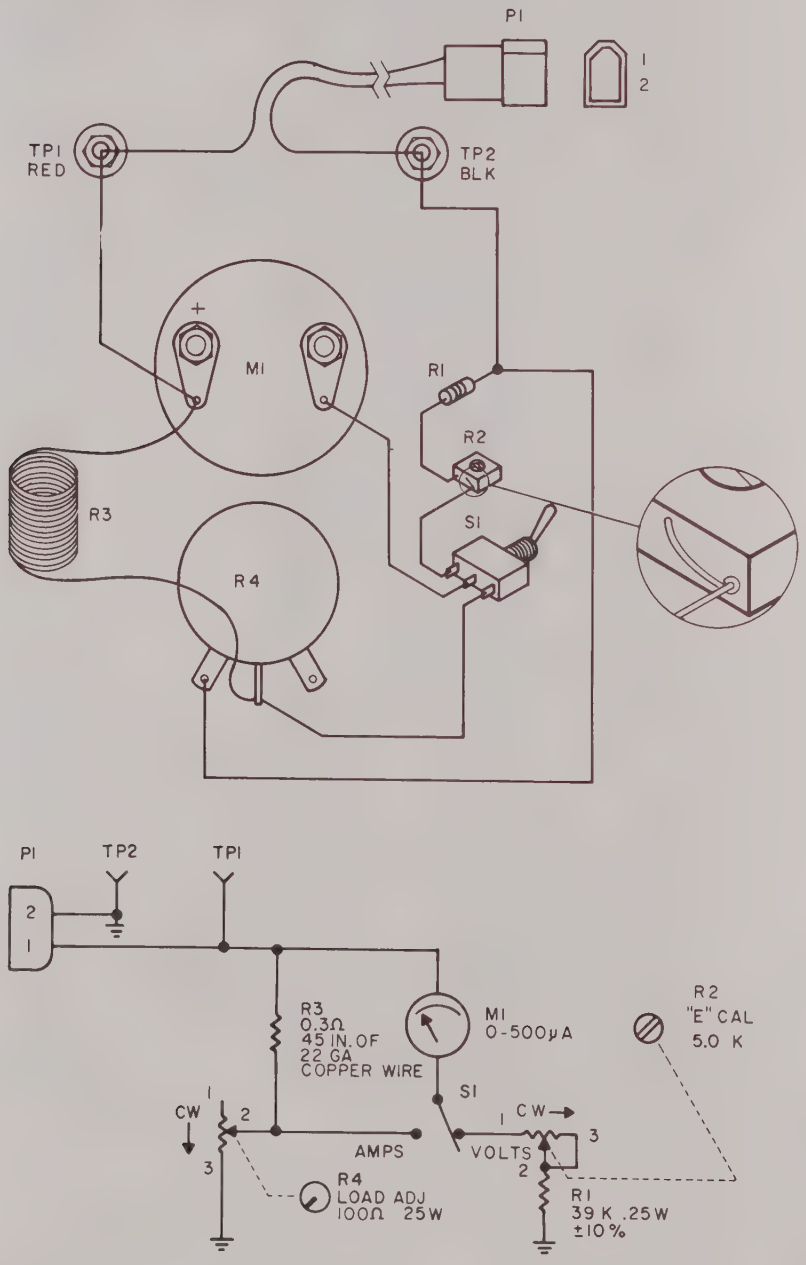
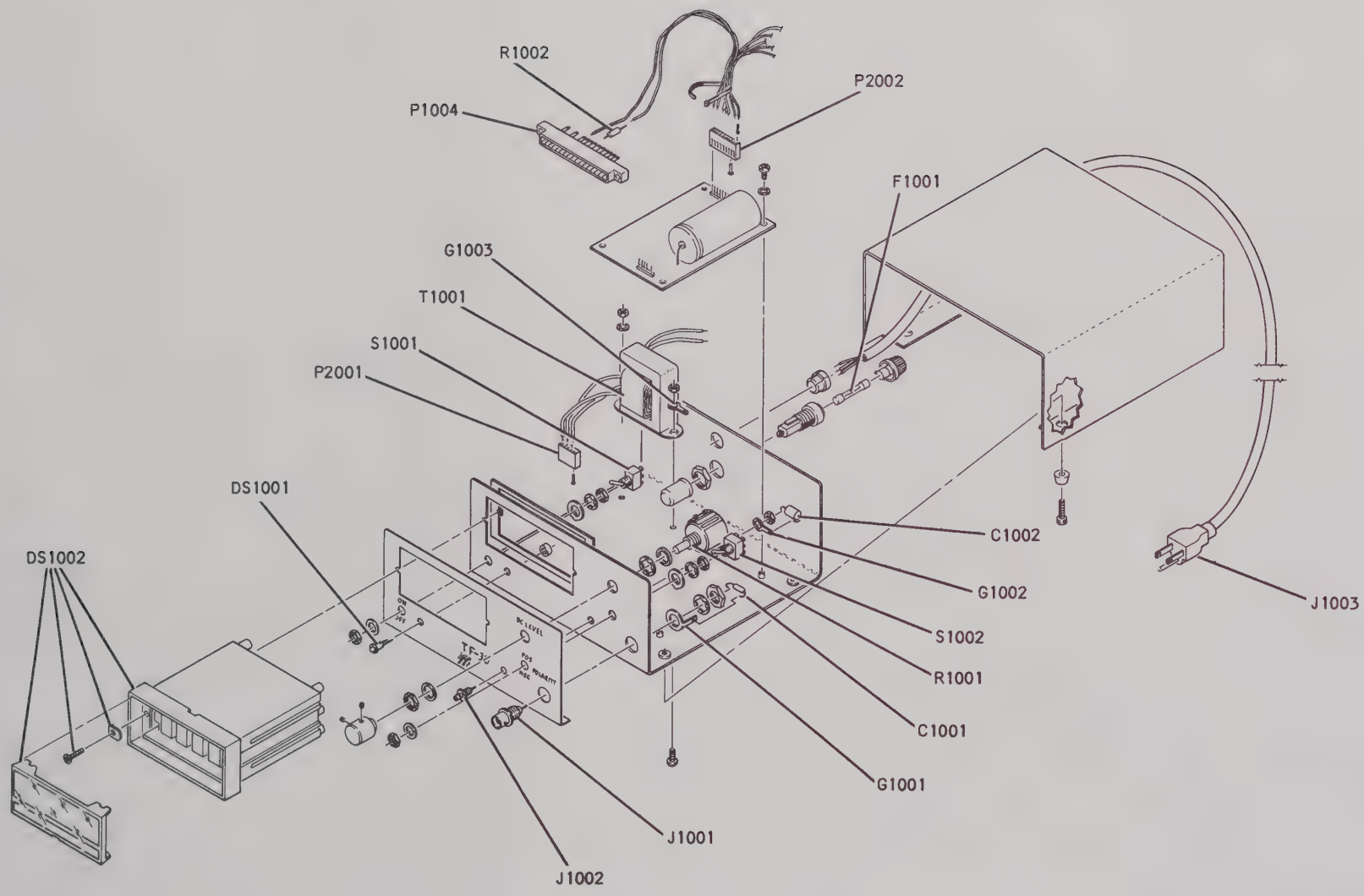


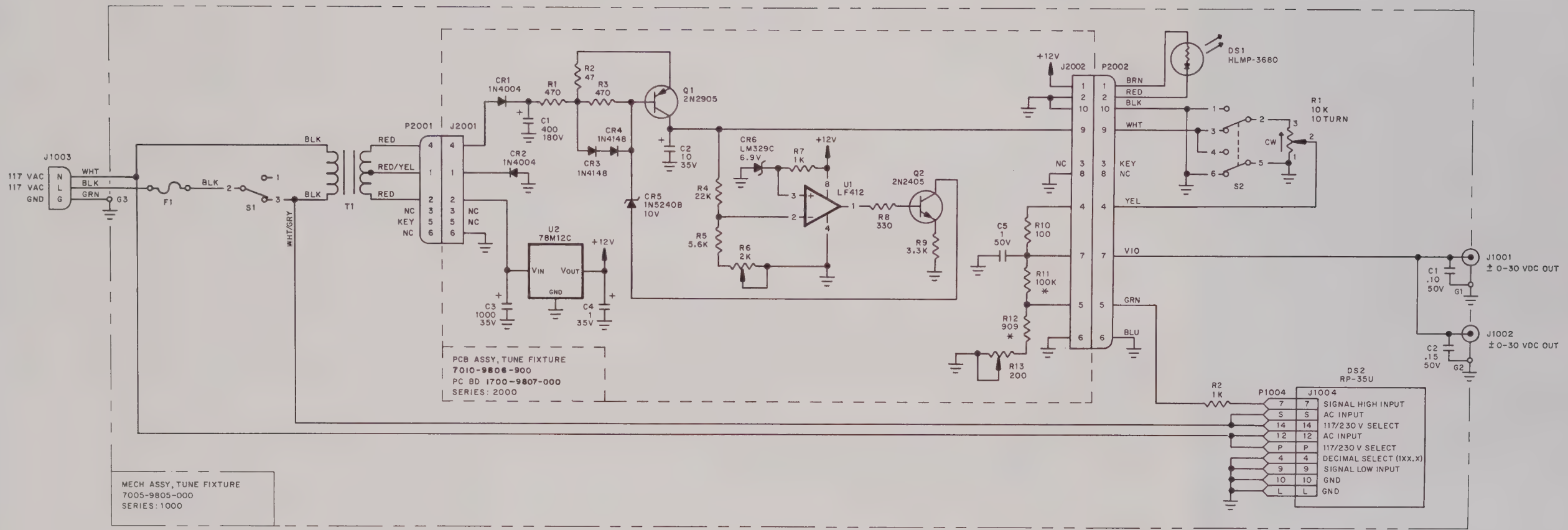
Figure D-1 Circuit Schematic and Diagram of Battery Load Simulator

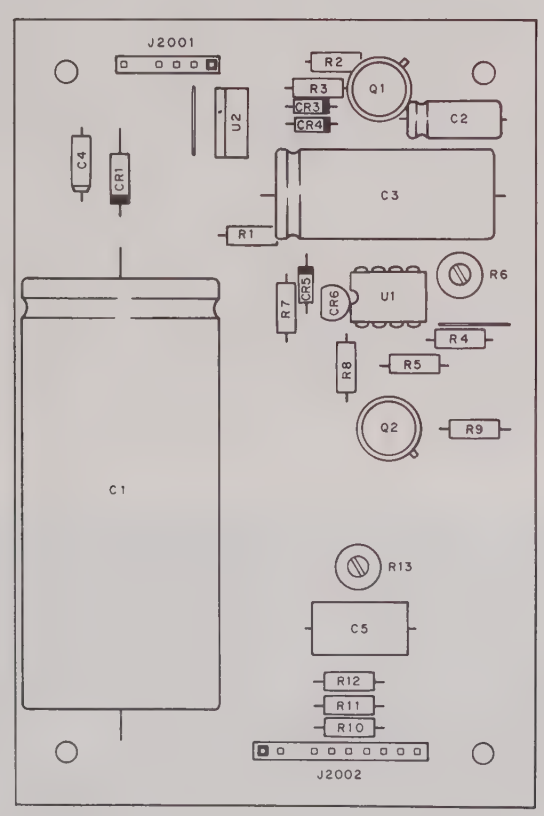
D-3 TF-30 TUNE FIXTURE



REF DES	DESCRIPTION	IFR PART NO.	QTY
	TUNE FIXTURE ASSEMBLY		
J1001	CONNECTOR, BNC	2113-0000-020	1
J1002	CONNECTOR, SMB	2123-0000-038	1
J1003	CABLE ASSY, AC POWER	6041-0000-001	1
P1004	CONNECTOR, CARD EDGE	2122-0000-018	1
P2001	CONNECTOR, WAFER	2115-0000-006	1
P2002	CONNECTOR, WAFER	2115-0000-013	1
C1001	CAPACITOR .10 µF, 50 V	1521-0000-008	1
C1002	CAPACITOR .15 µF, 50 V	1646-1540-098	1
DS1001	LED GRN	4950-0300-200	1
DS1002	DISPLAY, DIGITAL VOLTMETER	4600-0000-006	1
F1001	FUSE, FAST BLO 1 A, 250 V		1
G1001	LUG, GND 3/8"	2850-0000-025	1
G1002	LUG, GND 3/8"	2850-0000-041	1
G1003	LUG, GND #4 INT TOOTH	2850-0000-014	1
R1001	RESISTOR, VAR 10 K	4770-8810-300	1
R1002	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
S1001	SWITCH, TOGGLE	5114-0000-001	1
S1002	SWITCH, TOGGLE	5114-0000-004	1
T1001	TRANSFORMER	5604-0000-002	1
	TUNE FIXTURE, PC BD	7010-9806-900	1
J2001	CONNECTOR, WAFER	2115-1001-006	1
J2002	CONNECTOR, WAFER	2115-0000-016	1
C2001	CAPACITOR 400 µF, 180 V	1580-4010-800	1
C2002	CAPACITOR 10 µF, 35 V	1580-1000-350	1
C2003	CAPACITOR 1000 µF, 35 V	1580-1020-358	1
C2004	CAPACITOR 1 µF, 35 V	1507-0105-118	1
C2005	CAPACITOR 1 µF, 50 V	1502-0105-007	1
CR2001	DIODE, RECT IN4004	4815-0000-002	1
CR2002	DIODE, RECT IN4004	4815-0000-002	1
CR2003	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2004	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2005	DIODE, ZENER 10 V	4818-0000-001	1
CR2006	DIODE, ZENER 6.9 V	4818-0000-015	1
Q2001	TRANSISTOR 2N2905	4801-0000-004	1
Q2002	TRANSISTOR 2M2405	4801-0000-002	1
R2001	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2002	RESISTOR 5%, 1/4 W, 47 OHM	4702-0470-003	1
R2003	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2004	RESISTOR 5%, 1/4 W, 22 K	4702-0223-003	1
R2005	RESISTOR 5%, 1/4 W, 5.6 K	4702-0562-003	1
R2006	RESISTOR, VAR 2 K	4752-0202-002	1
R2007	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
R2008	RESISTOR 5%, 1/4 W, 330 OHM	4702-0331-003	1
R2009	RESISTOR 5%, 1/4 W, 3.3 K	4702-0332-003	1
R2010	RESISTOR 5%, 1/4 W, 100 OHM	4702-0101-003	1
R2011	RESISTOR 1%, 1/4 W, 100.00 OHM	4706-1003-001	1
R2012	RESISTOR 1%, 1/4 W, 909.00 OHM	4706-9090-001	1
R2013	RESISTOR, VAR 200 OHM	4752-0201-002	1
U2001	IC, DUAL J-FET OP AMP LF412	3135-0000-054	1
U2002	IC, REGULATOR 78M12C	5750-0000-010	1
	WIRE, BUS 22 GA	1050-0000-073	

Figure D-2 TF-30 Tune Fixture Assembly (Sheet 1 of 2)





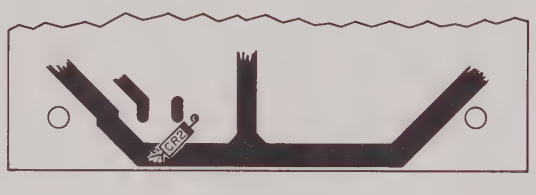


Figure D-2 TF-30 Tune Fixture Assembly (Sheet 2 of 2)

APPENDIX E - dBm TO MICROVOLT CONVERSION CHART

dBm	µV	dBm	µV	dBm	µV
0	223,607	-47	1,000	-94	4.46
-1	199,290	-48	890	-95	3.98
-2	177,617	-49	793	-96	3.54
-3	158,302	-50	707	-97	3.16
-4	141,086	-51	630	-98	2.82
-5	125,743	-52	562	-99	2.51
-6	112,069	-53	501	-100	2.24
-7	99,882	-54	446	-101	1.99
-8	89,020	-55	398	-102	1.78
-9	79,339	-56	354	-103	1.58
-10	70,711	-57	316	-104	1.41
-11	63,021	-58	282	-105	1.26
-12	56,168	-59	251	-106	1.12
-13	50,059	-60	224	-107	1.00
-14	44,615	-61	199	-108	0.890
-15	39,764	-62	178	-109	0.793
-16	35,439	-63	158	-110	0.707
-17	31,585	-64	141	-111	0.630
-18	28,150	-65	126	-112	0.562
-19	25,089	-66	112	-113	0.501
-20	22,361	-67	100	-114	0.446
-21	19,929	-68	89.0	-115	0.398
-22	17,762	-69	79.3	-116	0.354
-23	15,830	-70	70.7	-117	0.316
-24	14,109	-71	63.0	-118	0.282
-25	12,574	-72	56.2	-119	0.251
-26	11,207	-73	50.1	-120	0.224
-27	9,988	-74	44.6	-121	0.199
-28	8,902	-75	39.8	-122	0.178
-29	7,934	-76	35.4	-123	0.158
-30	7,071	-77	31.6	-124	0.141
-31	6,302	-78	28.2	-125	0.126
-32	5,617	-79	25.1	-126	0.112
-33	5,006	-80	22.4	-127	0.100
-34	4,462	-81	19.9	-128	0.0890
-35	3,976	-82	17.8	-129	0.0794
-36	3,544	-83	15.8	-130	0.0707
-37	3,159	-84	14.1	-131	0.0630
-38	2,815	-85	12.6	-132	0.0562
-39	2,509	-86	11.2	-133	0.0501
-40	2,236	-87	10.0	-134	0.0446
-41	1,993	-88	8.90	-135	0.0398
-42	1,776	-89	7.93	-136	0.0354
-43	1,583	-90	7.07	-137	0.0316
-44	1,411	-91	6.30	-138	0.0282
-45	1,257	-92	5.62	-139	0.0251
-46	1,121	-93	5.01	-140	0.0224

APPENDIX F - REPACKING FOR SHIPMENT

F-1 SHIPPING INFORMATION

IFR test sets returned to factory for calibration, service or repair must be repackaged and shipped subject to the following conditions:

Do not return any products to factory without first receiving authorization from IFR Customer Service Department.

CONTACT:

Customer Service Dept.
IFR Systems, Inc.
10200 West York Street
Wichita, Kansas 67215

Telephone: (800)-835-2350
TWX: 910-741-6952

All test sets must be tagged with:

a. Owner's identification and address.
b. Nature of service or repair required.
c. Model No.
d. Serial No.

Sets must be repackaged in original shipping containers using IFR packing materials. If original shipping containers and materials are not available, contact IFR Customer Service Dept. for shipping instructions.

All freight costs on non-warranty shipments are assumed by customer. (See "Warranty Packet" for freight charge policy on warranty claims.)

F-2 REPACKING PROCEDURE (Reference Figure F-1):

1. Make sure bottom packing mold is seated on floor of shipping container.

2. Carefully wrap test set with polyethylene sheeting to protect finish.

3. Place test set into shipping container, making sure set is securely seated in bottom packing mold.

4. Place top packing mold over top of set and press down until mold rests solidly on bottom packing mold.

5. Close shipping container lids and seal with shipping tape or an industrial stapler. Tie all sides of container with break resistant rope, twine or equivalent.

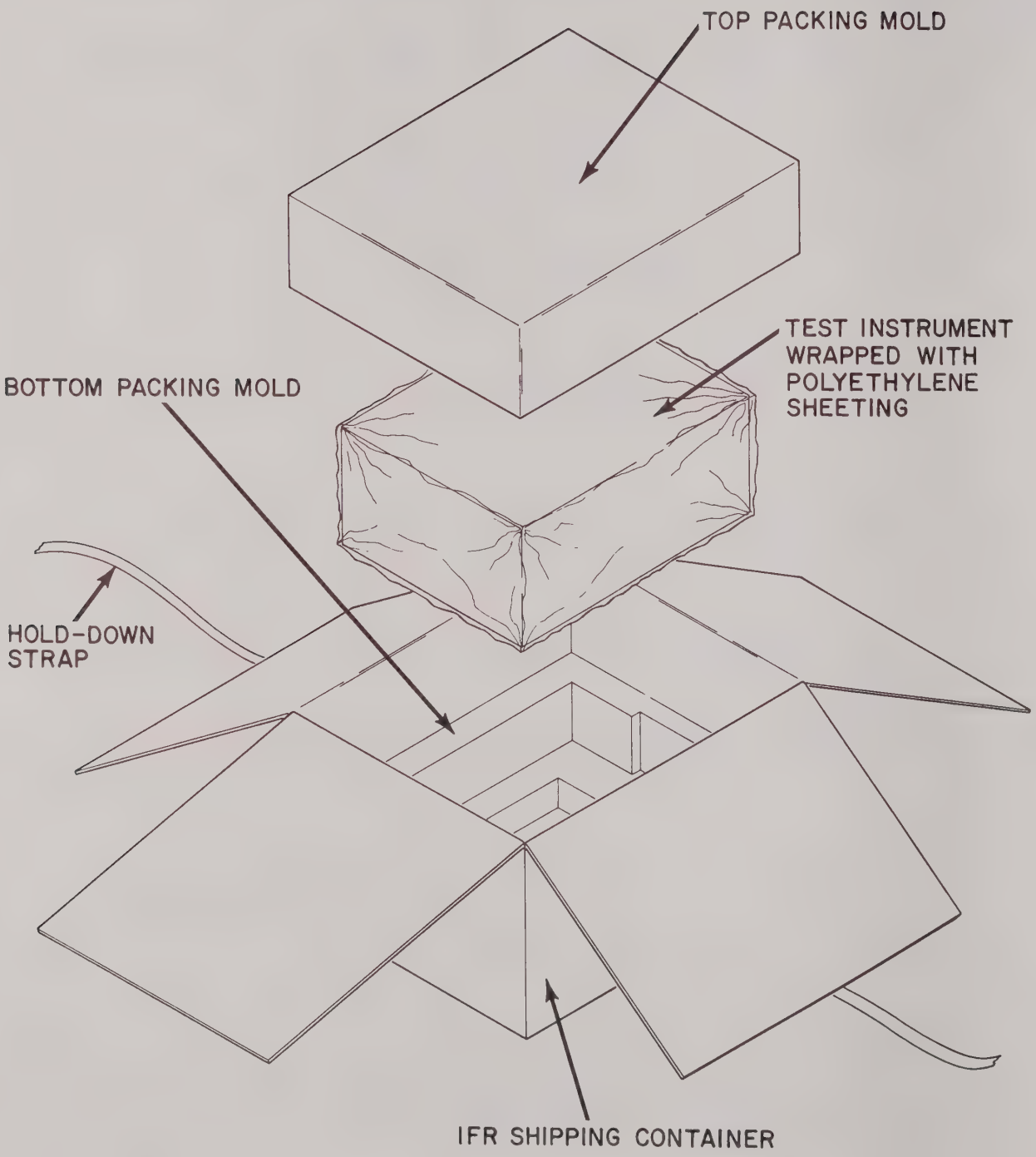


Figure F-1 Repacking for Shipment

APPENDIX G - ABBREVIATIONS & SYMBOLS

G-1 GENERAL

Defined below are various abbreviations and symbols which are commonly used throughout the FM/AM-1200S/A Maintenance Manual text.

G-2 GENERAL ABBREVIATIONS

A	- Ampere
AC or ac	- Alternating Current
Adj	- Adjustment
AGC	- Automatic Gain Control
AM	- Amplitude Modulation
Amp	- Ampere
ANALY DISP.	- Analyzer Dispersion
Assy	- Assembly
BATT	- Battery
BCD	- Binary Coded Decimal
BFO	- Beat Frequency Oscillator
°C	- Degrees Celsius
CAL	- Calibration
ccw	- Counterclockwise
CRT	- Cathode Ray Tube
cw	- Clockwise
CW	- Carrier Wave
DAC	- Digital to Analog Converter
dB	- decibels
dBc	- decibels above or below carrier level
dBm	- decibels above (or below) 1 milliwatt
DC or dc	- Direct Current
DCR	- Duty Cycle Regulator
DEFLEC AMP	- Deflection Amplifier
DEMOD	- Demodulation, demodulate or demodulated
DEV	- Deviation
DMM	- Digital Multimeter
DVM	- Digital Voltmeter
ECL	- Emitter Coupled Logic
EXT ACC	- External Accessory
EXT MOD	- External Modulation
EXT DC	- External Direct Current
°F	- Degrees Fahrenheit
FET	- Field Effect Transistor
FILT	- Filter
FM	- Frequency Modulation
FREQ	- Frequency
GEN	- Generate
GHz	- Gigahertz
GND	- Ground
HI LVL	- High Level
HORIZ	- Horizontal

Hz	- Hertz
IC	- Integrated Circuit
IF	- Intermediate Frequency
IMTS	- Improved Mobile Telephone System
INT MOD	- Internal Modulation
IPC	- Illustrated Parts Catalog
Kg/cm^3	- Kilogram per cubic centimeter
kHz	- kilohertz
LC	- Inductance filter
L/H	- Left-hand
LOG LIN	- Logarithmic Linearity
LO	- Local Oscillator
mA	- Milliamperes
MAX DISP	- Maximum Dispersion
Mech	- Mechanical
MHz	- Megahertz
MOD	- Modulation
MON	- Monitor
MTR	- Meter (display)
µs	- microsecond
µV	- microvolt
ms or mSec	- millisecond
mV	- millivolt
mW	- milliwatt
MULT	- Multiplier
NC	- Not Connected
N/A	- Not Applicable, Not Appropriate
NORM	- Normal
OSC	- Oscillator
para	- paragraph
PC Bd	- Printed Circuit Board
PLL	- Phase Lock Loop
Preamp	- Preamplifier
psi	- pounds per square inch
PWR	- Power
PWR MON	- Power Monitor
RAM	- Random Acess Memory
R-C	- Resistance Capacitance (network, filter)
RCVR	- Receiver
REF	- Reference
RF	- Radio Frequency
R/H	- Right-hand
RMS	- Root Mean Square
ROM	- Read Only Memory
s or sec	- Seconds
Scope Dev	- Oscilloscope Deviation
SIG	- Signal
SSB	- Signal Sideband
TCXO	- Temperature Compensated Crystal Oscillator
TRANS	- Transmitter or Transceiver
TTL	- Transistor Transistor Logic
V	- Volts

Vp - Volts Peak
Vp-p - Volts Peak-to-Peak
VAC - Volts Alternating Current
VCO - Voltage Controlled Oscillator
VDC - Volts Direct Current
VHG - Very High Frequency
VOL - Volume
VRMS - Volts Root Mean Square
VSWR - Voltage Standing Wave Ratio
W - Watts
XMTR - Transmitter
XTAL - Crystal

G-3 ABBREVIATIONS FOR REFERENCE DESIGNATORS

BR - Bridge Rectifier
C - Capacitor
CR - Diode
DS - Display Lamps
E - Terminal
FL - Feed-thru Filter
G - Oscillator
J - Connector (Fixed)
K - Relay
L - Inductor
M - Meter
MXR - Mixer
P - Connector (Movable)
Q - Transistor
R - Resistor
S - Switch
T - Transformer
TU - Tuning Pole
U - Integrated Circuit
VR - Voltage Regulator
Y - Crystal
YFL - Crystal Filter

APPENDIX H - OPTIONAL GENERATE AMPLIFIER (OPTION 05)

H-1 GENERAL

The Generate Amplifier is a 30 dB amplifier intended to increase the output level of a generated signal above the normal maximum level of the service monitor. It is not designed to receive any signal directly from a Unit Under Test (UUT); however, if properly installed, it can be used to transmit and receive signals "off the air," using the antenna.

CAUTION: TRANSMITTING FROM A UUT DIRECTLY INTO THE GENERATE AMPLIFIER OR THROUGH AN EXTERNAL ATTENUATOR WILL DAMAGE THE GENERATE AMPLIFIER AND/OR THE SERVICE MONITOR. DO NOT TRANSMIT FROM THE UUT DIRECTLY INTO THE GENERATE AMPLIFIER OR THROUGH AN EXTERNAL AMPLIFIER.

H-2 INSTALLATION

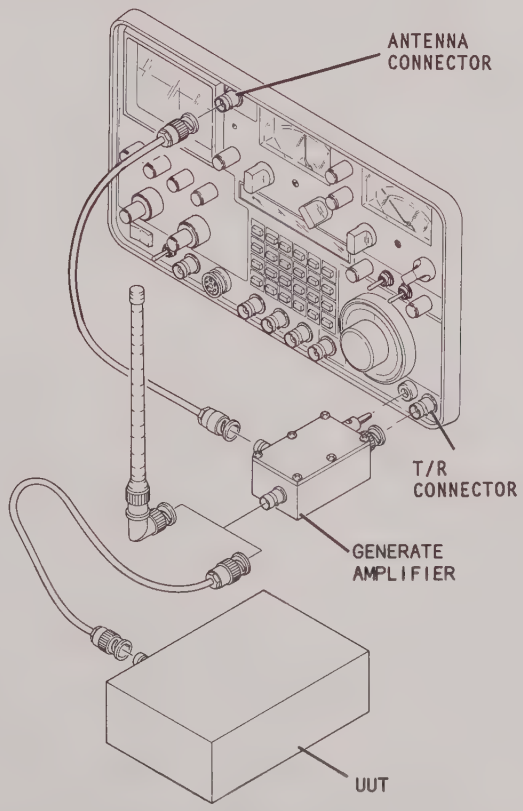
Insert the banana plug on the Generate Amplifer into the AUX PWR Connector on the Front Panel of the Service Monitor and connect the BNC connector to the T/R Connector.

For Direct Connection to UUT:

Connect coax cable between the UUT Test Connector on the Generate Amplifier and the Microphone Connector or other audio input on the UUT.

For Radio Installation Checkout:

WARNING: THIS TEST MUST BE PERFORMED WITH THE SERVICE MONITOR AND UUT INSIDE A SHIELDED AREA TO PREVENT UNRESTRICTED RADIATION OR RF SIGNALS.



Connect coax between Antenna Connector on the Front Panel of the Service Monitor and the Antenna Connector on the Generate Amplifier. Connect accessory antenna to the UUT Test Connector on the Generate Amplifier.

H-3 OPERATION

Refer to FM/AM-1200S/A Operation Manual, Section 4 and perform the procedures for generating and receiving RF signals.

APPENDIX J - FM/AM-1200S OPTION COMBINATIONS SOFTWARE/FIRMWARE NUMBERS

FM/AM-1200S Software Version 5.2-XX

EPROM U67003, DPN 3271-7752-2XX

EPROM U67004, DPN 3271-7752-1XX

If "XX" is:	Options installed are:
01	Tracking Generator
02	Trunking
03	Tracking Generator, Trunking
04	Cellular
05	Tracking Generator, Cellular
06	Trunking, Cellular
07	Tracking Generator, Trunking Cellular
08	Not Used
09	Not Used
10	Encode-Decode (European Signaling)
11	Tracking Generator, Encode-Decode
12	Trunking, Encode-Decode
13	Tracking Generator, Trunking, Encode-Decode
14	Cellular, Encode-Decode
15	Tracking Generator, Cellular, Encode-Decode
16	Trunking, Cellular, Encode-Decode
17	Tracking Generator, Trunking, Cellular, Encode-Decode

Option Combinations with Tracking Generator (Option 12)

Options Desired	Firmware #
Tracking Generator	01
Tracking Generator Trunking	03
Tracking Generator Cellular	05
Tracking Generator Encode-Decode	11
Tracking Generator Trunking Encode-Decode	13
Tracking Generator Cellular Encode-Decode	15
Tracking Generator Trunking Cellular Encode-Decode	17

Option Combinations with Cellular (Option 15)

Options Desired	Firmware #
Cellular	04
Cellular Tracking Generator	05
Cellular Trunking	06
Cellular Tracking Generator Trunking	07
Cellular Encode-Decode	14
Cellular Tracking Generator Encode-Decode	15
Cellular Trunking Encode-Decode	16
Cellular Tracking Generator Trunking Encode-Decode	17

Option Combinations with Encode-Decode (Option 11)

Options Desired	Firmware #
Encode-Decode	10
Encode-Decode Tracking Generator	11
Encode-Decode Trunking	12
Encode-Decode Tracking Generator Trunking	13
Encode-Decode Cellular	14
Encode-Decode Tracking Generator Cellular	15
Encode-Decode Trunking Cellular	16
Encode-Decode Tracking Generator Trunking Cellular	17

CUSTOMER RECOMMENDED CHANGES TO TECHNICAL MANUALS

CUSTOMER INFORMATION

NAME (PLEASE PRINT) _____ DATE _____

YOUR TITLE _____ BUSINESS PHONE # _____

COMPANY NAME _____

BUSINESS ADDRESS _____

CITY _____ STATE _____ ZIP _____

PRODUCT INFORMATION

MODEL # _____ SERIAL # _____

MANUAL TYPE

- ☐ OPERATOR'S GUIDE
- ☐ OPERATION MANUAL
- ☐ MAINTENANCE MANUAL
- ☐ ILLUSTRATED PARTS CAT.

PUBLICATION DATE _____

PLEASE BE SPECIFIC IN IDENTIFYING PROBLEMS

PAGE NO.	PARA. NO.	FIGURE NO.	TABLE NO.	COMMENTS

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